Report

The HBT model

ABSTRACT

A physics-based large signal model including thermal dependence has been developed for $Si/Si_{1-x}Ge_x$ HBTs. The alloying composition for the modelled device may vary between $0 \leq x \leq 0.30$, having a pure silicon transistor as a special case. The model takes into account several effects that are important for the operation of $Si/Si_{1-x}Ge_x$ HBTs and is directly related to the parameters in the fabrication process. Using extraction procedures for parameters that inherently are difficult to predict, either due to uncertainties in the fabrication process or due to complex physical relations, a good agreement is found between the model and measurements. The fitting procedure of model parameters against measured data is described in the DC-case and particular effects are discussed. In the RF-case, effects from the variation of key equivalent circuit parameters on the different scattering parameters are discussed.

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The HBT model

INTRODUCTION

Progress in Silicon Germanium (SiGe) technology has yielded Heterojunction Bipolar Transistors (HBTs) with f_{max} of 90 GHz [1], using a common emitter configuration, and excellent noise figures for frequencies up to at least 10 GHz [2]. For analysis and implementation of Si/SiGe HBTs in non-linear microwave applications, the access to an accurate physics-based large-signal model with parameters directly related to the fabrication process and describing the physical properties of SiGe is of great importance. The thermal properties of the Si/SiGe HBT which can play an important part in power applications, such as frequency multipliers, has also to be taken into account in a model. From a research point of view it is also of interest to have a model whose parameters can relate circuit performance to technological parameters defining the transistor. In order to fill these needs a modified Ebers-Moll model has been developed for Si/SiGe HBTs.

BACKGROUND

THE PHYSICS OF THE HBT

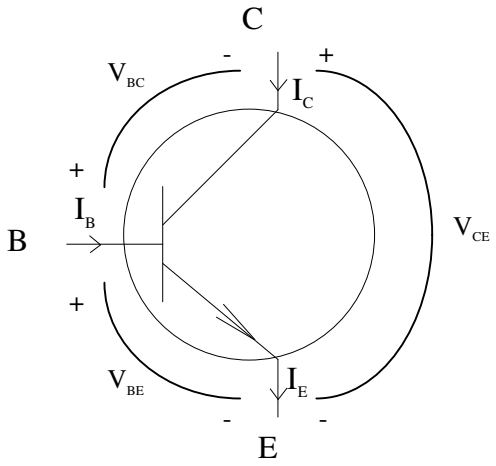

Fig. 1. Schematic picture of the NPN transistor. Currents and voltages for the device are defined.

The bipolar junction transistor (BJT) is generally treated as a current controlled device where the current amplification factor, β, is defined as [3]:

$$\beta = \frac{\partial I_C}{\partial I_B} \tag{1}$$

where I_C and I_B are defined as in Fig. 1. Equation 1 can be translated to more physical terms as [3]:

$$\beta = \frac{D_{eB} n_{iB}^{\ 2}}{W_B N_B} \frac{W_E N_E}{D_{hE} n_{iE}^{\ 2}} \tag{2}$$

where a short base and emitter and a negligible base recombination has been assumed. The intrinsic carrier concentrations, n_{iE} and n_{iB} can for a BJT be considered to be equal.

The device can also be treated as a voltage controlled device where the transconductance, g_{BC} is defined as:

$$g_{BC} = \frac{\partial I_C}{\partial V_{BE}} \tag{3}$$

From a physics point of view, this is a more correct description of the device. The current on the output is clearly controlled by the voltage on the input, from the injection of electrons from the emitter into the base. Due to the well defined reverse injection of holes from the base to the emitter which creates a current on the input and the strict relation between the input and output current (in the ideal case), however, this definition stands back for the previously described.

Equation eq. 2 shows the relation between the injection of carriers from the emitter into the base and the injection of carriers from the base to the emitter. If a large β is desired, the numerator should be as large as possible and the denominator as small as possible. In an ordinary BJT the possibilities are to set $N_E >> N_B$ and/or making W_B small. A wide emitter does not improve the behaviour very much as W_E in eq. 2 would be substituted for the diffusion length of the minority carriers (holes in an NPN structure) when W_E becomes too big. This puts rather strong constraints on the device and a good trade-off between the parameters is necessary. For the current amplification, a low N_B and small W_B is desirable, but at the same time the doping and width of the base must be large enough to withstand the depletion occurring in the junctions so that a punch-through of the base does not result. Furthermore a high base doping allows a higher current density before high injection effects occur caused by the minority carriers concentration reaching the doping level in the base. A high base doping in combination with a large base width gives a low base lead-resistance which is important. At the same time though it is necessary to keep the base-width low so that the delay caused by the diffusion of the minority carriers through the base is kept low. In conclusion it can be said that the device is highly dependent on the design of the base.

In the heterojunction bipolar transistor (HBT), a bandgap difference has been introduced between the emitter and base, see Fig. 2, to increase the degrees of freedom for the design. The bandgap difference can be accomplished by having two

different material combinations like AlGaAs in the emitter and GaAs in the base and collector which gives a single heterojunction bipolar transistor (SHBT), see Fig. 2b. It is also possible to just introduce a different material in the base as is done in the SiGe HBT, where a strained layer of SiGe is grown. This creates then a double heterojunction bipolar transistor (DHBT) since both emitter and collector consist only of Si, see Fig. 2a.

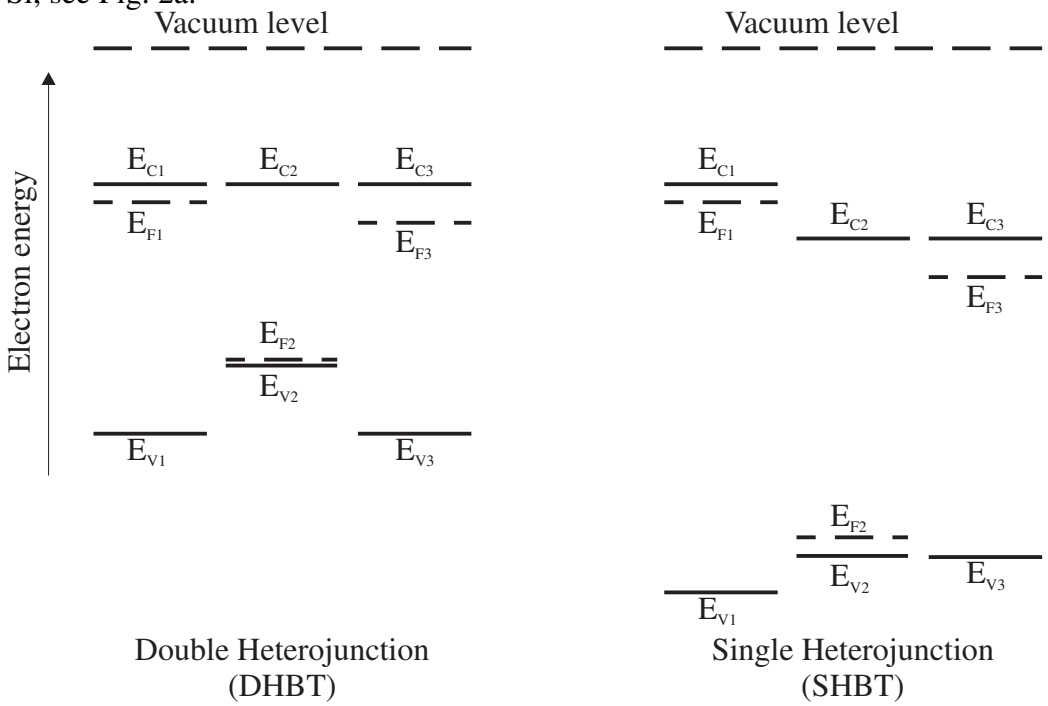

Fig. 2 Comparison of band diagrams for Si/SiGe/Si DHBT and a SHBT AlGaAs/GaAs/GaAs where both transistors are of NPN-type. E_V, E_F and E_C define valence band-, Fermi- and conduction band level, respectively. The energy levels are drawn to scale for a comparison between the two structures (distance to vacuum level is decreased to fit the figure).

The effect is still the same though for the both types: β increases drastically with increasing bandgap difference. The reason for this can be seen in eq. 2 and eq. 4. The intrinsic carrier concentration is strongly dependent on the bandgap in the following way [3]:

$$n_i \propto \sqrt{e^{\frac{-E_g}{qV_T}}} \tag{4}$$

$$V_T = \frac{k_B T}{q} \tag{5}$$

Thus the current amplification factor for the HBT can be defined as:

$$\beta_{HBT} = \frac{D_{eB}}{W_B N_B} \frac{W_E N_E}{D_{hE}} e^{\frac{\Delta E_g}{k_B T}} \quad (6)$$

where ΔE_g is the difference in bandgap between the emitter and base. Depletion width of the base-emitter junction has been considered negligible in comparison to W_B and W_E since the junction is forward biased. As the second term in eq. 6 can amount to several orders of magnitude it is no longer necessary to keep the constraints put on the BJT. Most importantly, the base doping can be increased to values above the emitter doping and still maintain an adequate gain. This means that the base width can be lowered without risking neither punch-through nor a too high base lead-resistance. The current density can also be increased which means that an HBT can be made smaller compared to a BJT which also decreases parasitics.
Thanks to these changes the unity current gain frequency (f_t) increases and more importantly for microwave applications, the maximum frequency of oscillation (f_{max}) increases. The biggest impact has here the base lead-resistance which can be seen from the expression [4]:

$$f_{\max} = \sqrt{\frac{f_t}{8\pi R_B C_{BC}}} \quad (7)$$

where R_B is the whole base-lead resistance and C_{BC} is the collector capacitance.
There are also approaches to grade the bandgap of the base to create a drift field for the minority carriers in order to decrease the base delay, but this would unfortunately result in a lower bandgap difference at the base emitter junction which is not desirable. A trade-off between high β_{HBT} and low base delay could here be considered.
The concept of increasing device performance by introducing different bandgap structures was suggested early by Shockley [3], but due to limitations in the fabrication technology the practical development of the HBT did not begin until the early seventies when the technology of molecular beam epitaxy (MBE) developed [5].

THE STUDIED DEVICE

In this work, mainly double mesa devices (see Fig. 3) fabricated by Daimler Benz Research Center (DBRC) in Ulm, Germany have been studied. With this design DBRC has at present the world record of f_{max} [6]. Sub-micron dimensions are achieved with optical lithography by employing a selfaligning process, see Fig. 3. Using MBE, the process facilitates well controlled and very steep doping profiles in thin layers, see Fig. 4, 5.

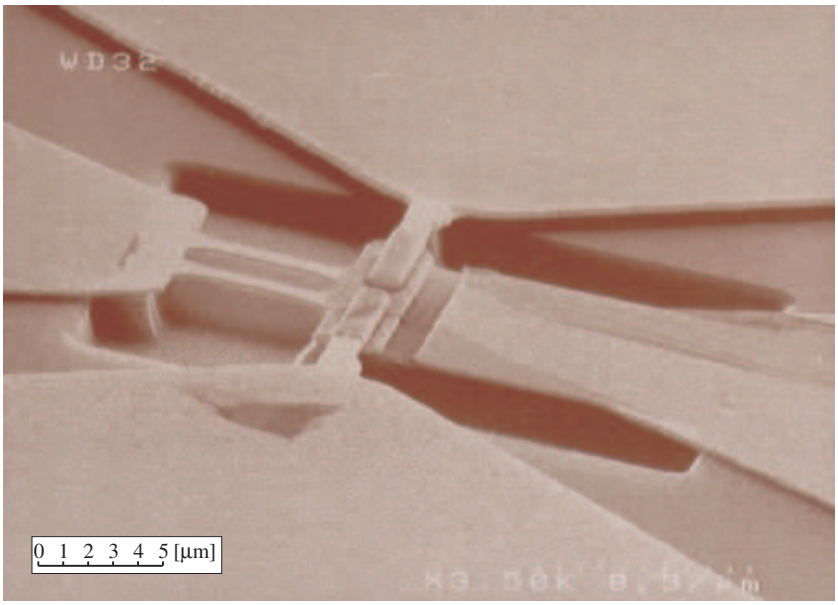

Fig. 3 Scanning electron microscopy (SEM) picture of a transistor fabricated by DBRC. Base contact metallisation is on the left side. Collector contact metallisation is on the right side.

To get a the base contact close to the intrinsic base and thus minimise the base lead resistance, a selfalignment procedure has been employed. In the first step the emitter contact has been defined which can be seen as the highest lying metal in Fig. 3. By using this metallisation as etchmask when removing the emitter-layer, a slight undercut can be accommodated which assures that the subsequent metal deposition for the base-metal will not short-circuit the device, see Fig. 4. A very short baselead from the extrinsic base contact to the intrinsic transistor can thus be accomplished with optical lithography. The undercut of the emitter can be estimated to between 0.1 and 0.2 µm. To isolate the device, a deep groove is etched around the whole transistor, see Fig. 3. To facilitate access for the etchant under the wide base contact, the metallisation is made with holes, see Fig. 3.
What can be noticed is that not all material has been removed under the base-metallisation and that the device has a fairly large amount of open surfaces. This can give rise to parasitic currents.

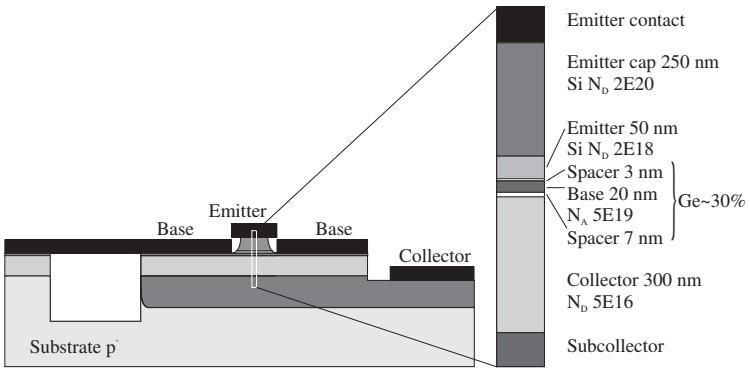

Fig. 4 Schematic picture of the inner part of the transistor. Doping profile and thicknesses are generic values.

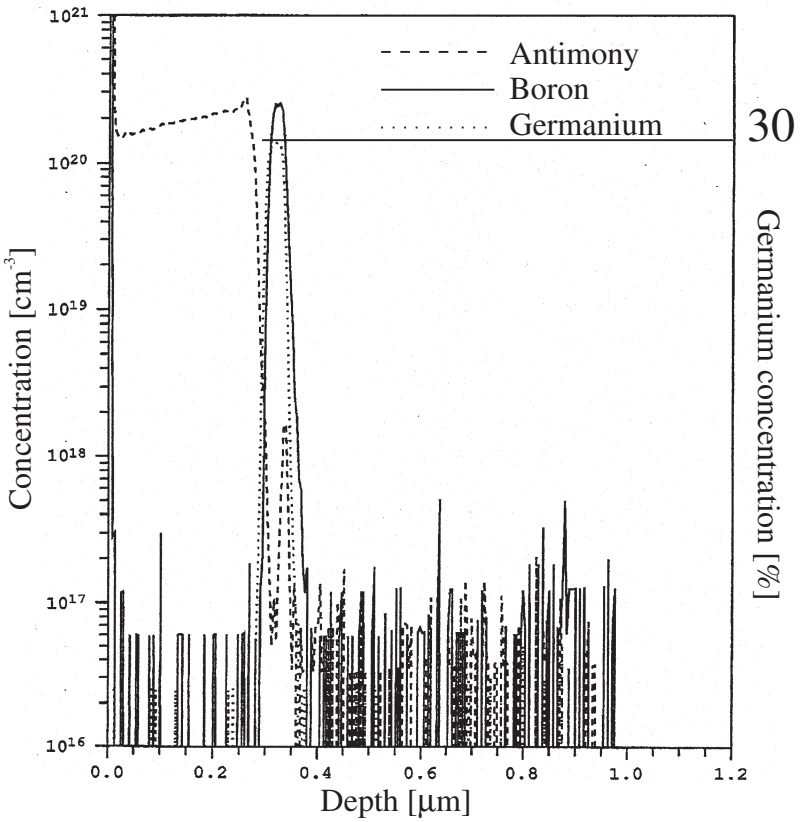

Fig. 5 Measured data of doping and alloy levels in a sample of Si/SiGe, aimed for HBT fabrication, using secondary ion mass spectroscopy (SIMS).

DIFFERENT DEVICE MODELS

A device model is an important tool in any kind of design work. Some different types have been presented for the BJT and in general these can be considered to be aimed for two purposes [7]: to describe how the device interacts within a circuit with other devices and/or to relate device behaviour to device physics. Depending on what kind of application the model is developed for, the approach in defining the model differ; from purely physical or mathematical to empirical or phenomenological. An important issue for models is the trade-off between accuracy and complexity. A good prediction of device or circuit behaviour is naturally important, but by using a more complex model the computing effort and thus also time consumption increases. Fortunately the computing power has steadily increased since the advent of the computers, but this has also been accompanied by increasing complexity in the models and, not to underestimate, the complexity in the designed circuits of which one device only is a small part.

With an increasing amount of elements in a device model there are also more degrees of freedom. These are unfortunately seldom orthogonal which means that there does not necessarily need to be a unique parameter set for a certain solution, or in other words, during extraction or other type of method for finding the parameters, it's not

obvious how to set the relative importance or impact between the different elements that make up the model.

EBERS-MOLL

The first model to be presented for the BJT was the Ebers-Moll model (EM) [3]. It is a physical model and in its most fundamental version there are only two diodes in parallel with two current generators. The diodes correspond to the two junctions, causing injection of carriers into the base. The current generators model how these carriers are swept through the depletion region of the opposite junction. Due to losses, e.g., recombination in the base, this current is slightly smaller and this is accounted for by the current transport factor (α). In a slightly expanded version, series resistors are added to the three terminals and two capacitors are added in parallel with the junctions. These elements can physically be related to contact and lead resistances for the resistors and junction- together with parasitic capacitances for the capacitors.

GUMMEL-POON

In the Gummel-Poon model (GP) the terminal currents are related to the stored minority charge in the base rather than the injected currents into the base which is the case in the EM model [3]. The GP thus treats the device from a more physics-based point of view compared to the engineeringwise very intuitive EM.

Both the EM and GP have been extended from their initial definitions and they are basically equivalent, comparing the EM^3 and the extended GP [8].

VBIC, MEXTRAM

New models for BJTs have been developed where the aim has been directed at creating a model which is easily implemented in a circuit simulator. This means having model equations that are continuous for all values of the variables and are explicit functions of only internal branch voltages, thus preventing any iterative solutions. Furthermore the equation parameters must be easily extracted from well defined measurements.
As an industrial model it is also important to, to some respect, be standardised in order to facilitate portability and comparability. The Mextram model [9] [10] from Philips Research, The Netherlands and the VBIC model [11] [10] from the VBIC Consortium (with members from the major companies in the semiconductor industry) are the two major candidates for replacing the so far essentially solitaire GP in circuit simulators, e.g., SPICE.
Due to the origin in industrial applications the goal has been to achieve an as correct modelling of device behaviour as possible on the sacrifice of relation between model parameters and physical understanding.

THE DEVELOPED MODEL

BACKGROUND

The initial reason for creating a model has been an interest in μwave applications and the possibility of studying designs using the HBT for these. Previously, several small signal models have been proposed, but at the start of this project, essentially no model including large signal effects was available for the SiGe HBT.
Of interest for this model was to have an as versatile set-up as possible in order to make it possible to account for many different devices (or types of devices). From a scientific (research) point of view it is also interesting to have a model which makes it possible to relate parameters to the actually modelled device in order to create a feedback from the final design to the fundamental component. This could give information on how the device could be altered to improve the performance in a particular application or, which might be even more important, to understand what part of the device/design made the application not work as desired. To meet these demands, the model should contain components that independently describe different effects or processes in the transistor in a way that makes it possible to study certain parts more thoroughly or add components to account for new effects. Furthermore, to make the model more general, the equations should not be dedicated to a certain alloy concentration of SiGe, but rather account for a variable combination where a special case should be a regular Si BJT.

CONCEPT/IDEA

The Ebers-Moll model was chosen as foundation for further development into a suitable model. From an early point the choice in favour of a model consisting of physics related lumped elements was clear. With the possibility of modelling the different physical processes inside the device with different components, a clear partition between the different effects is possible and an intuitive understanding of the device function is also facilitated. By using physical processes to describe the function of the device, the values of the initial parameters should also be possible to calculate from data defining the actual device, e.g., device geometry, layer structure and specific parameters for contacts etc. (contact resistivity). A drawback with a physics related model consisting of lumped elements can be that certain distributed effects are difficult to model properly. This is however a general problem and where practical aspects necessitates it, phenomenological or even empirical models for the physical effects can be implemented. Preferably this approach is only done during the process of developing a more correct description based on physics, but the trade-off between research investment and accuracy pay-off must clearly be taken into consideration. The usage of lumped elements should however not be seen as an absolute decision. If computing power allows and the understanding of the physical

effects is not obscured, one could consider a hybrid model where more complex or distributed parts are modelled, using for example finite element analysis (FEM).

CONCEPT FOR THE IMPLEMENTATION

From a physical point of view the transistor can be divided into three different levels or complexities: the embedding part connecting the device, the extrinsic part of the transistor and the intrinsic part of the transistor, see Fig. 6, compare with Fig. 3.
In the same way the model has been divided into three different shells corresponding to these levels. The reason for this can be found in the complexity of the model and in how different parts of the model have been implemented. The embedding part consists of only linear and passive elements who are immediately extracted and thus not calculated from technological data. Further on these passive elements do not scale with transistor dimensions since they essentially have a fixed, much larger dimension independent from the transistor type, see Fig. 6 a. The extrinsic part of the transistor (see Fig. 6 b) has in addition to the passive and linear elements also non-linear elements that are initially calculated from parameters related to the physical device, but not momentarily updated during simulations. Finally there is the inner core (see Fig. 6 c) which relates mainly to the intrinsic device. Using a special feature of the implementation program, the symbolically defined device (SDD), this part is continuously updated throughout a simulation. This means that it is possible to find for example a junction temperature rise caused by an internal power dissipation both from a DC-bias and RF power.

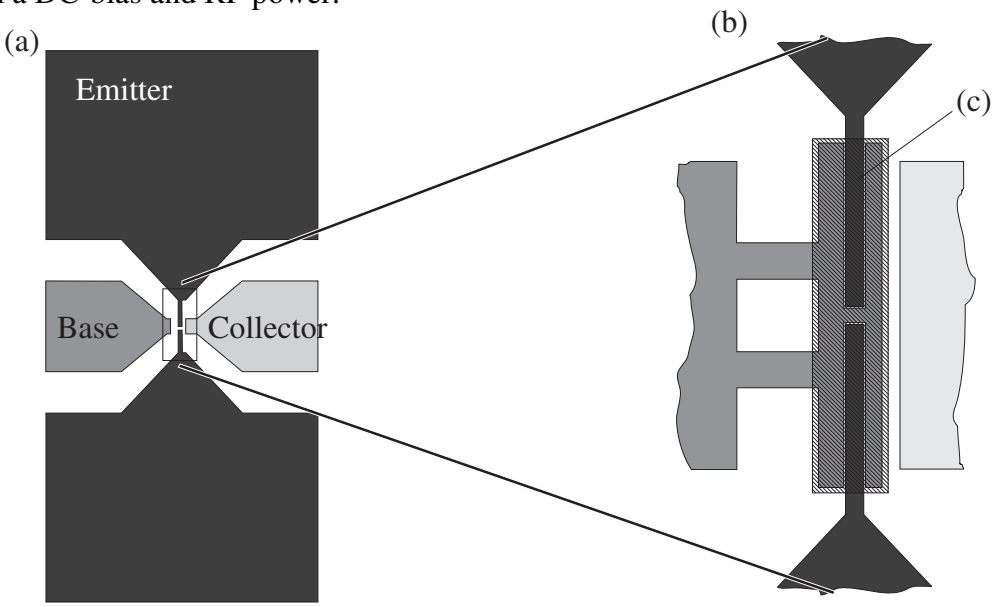

Fig. 6 Top view of a typical transistor. (a) the left figure shows the contacting pads. (b) a close-up showing the actual transistor (shaded part) can be seen in the right figure. (c) intrinsic part of the transistor is defined as the part immediately under the emitter-finger. Base-metallisation can be seen on both sides of the emitter-finger.

A NOTE ON ACCURACY IN THE CALCULATIONS

In the following equations and expressions the number of significant digits vary. This is caused by the variation of digits in the equations found in the literature. Empirical expressions may not be possible to evaluate with more than two digits of accuracy whereas some analytical expressions may have constants that can have very high accuracy; which not necessarily assures a correct result as the model itself might be incomplete. For practical reasons a final result with an accuracy of two digits is often sufficient and for this reason it is desirable to use at least three digits within the equations, but more digits are clearly useful. In the expressions that follows, the amount of significant digits in the expressions reflect therefore what has been found in the literature.

THE EMBEDDING SHELL

The embedding shell corresponds to the parasitic elements related to the contacting pads, see Fig. 6 and 9. This means shunting capacitances between the pads (C_{BEpad}, C_{CEpad} and C_{BCpad} respectively) in series with a possible substrate resistance (R_{BEpad}, R_{CEpad} and R_{BCpad} respectively) and series inductances and resistances (L_{Bpad}, R_{Bpad}, L_{Cpad}, R_{Cpad}, L_{Epad} and R_{Epad} respectively) for each connecting terminal, see Fig. 9. The shunting capacitances are created through the semiconductor and are weakly bias dependent. The resistances and inductances contacting each node of the transistor originates solely in the contacting metal (see Fig. 6) and are thus completely bias independent.

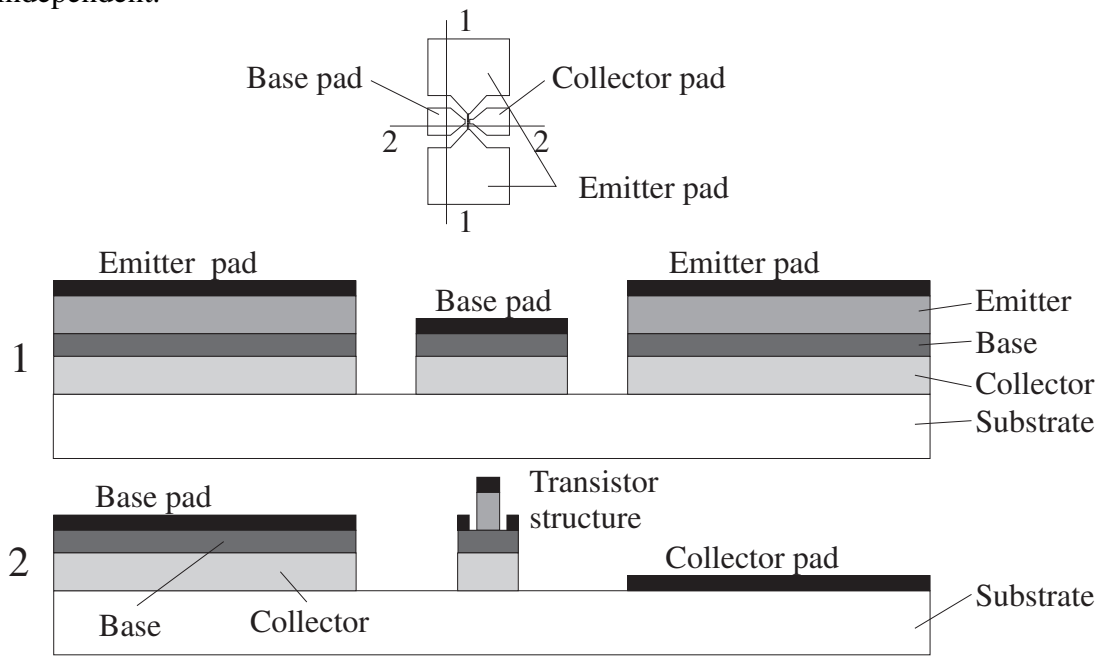

Fig. 7 Schematic picture of how the pads are put on the substrate. The thickness of the different layers is strongly exaggerated for clarity. The numbers indicate the different cross sections.

So far the studied devices have been realised on substrates with high enough resistivity for any essential coupling to the substrate not to occur, see Fig. 8 which shows S_{11} of open structures. The collector pad lies immediately on the substrate, the base pad lies on the base layer which is on top of the collector layer, see Fig. 7. Under the base pad is thus a large base-collector junction in connection with the collector pad through the substrate. This should ensure a good insulation between the different terminals due to the high resistivity in the substrate. In a similar way the emitter and base layers are removed outside the pad metallisation and thus there is essentially no connection between their corresponding pads since there will at least be one reverse biased junction to prevent current from flowing. For the collector pad there can possibly be a shunting load to ground as the substrate can be mounted on a grounded carrier.

The deviation in the measured phase value, as seen in Fig. 8 a, from that of an ideal open structure (corresponding to a single point at magnitude one and phase zero) can be attributed to the very short transmission line, about 50-100 μm, that actually exist from the probe connector to the physical open structure. As can be seen in Fig. 6, an open structure corresponds to a pad structure where the metallisation for the inner transistor (see Fig. 6) has been omitted. This deviation has been verified using a method of moments simulator (Momentum from HP), see Fig. 8c. A distance of 100 μm would correspond to a phase shift of approximately 25^o (30^o) at 40 (50) GHz in the Smithchart which compares well with an analytical calculation of the phase shift assuming a coplanar waveguide. The dielectric constant is then assumed to be the arithmetic mean of the dielectric constant in air and the one of Silicon. In the model, these transmission lines have been included as coplanar waveguides (CPW) in the base- and collector lead, assuming a pad configuration as in Fig. 6.

Had there been any coupling to the substrate, this would have appeared as a measured result closer to a short-circuit. The coupling to the substrate should however be further studied if material with lower resistivity is to be used, e.g. 10 Ωcm which is more common material for regular fabrication of Si devices [12]. The doping can there create shunting parasitics who drastically affect performance in a degrading manner. As an example, a pad size of $100\text{x}100\mu m^2$ laying on top of a 1 μm oxide as insulator could give rise to a capacitance of 345 fF. The resulting S_{11} of such a capacitance connected immediately to ground can be seen in Fig. 8d. This shunting effect can however be decreased with a thicker insulator. One method is to put the pads on a 10 μm thick polyamide.

With high ohmic substrates there can also be a possibility of bulk currents due to a large space charge region (SCR) between base and collector in which generation-recombination (GR) processes can occur.

At the outer end of each node (see Fig. 9) is an RC parallel circuit, e.g. R_{Bprobe} in parallel with $C_{RFshunt}$ for the base node, connected to model the effects caused by the connection between the measurement equipment and the device. At DC-measurements, the resistive load can have an impact whereas at S-parameter measurements the calibration process assures that measurement data present the result

at the probe tips. With a good measurement set-up consisting of high quality cables, these resistances can usually be neglected.

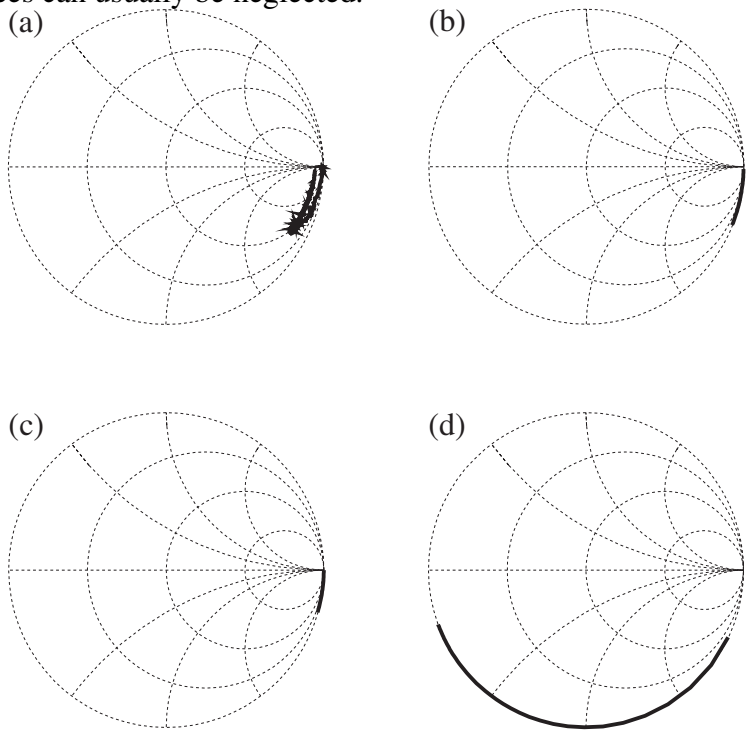

Fig. 8 Measured and calculated S_{11} for different circuits. (a) measured data for two 'open' test structures: lossy (non-ideal) structure with a reflection coefficient (radius) smaller than unity for all frequencies and an almost ideal open structure with a reflection coefficient close to unity, (b) calculated data for a short transmission line terminated in a high impedance (open), (c) calculated data for a 2D pad-structure using the Momentum (from HP) simulator, (d) calculated data for a short transmission line in parallel with a 345 fF capacitance (open with connection via the substrate to ground). Frequency is from 1 to 50 GHz except for the measurement of the non-ideal open structure where the frequency is from 1 to 40 GHz.

In some measurements of test structures, losses can be noticed as a magnitude of S_{11} and S_{22} which is smaller than unity, see Fig. 8 (a). These can generally not be attributed to losses in the transmission lines as these are fabricated on high impedance substrate. Losses physically related to the area of the actual transistor is then more likely as this part of the wafer undergoes more processing steps unprotected. A tentative approach at modelling these losses has been done with the shunting and series resistances nearest to the actual transistor (R_{BEloss}, R_{CEloss}, R_{Eloss} and R_{Closs} respectively). The capacitances and inductances related to these resistors ($C_{DCblock}$ and $L_{DCshunt}$ respectively) are included to prevent these lossy effects to have an impact on the DC performance. The resistance in the base-lead (which should be called R_{Bloss}) has been omitted since the current approach has from experience been sufficient for modelling the lossy test circuits. The shunting resistances (R_{BEloss} and R_{CEloss}

respectively) reflect the common emitter configuration of the pad structure. Depending on device fabrication, the losses can vary and often the lossy effects need not to be included. Thus the redundancy of resistors in each terminal connection can be explained with handling different situations.
For modelling the different test structures (open, short and through), the nodes 'Base', 'Collector' and 'Emitter' in Fig. 9 are connected differently. For open, all nodes are disconnected. For short all nodes are connected to eachother and for through, 'Base' and 'Collector' are connected to eachother while 'Emitter' is disconnected.

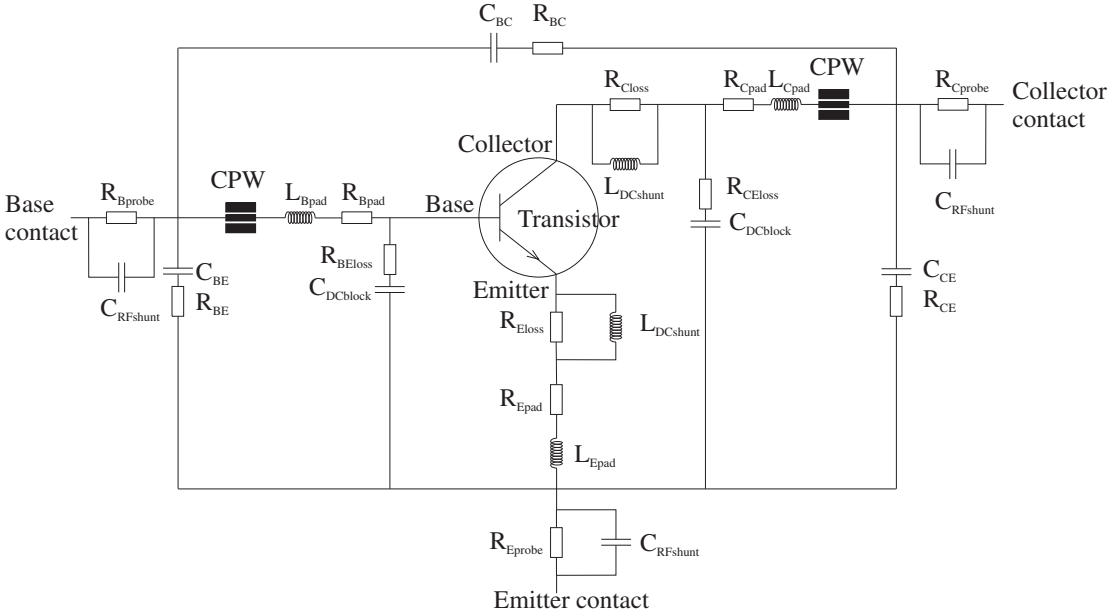

Fig. 9 Schematic of the embedding shell. The transistor symbol depicts where the transistor is to be connected. The components 'CPW' are coplanar transmission lines.

THE EXTRINSIC SHELL

The extrinsic part of the transistor, see Fig. 10, form the surrounding shell around the intrinsic transistor. In a general 'collector down' design this means that the extrinsic base-collector junction and the distributed base connection is accounted for here. In addition, the contact resistances for the three terminals are accounted for. In the base lead, a metal-semiconductor resistance (R_{Bcont}) in parallel with a depletion region capacitance (C_{Bshunt}) connects the metal pad with the base layer. Immediately under this contact lies physically the extrinsic part of the collector which has been modelled with a diode (i_{BCext}) in parallel with a shunting capacitance (C_{BCext}) and finally a series resistance to account for the undepleted part of the collector (R_{BCext}). In the simulator, the sub-circuit consisting of C_{BCext}, i_{BCext} and R_{BCext} are substituted with a diode element taking these three components into account. The base sheet leading from the contact into the intrinsic base is modelled with a single resistance (R_{Blead}). Using a lumped element works well at high base doping. The voltage drop along the base sheet inside the intrinsic transistor is then very small and thus also the variation of the injection currents due to variation in base-emitter voltage.

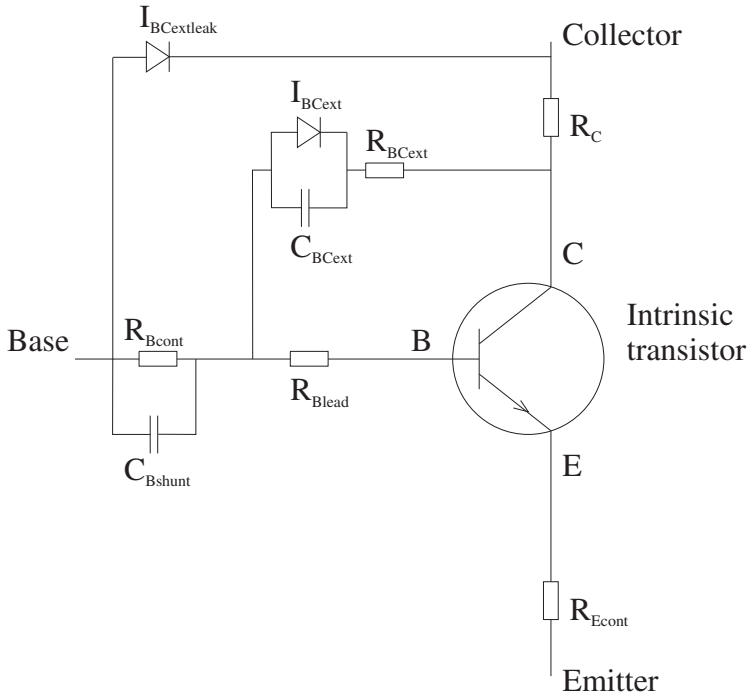

Fig. 10 Schematic of how the extrinsic part of the transistor has been modelled. The transistor symbol shows the connection to the intrinsic device.

Care should however be taken when modelling transistors with low base doping (e.g. pure Si). A rough estimate of minimal base doping where the voltage drop can be neglected can be made assuming that the voltage drop between any two points inside the intrinsic transistor should be lower than $V_T=k_BT/q$ which corresponds to a variation in collector current of approximately the natural exponential (e), see eq. (10). Assuming a finger-shaped intrinsic transistor (see Fig. 6), a minimum basedoping (N_B) can be defined as:

$$N_B > \frac{L_F I_B}{2 * 2qV_T W_B W_F \mu_{hBtrans}}, \qquad (8)$$

where L_F is the length (in the direction of the base current flow) of the intrinsic emitter finger from one side to the other and W_F is the width of the finger, compare with the similar definition in an FET. $\mu_{hBtrans}$ is the hole mobility parallel to the base layer. The other terms are common definitions. The base is also assumed to be contacted from both sides of the finger (see Fig. 4), thus causing the current to be splitted and the distance for the current to flow to be half of L_F.
For a device with $L_F/W_F=0.05$, $W_B=100*10^{-7}$ cm, $\mu_{hBtrans}=125$ $cm^2V^{-1}s^{-1}$[13] and $I_B=10$ μA, the base doping must thus be larger than

$$N_B > \frac{0.05 * 10 * 10^{-6}}{2 * 2 * 1.602 * 10^{-19} * 0.0259 * 100 * 10^{-7} * 125}$$

$$>2.4*10^{16}\ cm^{-3}.$$

It should be remembered that this is a lower limit and that L_F can be considerably bigger (caused, e.g., by contacting from only one side).
For the contacting of the collector and emitter layers, there are also resistances (R_{Econt} and R_C respectively). The value of the collector contact resistivity is not so critical since the buried sub-collector facilitates a large contacting area and the device performance is not very much affected by the value of the resulting contact resistance as long as it is small compared to resistances outside the device. The resistance of the sub-collector is also included in R_C, thus the index 'C' instead of 'Ccont'. The actual resistance of the sub-collector is difficult to extract due to the position in the circuit and a value of 5 Ω has been used as a typical value [14].
The emitter contact resistance is more critical as a voltage drop over this component immediately affects the injection over the base-emitter junction.
In addition to the diode modelling the extrinsic part of the base-collector junction there is also a diode ($i_{BCextleak}$) to account for the possible leakage currents occurring on the surfaces of the mesa structure between the base and collector contact, see Fig. 3. The usage of a diode implies a current flowing in only one direction which does not have to be the case for this current. The diode model element works however well for modelling the impact of this current on transistor behaviour throughout the studied bias ranges.

THE INTRINSIC SHELL

The intrinsic transistor is the most thoroughly modelled part and it consists of several different components to account for the different physical processes occurring.
In each junction, two different diodes model the electron and hole injection respectively (i_{Ee} and i_{Eh} for injection in the base-emitter junction and i_{Ce} and i_{Ch} for injection in the base-collector). The reason for treating the two kinds of injections separately is due to their dependence on different energy bandgaps. The electron injection from the emitter and collector into the base is inversely proportional (through the intrinsic carrier concentration, n_i) to the exponential of the bandgap in the base through the following relation:

$$J_{0e} = \frac{qD_{eB}n_{iB}^{\ 2}}{N_B W_B} \tag{9}$$

where n_i^2 is defined as:

$$n_{iB}^{\ 2} = N_{Cond}N_{Val}e^{\frac{-E_{gB}}{k_B T}}, \tag{10}$$

q, D_{eB} and W_B can be considered as independent of T whereas $N_{Cond}*N_{Val}$ is proportional to T^3. This gives the bandgap dependence of the electron injection.

Similar expressions are valid for the hole injection from the base into the emitter and the collector. The conduction band throughout the transistor has been assumed to be continuous thus not creating any bandspikes (existing for example in abrupt AlGaAs/GaAs junctions). Heavy doping could have an effect on the conduction band continuity [15], but a proper fabrication process seem to make the impact of these effects small. The ideality factor of the collector current is very close to unity in gummel measurements which would not be the case with a bandspike occurring [16]. A very small band offset can not be excluded, but it can not be identified as a distinct effect and is thus not included in the model.

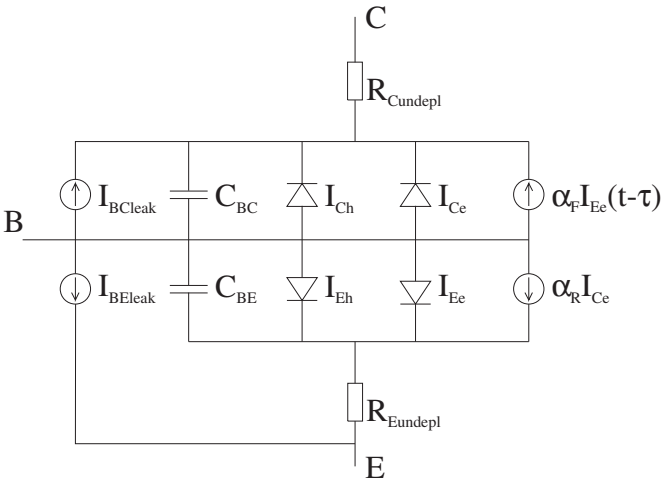

Fig. 11 Schematic of how the intrinsic part of the transistor has been modelled. The terminals C, B and E denotes the points where the intrinsic part connects to the extrinsic part (see Fig. 10).

Due to the temperature dependence in the exponential, eq. 10 is strongly temperature dependent. Since there are different energy bandgaps in the emitter and the base, the saturation currents and thus also the injection currents will vary differently with temperature. By modelling the currents in this physics related way, the electron current is readily available and since this is the only part that is swept through the base to the collector, the current generator corresponding to this mechanism only need to account for an electron loss due to recombination in the base layer which, compared to the exponential term in eq. 9, can be considered fairly constant with respect to temperature. In the approach where both injections are considered in the same diode, a more complex expression for the then temperature dependent α for the current generators, see Fig. 11, needs to be defined (which also obscures the physical connection).

The two capacitors (C_{BE} and C_{BC} for the base-emitter junction and the base-collector junction respectively) account for the junction capacitance and are based on the expression used in SPICE [17]. During normal operation of the HBT however, the current density in the collector SCR can become so high that the injected majority carriers compensate the charge of the ionised impurity atoms (note that local charge neutrality does not exist in the SCR). In this case more impurity atoms need to be ionised in order to keep global charge neutrality which has an expanding SCR as

result. This means that the junction capacitance decreases and also the collector transit time should increase. So far, only modelling of the collector capacitance lowering has been included whereas the transit time change not has been possible to implement in the simulator due to limitations in the SDD.
In series with the current generators and the capacitances are the resistances that account for the undepleted regions of the collector ($R_{Cundepl}$) and emitter ($R_{Eundepl}$), respectively. The resistance in the collector will thus vary as the collector SCR varies. Since the depletion region of the emitter is extremely small during all operation, this resistance could be assumed to be constant, but for completeness also the modulation of this value is modelled. Where computing time is a key figure, this part should be possible to remove from the SDD.
In each junction is also one more current generator which is voltage dependent (I_{LBE} and I_{LBC} respectively). These are modelling the leakage currents occurring. They can be related to different processes such as surface currents on mesa type devices and high injection effects causing a higher recombination in the base. Their parameter values have not been calculated as they vary between devices in a very unpredictable way, probably due to an incomplete passivation process of the devices. The empirical approach can partly be justified by that the need for these generators hopefully goes away in devices where the technology has reached a more mature stage. At the moment, the connection of the base-emitter current generator suggests to only account for surface currents as it is connected past the intrinsic bulk resistance, but with minor corrections in the expressions calculating the currents, this generator can also account processes occurring inside the device, e.g., the high injection effects that occur in the base emitter junction. Due to the empirical treatment of this component and the underlying effects, no effort has been made to justify or verify its placement.
In the present implementation the aim has been to use explicit expressions for calculating the various parameters. This has led to that the capacitance and resistance in each side of the base (e.g. C_{BC} and $R_{Cundepl}$ for the collector side) have been calculated using junction voltages rather than using the resulting currents. In doing so, effects related to the currents (e.g. expansion of the SCR as described above) are very difficult to model in a correct way. With a new approach where the currents (primarily the collector current) are included implicitly in the simulation, a more straightforward implementation of, e.g., the capacitance could be realised. This would make the value at the same time accessible for other elements in the intrinsic device. The technique of using implicitly defined currents inside SDDs is well described in [15].

IMPLEMENTATION OF THE MODEL INTO A COMMERCIAL SIMULATOR

The model has been implemented in Microwave Design System (MDS) from Hewlett Packard which is a fairly complex system for design of microwave components. The essential parts are a 2.5D simulator (Momentum) for passive, distributed circuits and a simulator with SPICE like environment (DCS) for lumped element circuits. DCS

also contains the SDD which facilitates modelling of currents and voltages through both explicit and implicit equations. These equations are also treated in both the frequency and time domain which makes the implementation of, e.g., time delays very straightforward. Some limitations exist however in the SDD.

DESCRIPTION OF THE SDD

The SDD can be seen as a tool for defining the relationship between voltage and current between two nodes. These nodes are considered to be one port. Each port has two state variables: voltage drop between the two nodes (called $_V_n$) and current flowing from one node to the other (called $_I_n$). For each port either an explicit expression for the current, $_I_n$ where n is the index for the port, or an implicit equation relating $_I_n$ to any other state variable (to any $_I_m$ and to any $_V_m$) can be defined. These are evaluated in both the time and frequency domain in one of the following manners:
For explicitly defined currents:

$$V(\omega) \underset{1}{\overset{FFT^{-1}}{\Longrightarrow}} v(t) \underset{2}{\overset{f}{\Longrightarrow}} \hat{\imath}(t) \underset{3}{\overset{FFT}{\Longrightarrow}} \hat{I}(\omega) \underset{4}{\overset{weighting}{\Longrightarrow}} I(\omega) \qquad (11)$$

The variables are column vectors where the elements correspond to the individual ports. In step 1 an inverse fourier transform of the voltage input spectrum over all connected ports is done. Their corresponding values in the time domain are thus available in all equations. At step 2 this can be used for explicitly calculating a value, also incorporating non-linear effects, for the current in the time domain. Important to note however, is that evaluation is not pointwise individual. The whole time sweep is evaluated at one time which makes functions relating values at different timepoints impossible. This is a drawback as, e.g., time varying time delays occurring in the Base-Collector SCR due to the strong variation in SCR width during big voltage swings thus are not possible to implement. At the moment this is not a big constraint since the added delay in the collector in relation to the whole delay through the transistor is fairly small, but in high power applications where a long low doped collector is used, the effect should be studied further. The current waveform is in step 3 transformed into the frequency domain where in step 4 it is multiplied with a frequency dependent function. Different operators in the time domain can thus be implemented, e.g., a time derivative which equals to $j\omega$.

For implicitly defined currents the steps are similar, however somewhat more complicated. Instead of using only the voltage spectrums as input, a vector consisting of both the voltage and current spectrums,

$$X(\omega) = \begin{bmatrix} V(\omega) \\ I(\omega) \end{bmatrix} \qquad (12)$$

is used and instead of explicitly calculating a value for I(ω), the solver tries to minimise an error, E(ω):

$$X(\omega) \underset{1}{\overset{FFT^{-1}}{\Longrightarrow}} x(t) \underset{2}{\overset{f}{\Longrightarrow}} e(t) \underset{3}{\overset{FFT}{\Longrightarrow}} \hat{E}(\omega) \underset{4}{\overset{weighting}{\Longrightarrow}} E(\omega) \qquad (13)$$

In step 1 an inverse fourier transform of the input spectrum (X) is done. At step 2, a function operates on the time series vector which yields a result e(t). This is in step 3 transformed to the frequency domain where in step 4 a weighting function as described in the explicit case is multiplied to the spectrum. The resulting spectrum is an error which the solver tries to find spectrums of X(ω) so that E(ω)=0.

EQUATIONS FOR FINDING THE PARAMETERS OF THE COMPONENTS

In the following section the equations used for finding parameter values to the lumped elements in the embedding shells and the actual currents (and for some cases, voltages) occurring in the SDD will be defined. The order is done from outer components going towards the intrinsic transistor. To point out relative importance, calculations of typical values have been done. When nothing else is mentioned, the values shown in Table 1 are used.

Table 1.
Nominal values used in calculations.

W_E	[cm]	$.070*10^{-4}$	W_B	[cm]	$.030*10^{-4}$	W_C	[cm]	$.300*10^{-4}$
N_E	[cm^{-3}]	$2*10^{18}$	N_B	[cm^{-3}]	$1*10^{20}$	N_C	[cm^{-3}]	$5*10^{16}$
$\varepsilon_E/\varepsilon_0$		11.7	$\varepsilon_B/\varepsilon_0$		13.1	$\varepsilon_C/\varepsilon_0$		11.7
A_E	[cm^2]	$20*10^{-8}$				A_C	[cm^2]	$40*10^{-8}$
A_{ECont}	[cm^2]	$20*10^{-8}$	x_{Ge}		0.30			
W_F	[cm]	$20*10^{-4}$	T_0	[K]	293			

Some terms considering fundamental physics of the semiconductor are defined in the section following this.

THE EMBEDDING SHELL

In the embedding shell all parameter values are directly extracted from measurements and has thus no expressions related to them. As mentioned before this is consistent with the model since these parts to a very low degree scale with dimensions of the actual transistor, see Fig. 6. Method for extraction of the values will be described in a later section.

THE EXTRINSIC SHELL

The extrinsic shell consists of the components connecting the intrinsic terminals of the transistor to the pads as described before. The metal base-layer contact (R_{Bcont}) is calculated using:

$$R_{Bcont} = \frac{\rho_B}{A_B}, \tag{14}$$

where A_B has been defined as (A_C-A_{Econt}) which corresponds to the base area outside the intrinsic transistor. ρ_B is the contact resistivity between metal and the heavily doped base layer. A_C is the total collector area defined by the perimeter of the base metal contact inside the etched groove. A_{Econt} is the area defined by the emitter-finger metallisation.
The contact resistivity can vary, but is difficult to extract unless it for some reason is high. A conservative initial value which has been chosen for the contact resistivity is $\rho_B=5*10^{-6}$ Ωcm^2 [13]. The emitter contact (A_{Econt}) can be well defined through the lithography (verified through SEM) and the value given from the design can be used as a good initial value. The collector area which is defined by a very deep etch can vary somewhat and need also to be extracted. A calculated value of R_{Bcont} is 25 Ω..
In parallel with the resistance is a shunting capacitance. This was first inserted when it was noticed that the base contact resistance did not have a big impact on RF-parameters and it should thus be shunted. The origin could, in a poor contact, be related to the metal-semiconductor interface as [3]:

$$C_{Bshunt} = \sqrt{\frac{q\varepsilon_B N_B}{2V_j}} * A_B \tag{15}$$

$$=0.6 \text{ pF, assuming } V_j=1V.$$

The assumption of V_j is not fully correct, but the impact on C_{Bshunt} from a variation in V_j is small. V_j itself can roughly vary between 0.8 V and 1.1 V, assuming a base of heavily doped Germanium or Silicon, respectively.
The extrinsic diode, accounting for the pn-junction outside the intrinsic base-collector junction has a saturation current calculated as[3]:

$$I_{BCext00} = q(A_C - A_{Econt})\left(\frac{D_{eB}n_{iB}^{\ 2}}{W_B N_B} + \frac{D_{hC}n_{iC}^{\ 2}}{\left(W_C - X_{jC00}\right)N_C}\right) \tag{16}$$

where

$$X_{jC00} = \sqrt{\frac{2N_B \varepsilon_B \varepsilon_C V_{jC00}}{qN_C(\varepsilon_B N_B + \varepsilon_C N_C)}} \tag{17}$$

Only steady state thermal dependence is included. Since the current in the normally reverse biased junction is very small, this does not create any big errors. The bias dependent capacitance is the important component and this can be adequately modelled with the expression for the junction capacitance for a zero bias condition which the simulator then uses to calculate the bias dependent capacitance.

$$C_{BCext00} = \frac{\varepsilon_C A_C}{X_{jC00}} \tag{18}$$

In series with the capacitance is also the resistance to account for the undepleted region of the collector. The expression for this resistance is [3]:

$$R_{BCext} = \frac{W_C - X_{jC00}\sqrt{1 - \frac{V_{BC0}}{V_{jC00}}}}{q\mu_{eC0} N_C A_C} \tag{19}$$

All individual parameters has to be given as fixed values since the lumped elements in this part of the simulator cannot be updated throughout the simulation, therefore the added '0' as a suffix. In order to get a reasonable value, the base-collector voltage (V_{BC0}) is set to -1 V which corresponds to a collector-emitter voltage of about 2 V in an ordinary bias condition. The capacitance is not evaluated only at this voltage since the simulator automatically treats this part as bias dependent as it is part of the diode model element.

The base sheet resistance (R_{Blead}) is calculated as:

$$R_{Blead} = \frac{L_B}{2qW_F \mu_{hBtrans} \frac{W_B}{2} N_B} \tag{20}$$

=12.5 Ω assuming L_B=1.5 μm which is an effective length of the resistive sheet. The open distance between the base metallisation and the intrinsic base is lower than 1.5 μm, but to account for the distributed behaviour occurring under the base contact (all current does not float in the infinitesimally narrow part that is the closest to the intrinsic base, see Fig. 4) a higher value has been chosen. Metallisation for the base contact has been assumed on both sides of the emitter finger. The outside base layer under the metallisation is assumed to have approximately half the thickness of the intrinsic base layer due to overetch [18].

The emitter contact resistance (R_{ECont}) is calculated similarly to the base contact resistance:

$$R_{Econt} = \frac{\rho_E}{A_{Econt}} \qquad (21)$$

$$= 25\Omega$$

The contact resistivity can vary and need to be extracted. An initial value which seems to be reproducible and conservative is $5*10^{-6}$ Ωcm^2 [13]. Extraction is however necessary since the impact on device behaviour from this resistance is big at high currents (see later section describing the fitting of parameters towards the Gummel plot).
The collector resistance (R_C) includes both the contact resistance and the resistance in the sub-collector lead. These are difficult to distinguish between eachother, but from a modelling point of view R_C does not play an important part. Neither f_t nor f_{max} is heavily affected by its value and further investigations regarding the partitioning of R_C has thus not been done. Choosing an initial value of approximately 5 Ω for small devices has been practically sufficient [14] and a possible variation, to fit a plot of I_C vs. V_{CE}, can be done.

THE INTRINSIC SHELL

In this part all implementation has been done using the SDD as described above. Thus the expressions need to describe the actual currents and, possibly, voltages. To achieve convergence during the simulations, it is very important to have somewhat bounded and differentiable functions, preferably also with a continuous derivative [15]. A special expression for the exponential function has thus been defined which is upwards limited by a linear function and has a continuous derivative:

$$\text{expon}(_value) = \begin{cases} e^k * (_value - k + 1) & _value > k \\ e^{-_value} & _value \le k \end{cases} \qquad (22)$$

where k is chosen to 69 ($e^{69} \approx 10^{30}$) to allow sufficiently high values in the calculations.
The current through the two diodes in the base-emitter junction are thus calculated as:

$$i_{Ee} = I_{Ee0} K_{IEe} \left(\text{expon}\left[\frac{v_{BE}}{V_T * n_F} \right] - 1 \right) \qquad (23)$$

$$I_{Ee0} = \frac{q A_E D_{eB} {n_{iB}}^2}{W_B N_B} \qquad (24)$$

$$i_{Eh} = I_{Eh0} K_{IEh} \left(\text{expon}\left[\frac{v_{BE}}{V_T * n_F} \right] - 1 \right) \tag{25}$$

$$I_{Eh0} = \frac{qA_E D_{hE} n_{iE}^{\ 2}}{W_E N_E} \tag{26}$$

In the base-collector junction, the currents are defined as:

$$i_{Ce} = I_{Ce0} K_{ICe} \left(\text{expon}\left[\frac{v_{BC}}{V_T * n_R} \right] - 1 \right) \tag{27}$$

$$I_{Ce0} = \frac{qA_E D_{eB} n_{iB}^{\ 2}}{W_B N_B} \tag{28}$$

$$i_{Ch} = I_{Ch0} K_{ICh} \left(\text{expon}\left[\frac{v_{BC}}{V_T * n_R} \right] - 1 \right) \tag{29}$$

$$I_{Ch0} = \frac{qA_E D_{hC} n_{iC}^{\ 2}}{W_C N_C} \tag{30}$$

it is here noticeable that the emitter area is used to define the collector current. This comes from the definition of the intrinsic transistor having the area of the base-emitter interface. The constants K_{IEe}, K_{IEh}, K_{ICe} and K_{ICh} are included to facilitate a possible reduction of the different currents. Due to lack of an accurate model for the bandgap narrowing at high doping levels and high Germanium concentrations, the value of the intrinsic carrier concentration in the base can be slightly overestimated [19] (too strong bandgap narrowing) which results in a slightly too big value of i_{Ee} and i_{Ce}. Thus these currents could be multiplied by a factor ranging from 1/3 to 1/2.
After injection of electrons into the base from the emitter, these charges are swept through the base to the opposite SCR, i.e. the base-collector SCR. A slight decrease due to base recombination is accounted for by multiplying the current with the base transport factor (α_F), which is very close to unity (negligible base recombination). The term is fed by the user at the time of simulation.
In the base-collector SCR the electrons can reach high enough energy to knock out more electrons when colliding with the lattice which can cause an avalanche multiplication. The multiplication factor is defined as [20]:

$$M_C = \frac{1}{1 - \left| \frac{V_{BC}}{V_{Cbreak}} \right|^4} \tag{31}$$

and is also added to the expression.
To account for the diffusion delay through the base (τ_B) and the drift delay through the base-collector SCR (τ_C), a multiplication term (φ) for the collector current generator inside the SDD is introduced in the frequency domain as [21]:

$$\varphi = \frac{\sin(\omega * \tau\ )}{(\omega * \tau\ )} * e^{-j\omega\tau} \tag{32}$$

$$\tau = \tau_C + 0.22 * \tau_B + \tau_F \tag{33}$$

which, at small $\omega*\tau$, corresponds to a frequency dependent phase shift. The τ_F is an adjusting parameter to make simulations at high frequencies fit with measurements. Both τ_C and τ_B are difficult to calculate exactly due to the inherent inaccuracy lying in the technological parameters.
The variable ω is created by the simulator at runtime and corresponds to the angular frequency that is calculated. This gives some possibility of controlling parameters in the frequency domain like introducing a delay as a frequency dependent phase shift. Relating values calculated by the simulator between different frequency points, e.g., $I1(\omega)=f(I2(\omega+\omega_0)$, is not possible more than for very simple relations as the expressions are defined in the time domain. Relating values calculated by the simulator between different time points, e.g., $I1(t)=f(I2(t+\tau_0))$, is not possible due to limitations in the software which is the reason for implementing the delay in the frequency domain.

Calculation of the currents through the two junction capacitances is done by using the SPICE model [17] [15]. The charge build-up on the edges of the SCR surfaces are calculated as:

$$Q = \begin{cases} Q_r(v), v < \alpha\ V_j \\ Q_f(v), v \geq \alpha\ V_j \end{cases}, \text{ where} \tag{34}$$

$$Q_r(v) = -2C_{j0}\sqrt{V_j(V_j - v)} \tag{35}$$

$$Q_f(v) = \frac{C_{j0}}{\sqrt{1-\alpha}}\left(v - \alpha\ V_j + \frac{(v - \alpha\ V_j)^2}{4V_j(1-\alpha\ )}\right) + Q_r(\alpha\ V_j) \tag{36}$$

Here, V_j is the built-in voltage, v is the applied voltage and C_{j0} is the junction capacitance at zero bias (v=0). Two regions have been chosen to avoid unrealistic values when applied voltage reaches the built-in voltage. These regions are defined by

the constant α (not related to the current transport factor defined for the current generators).
The reason for not using the classical definition of a depletion capacitance, having the following expression:

$$C_j(v) = C_0\sqrt{\frac{V_j}{V_j - v}} \tag{37}$$

is that it reaches infinity when v=V_j and the corresponding charge build-up is then not defined. This is thus avoided by having an expression identical to the classical at reverse bias and to a forward bias voltage α*V_j from which point a linear continuation is made. This approach is very suitable for the SDD since the expression for the charge build-up can be evaluated in the time domain and later multiplied by jω in the frequency domain which yields the spectrum of the time derivative, this being the displacement current.
The calculations for both junctions use eq. 34. Since these capacitances only accounts for the intrinsic parts of the transistor, the emitter area is used when calculating the individual C_0 for both junctions. In the base-emitter junction, a diffusion capacitance has been included to account for the charge build-up change in the base due to the diffusion time. The charge build-up is calculated as:

$$Q = i_{Ee} * \tau_B \tag{38}$$

The time derivative of this charge is then calculated as described above.
Further on the effect of charge compensation as discussed earlier has been implemented partially for the base-collector junction. Assuming a constant doping in the collector and an evenly distributed current, the widening of the SCR can be expressed as:

$$\frac{L'}{L} = \frac{1}{1 - \frac{I_C}{qN_C A_E v_s}} \tag{39}$$

Where I_C is collector current and v_s (=10^7cm/s) is the electron saturation velocity. For low currents, the expansion is very low, but at already at a current of 8 mA, the charge compensation has caused the SCR to expand by a factor of two. This is only valid for the low doped collector and as soon as the SCR reaches the sub-collector, charge compensation has no real effect. The inclusion of this effect has only been considered in the intrinsic part of the collector whereas one could intuitively expect that the electrons, from the Coulomb force, would spread through the whole of the collector. Calculations made using FEM tools (Atlas from Silvaco) show however

that for the thin collectors which so far have been treated, almost all current flows immediately under the interface defining the intrinsic transistor.
A problem with the implementation of the charge compensation effect is the difficulty of finding the collector current flowing through the SCR and thus causing charge compensation; displacement currents do not affect. The current has also to be found during the simulation. So far, different attempts using the complete collector current have been used which works fairly well with S-parameter simulations since the RF-part then is infinitesimal, thus not adding any displacement current in the simulation. Care must however be taken when using the collector current during large signal RF simulations since the displacement current then can become a substantial part of the total current. Different tentative approaches to solve this problem in a direct way have been employed, but none has been quite successful. An indirect way would be to use the calculated value of the depletion region width which is used for other components, see below, and with this calculate a direct parallel plate capacitance which is multiplied with the time derivative of the applied voltage (further discussed in ref. [15], appendix A). This necessitates however a free port for evaluating the time derivative of the applied voltage in each time-point which consumes computer power and it is not quite clear how big impact this capacitance has on overall performance. Assuming a base-collector built-in voltage of 1 V, the whole collector is fully depleted at base-collector voltage of -2.5 V without any current flow. If a collector current of 6 mA is injected, the whole junction is depleted already at zero bias. Possibly, applications with low reverse base-collector voltage and high collector currents could be affected. A frequency doubler designed with the developed model could be an example of a case where this bias occurs in combination with large-signal RF [22]. Calculated data using the model compared however well with measured data.

Additional current generators

In addition to the current generators that already have been discussed, there are also generators to account for the non-idealities in the base current appearing as a base current not being parallel to the collector current in a Gummel plot, see Fig. 12. Since these current generators are based on purely empirical data, the primary objective has been to make them suitable for fitting. In addition to a voltage dependence, they are also depending on junction temperature which is very important for a correct modelling of the temperature dependency of the whole device, see Fig. 13. What is important to point out here is that these generators do not stand for the total temperature modelling of the device which in that case would make this model unphysical. However, for the overall behaviour, this part need also a correct thermal modelling. In Gummel plots of an ordinary HBT, three essential regions of the base currents can be distinguished, see Fig. 12. The gummel plot is a graph of both base and collector current versus base-emitter voltage for a constant base-collector voltage (usually set to zero). Collector and emitter can also be interchanged for a reverse gummel measurement.

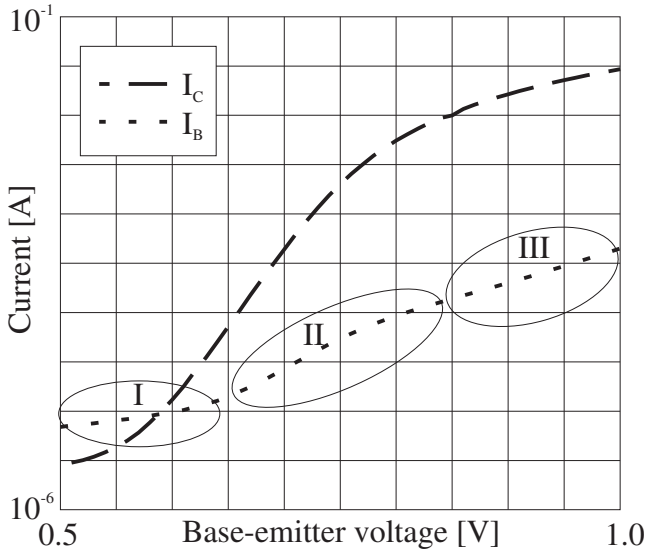

Fig. 12 A Gummel plot of a typical HBT, showing the three important regions of the base current.

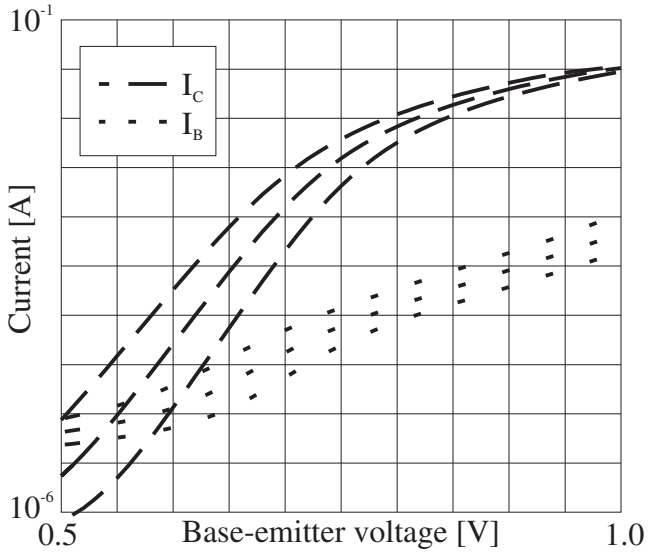

Fig. 13 Gummel plot at three different junction temperatures (293K, 323K and 373K respectively) for a typical HBT. Increasing currents correspond to increasing temperature.

At low junction voltages a current with a very weak slope is found, see region I, Fig. 12. This shows dependence on light and can thus be attributed to generation processes. The following region, region II in Fig. 12, exhibit a more ideal behaviour of the base current having an ideality factor between 1 and 2, indicating generation-recombination processes [3]. In this region essentially all biasing is made (corresponding to collector currents between 1 and 10 mA for the studied devices). The third region, region III in Fig. 12, exhibit high injection effects where the 'roll off' in the base current due to the voltage drop over the emitter-lead resistance is not following the collector (emitter) current which could be expected that it would. Instead it is steadily increasing. A possible explanation could lie inherently in how the Gummel measurement is made, namely in that the intrinsic base-collector junction

becomes forward biased due to the voltage drop over the collector resistance. The impact from the collector resistance is however a much stronger effect than the measured one and it can thus be clearly distinguished (see Fig. 14).

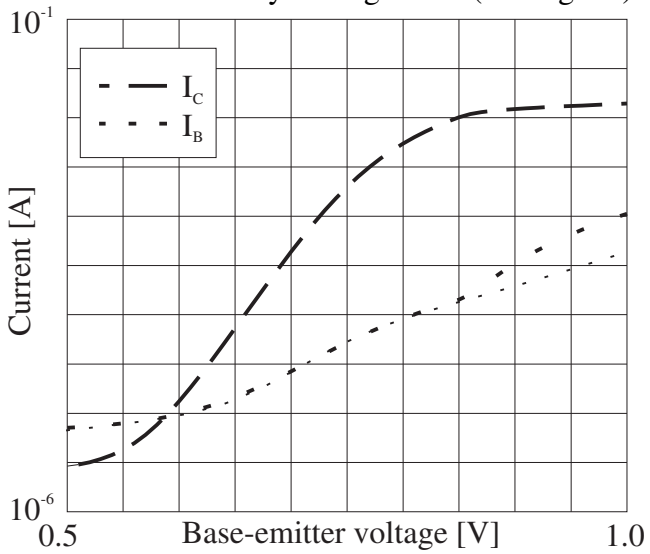

Fig. 14 Example of a Gummel plot in which the base-collector junction has been forward biased due to the voltage drop over the collector-lead resistance. The thinner curve shows the base current when the impact from the collector-lead resistance is negligible.

The approach to model these additional parts of the base current has thus been empirical with an emphasis on facilitating easy and accurate fitting. For this reason the current generator (I_{LBE}) is decomposed into three expressions; each defining one of the above discussed regions. The expression for one of these parts is:

$$I_m(V) = J_{Em} * A_E * \text{expon}\left(\frac{\text{V - V}_{\text{offset}_\text{m}}}{V_T * n_m} + \left[\frac{V_{therm_m}}{V_T} - \frac{V_{therm_m}}{V_{T0}} \right] \right) \qquad (40)$$

where m=1,2 or 3. V_{offset} indicates the voltage point in the Gummel plot where the different parameters are extracted. J_E, n and V_{therm} corresponds to the current density, ideality factor and thermal dependence respectively in this voltage point. The term V_{T0} is set to the thermal voltage of the temperature where the non-thermally dependent parts are extracted. The term V_{offset} is not necessarily needed since it is possible to extract from zero voltage, the resulting extraction procedure becomes however more difficult since small variations of the terms in the exponential have a very strong impact. Depending on how the base current looks in the Gummel plot, these currents are combined differently. Usually a sum of the current in the low and intermediate voltage is performed, having the current in the high voltage region as an upper limit. Since they are one component of the base current, their impact can be slightly obscured by the hole back-injection which is the reason for the somewhat strange approach of using one current as a limiter. A physical explanation for this is not quite obvious, but a further investigation should then be concentrated on the high-

current regime where the inaccuracy more likely can be attributed to an incomplete physical modelling of the intrinsic transistor, i.e., the observed effects do not necessarily disappear with an improved technology. It should however be noted that the high-current regime occur at high current densities (J>5*10^4 -1*10^5 A/cm^2) and it is questionable whether the device should be operated there. As can be seen in Fig. 12, the collector current exhibits a nearly ideal behaviour with an ideality constant less than 1.05 in the region where the impact from the emitter-lead resistance is negligible (approximately for the base-emitter voltage corresponding to region II of the base current, see Fig. 12).
The current generator in the base-collector junction (I_{LBC}) has so far not been used as leakage currents occurring on the surface of the device are accounted for by $I_{BCextleak}$.

The value of the resistance in the undepleted regions of the collector and emitter are calculated using:

$$R_{Cundepl} = \frac{W_C - X_{jC}}{q\mu_{eC} N_C A_E} \tag{41}$$

$$R_{Eundepl} = \frac{W_E - X_{jE}}{q\mu_{eE} N_E A_E} \tag{42}$$

where X_{jC} and X_{jE} are the width of the depletion regions in the collector and the emitter respectively. They use the common expression for space charge region as:

$$X_j = X_{j0}\sqrt{1 - \frac{V}{V_j}} \tag{43}$$

$$X_{j0} = \sqrt{\frac{2\varepsilon V_j}{qN}} \tag{44}$$

where ε, V_j, V and N are the dielectric constant, built-in voltage, applied voltage and the doping respectively in the considered SCR. This assumes a base doping that is at least one order of magnitude higher than the collector and emitter which is often the case. The addition in the expression to account for a lower doped base (mostly important for the emitter-base SCR) is easily accomplished and have been done when so has been needed. Care must be taken that the SCR does not evaluate to a value beyond the thickness of the material or becomes negative. The previous happens at high reverse applied voltages and the latter at positive applied voltages above the built-in voltage. To implement these restrictions, a somewhat cumbersome approach needs to be taken. In the simulator, conditional expressions can be given as:

Result= if (cond. statement) then *Expr1* else *Expr2* endif

which means that *Result* is given the value of *Expr1* if the conditional statement is valid and the value of *Expr2* otherwise. However, there is an important limitation included: if either of the expressions evaluates to an erroneous result, e.g., sqrt(-1) for an expected real result, then the total result is unpredictable. Even if the expression to be used according to the conditional statement evaluates correctly, the result is not clear. For this reason, one must take extra care not to evaluate any expression to an undefined value. Therefore all expressions are evaluated to an unconditionally positive (or zero) value. Using the conditional statement, the region for the input parameters are known within each restriction and it is still possible to calculate the correct final result.

The resistances are implemented as separate ports in series with the collector and emitter junction respectively. To find the currents, the voltages can be immediately divided by the calculated resistance. For this reason, the undepleted region is not allowed to vanish, but is set to a minimum of 1% of the complete layer-width. The collector current is used for calculating the internal power dissipation which in turn yields the temperature rise of the junction. This means that a direct definition of the current would give circular references. One way of solving this is to have 'parallel' parameters calculated at a given junction temperature . The parameters affected are: E_{gB}, X_{jC0}, μ_{nC} and V_{jC0}. At low power dissipations and low variation in temperatures this is sufficient. For the above chosen parameters, the resistance varies from 1.3Ω to 1.7Ω when changing the junction temperature from 300K to 350K, having a base-collector bias of -2V.
Another way to calculate the current is to use the possibility of an implicit relation. Assuming that port 1 of the SDD is used for this calculation, the following statement is made:

$$_V_1 - _I_1 * R_{Cundepl} = 0 \qquad (45)$$

which iterates the correct current during simulation and $R_{Cundepl}$ can still be temperature dependent although $_I_1$ in this case is used for calculating the internal power dissipation and thus also the temperature. This approach consumes however more computing power.

EXPRESSIONS USED IN THE EQUATIONS

For the equations/expressions above, several parameters are needed that are related to device physics. These will be stated, in no specific order, here and further described. In several cases both an expression for pure Silicon and an expression for an alloy is given. These expressions should give identical results in the case of no Germanium in the alloy (x=0). There is however no point in having a more complex expression than necessary and thus the expressions considering the collector and the emitter assumes

x=0, i.e. pure Silicon. The expressions for the alloy assumes a strained material; relaxed layers would cause a lattice mismatch which would render the transistor more or less useless and is therefore not interesting to consider in this respect.

PARAMETERS RELATED TO THE BANDGAP

In order to get a good modelling of the thermal effects, the bandgap need to be accurately accounted for since the impact, through the often exponential terms, is very big.
The bandgap for the different layers are calculated accounting for thermal variation, bandgap contraction due to heavy doping and possible strain. The last is only made for the base layer. To calculate the bandgap, the width of the doping induced contraction is subtracted from the value of the undoped semiconductor bandgap. This is performed assuming a fixed temperature of 300K. Following, the temperature dependence is accounted for by multiplying the bandgap with a scaling factor which relates the bandgap of undoped silicon at the present temperature to the bandgap of undoped silicon at 300K.

The expression for the bandgap energy is thus [23][24]:

$$E_{gX}(T,x,N_X) = QE_g(T) * \left[E_{gX0}(x) - \Delta E_{gX}(N_X) \right] \tag{46}$$

$$E_{gX0}(x) = \begin{cases} 1.124, & X\ is\ C\ or\ E \\ 0.9646 * (1.165 - 0.75 * x), & X\ is\ B, x \le 0.30 \end{cases} \tag{47}$$

$$\Delta E_{gX}(N_X) = E_1 * \left[\ln\left(\frac{N_X}{N_0}\right) + \sqrt{\ln\left(\frac{N_X}{N_0}\right)^2 + 0.5} \right] \tag{48}$$

$$QE_g(T) = \frac{1.1785 - 9.025 * 10^{-5} * T - 3.05 * 10^{-7} * T^2}{1.124}, \quad T > 170\,K \tag{49}$$

where X is C, B and E for collector, base and emitter respectively, E_1=0.009 eV and N_0=1*10^{17}cm^{-3}. In Fig. 15, the effect of doping, temperature and alloy concentration can be seen. Different expressions for the alloying dependence of the bandgap exist [23][24] and the one in [24] has been chosen to be consistent with the expressions for n_i in strained SiGe also found in [24]. The expression for the bandgap found in [24] gives a slightly higher estimation of the value of the bandgap (maximum 0.05 eV) than the one found in [23] and it can thus be expected that the real value is somewhere in between. For the Si/SiGe interface the whole bandgap offset has been assumed to occur in the valence band in the case of a strained alloy adjacent to pure Silicon as discussed earlier. This means no conduction band spike which occurs in

e.g. AlGaAs/GaAs structures and there affects the electron injection. Possibly, a small offset could be occurring which then has been attributed to a slightly smaller device area or a different ideality constant of the device.

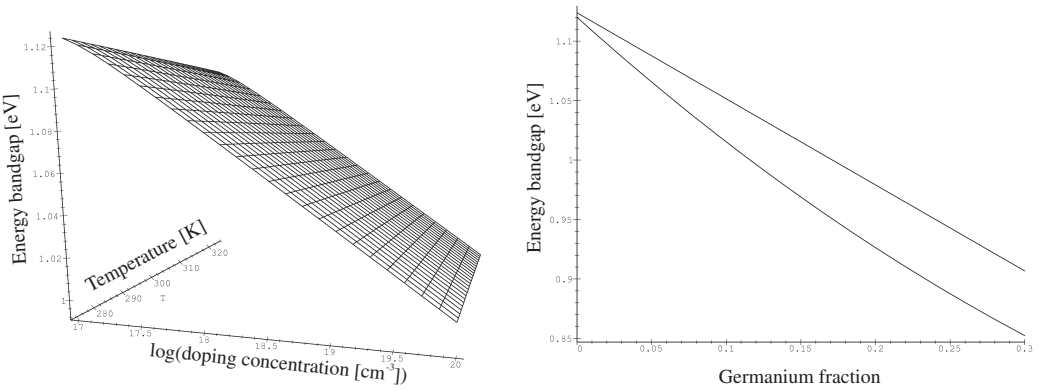

Fig. 15 Energy bandgap versus doping, temperature and alloy combination. (a) Silicon at different doping levels and temperatures, (b) impact of alloying with Germanium, the upper curve is calculated using [24] and the lower curve is calculated using [23].

INTRINSIC CARRIER CONCENTRATION, NI

The intrinsic carrier concentration is needed for the calculation of the saturation currents and is thus an important parameter. For pure Silicon the following expression is used [3]:

$$n_i = 3.59 * 10^{19} * \left(\frac{T}{300}\right)^{3/2} * e^{\frac{-E_g}{2*V_T}} \tag{50}$$

which includes the temperature dependence. In the case of an alloy, the expression becomes more complex [24]:

$$n_i(x,T) = \sqrt{N_{cSiGeStrain}(x,T) * N_{vSiGeStrain}(x,T) * e^{\frac{-E_g}{V_T}}} \tag{51}$$

$$N_{cSiGeStrain}(x,T) = N_{cSiGeXStrain}(T) + N_{vSiGeLStrain}(x,T) \tag{52}$$

$$N_{cSiGeXStrain}(T) = 2 * \left(\frac{2\pi * 0.3272 * m_0 k_B T}{h^2}\right)^{3/2} * \left(4 + 2 * e^{\frac{-0.6*x}{V_T}}\right) * 10^{-6} \tag{53}$$

$$N_{cSiGeLStrain}(x,T) = 2 * \left(\frac{2\pi * 0.2217 * m_0 k_B T}{h^2}\right)^{3/2} * 4 * e^{\frac{-1.0709+1.366*x-0.1615*x^2}{V_T}} * 10^{-6} \tag{54}$$

$$N_{vSiGeStrain}(x,T) = N_{vSiGehhStrain}(x,T) + N_{vSiGelhStrain}(x,T) \tag{55}$$

$$N_{vSiGehhStrain}(xT) = 2 * \left(\frac{2\pi * m_{hhSiGeStrain}(x) k_B T}{h^2} \right)^{3/2} * 10^{-6} \tag{56}$$

$$N_{vSiGeLStrain}(x,T) = 2 * \left(\frac{2\pi * m_{lhSiGeStrain}(x) k_B T}{h^2} \right)^{3/2} * e^{\frac{-0.155 * x}{V_T}} * 10^{-6} \tag{57}$$

$$m_{hhSiGeStrain}(x) = \frac{1}{\frac{1-x}{0.49} + \frac{x}{0.28}} * m_0 \tag{58}$$

$$m_{lhSiGeStrain}(x) = \frac{1}{\frac{1-x}{0.16} + \frac{x}{0.044}} * m_0 \tag{59}$$

where n_i has been calculated using the effective conduction ($N_{cSiGeStrain}$) and valence ($N_{vSiGeStrain}$) band. $N_{cSiGeXStrain}$ and $N_{cSiGeLStrain}$ account for the division of states into the X- and L valley respectively. $N_{vSiGehhStrain}$ and $N_{vSiGelhStrain}$ account for the division of states in the heavy and light hole band respectively.

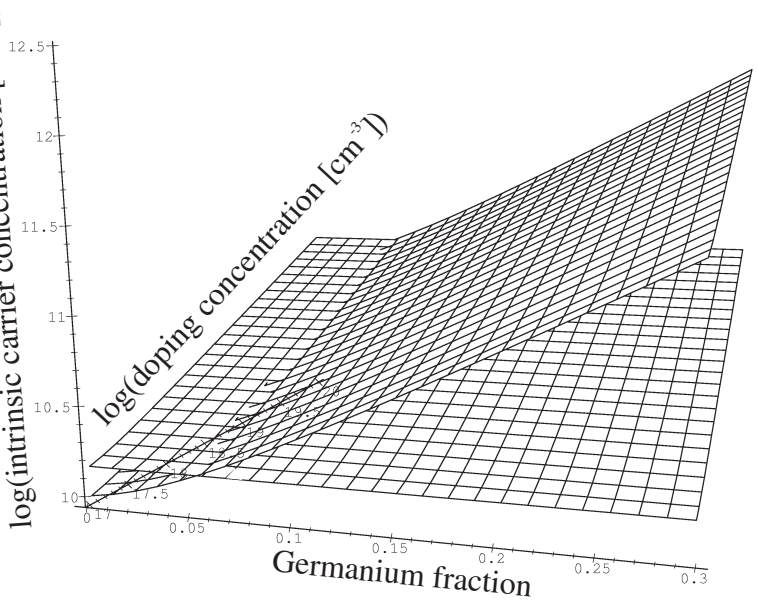

Fig. 16 Intrinsic carrier concentration versus alloy combination and doping. The curve with higher value corresponds to eq. 51 and the lower curve corresponds to eq. 50.

To convert the dimensions into [cm^{-3}] instead of [m^{-3}], a factor of $(10^{-2})^3=10^{-6}$ is used. The effect on intrinsic carrier concentration from adding Germanium can be seen in Fig. 16. As can be noticed, both curves have very similar values at low Germanium fractions, thus indicating that eq. 51 can be used for also the case of no Germanium, i.e., pure Silicon.

BUILT-IN VOLTAGE

The built-in voltage for a junction corresponds to the difference in work function for the two semiconductors, see Fig. 17. This can be calculated as [25]:

$$V_{jX} = \Phi_B - \Phi_X \tag{60}$$

Substituting for known entities, the expression becomes:

$$V_{jX} = \frac{E_{gB}}{q} - \Delta V_B + \mathrm{X}_B - \Delta V_X - \mathrm{X}_X \tag{61}$$

where X_B and X_X is the electron affinity for the base and the opposite layer respectively, see Fig. 17.

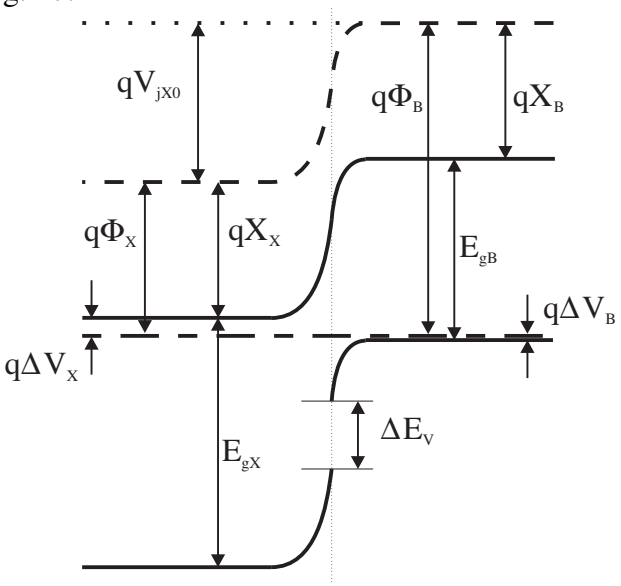

Fig. 17 Band diagram for a zero bias junction showing how the built-in voltage has been calculated. The band levels are defined as in Fig. 2 (notice that the valence band discontinuity does not affect the calculation).

ΔV_X and ΔV_B denote the distance from either conduction band or valence band, depending on doping, to the fermilevel:

$$q\Delta V_X = \frac{E_{gX}}{2} - qV_T \ln\left(\frac{N_X}{n_{iX}}\right) \tag{62}$$

assuming the fermilevel in an undoped material is in the middle of the bandgap. X is here either E, B or C.
At the usually high base doping, $\Delta V_B < V_T$ and can thus be set to zero. Care needs to be taken not to achieve a negative ΔV_B which occur at high N_B. Although this

indicates degenerate doping, the effects of this has not so far been treated. The impact on built-in voltage is still small. Possibly should only a part of the doping ions become electrically activated.

BREAKDOWN FIELD, BREAKDOWN VOLTAGE

For standard applications only the breakdown voltage over the collector SCR needs to be considered. This has been calculated as [20]:

$$V_{Cbreak} = \frac{\varepsilon_C * E_{Cbreak}{}^2}{2qN_C} \tag{63}$$

$$E_{Cbreak} = 2.5 * 10^5 * \left(1 + \left[\log(N_C) - 14\right]^{3/4}\right) \tag{64}$$

With the comparably low doping (see Table 1), the theoretical value of V_{Cbreak} is fairly high (20 V), but in the structures that have been measured so far, the collector has become depleted long before the voltage reaches this value and breakdown occurs instead in the highly doped subcollector. The highest voltage drop that can occur over the collector can roughly be calculated as:

$$V_{\max} = \frac{N_C q W_C{}^2}{2\varepsilon_C} \tag{65}$$

which evaluates to approximately 3.5 V. With charge compensation in the SCR caused by an electron current flow, the effective doping of the collector goes down and the V_{max} decreases even further. The calculation of V_{Cbreak} should thus more be seen as an upper possible limit of the device. In applications where a device will operate close to breakdown, a more accurate value of V_{Cbreak} should be used which then substitutes the above calculation of V_{Cbreak}.

CARRIER MOBILITIES

Electron mobility has been calculated with the following expression [26]:

$$\mu_{nX}(N_X, T) = \mu_{n0}(T) + \frac{\mu_{n1}(T) - \mu_{n0}(T)}{1 + \left(\frac{N_X}{N_{ref}(T)}\right)^{\gamma(T)}} \tag{66}$$

$$\mu_{n0}(T) = 80 * \left(\frac{T}{300}\right)^{-0.45} \tag{67}$$

$$\mu_{n1}(T) = 1430 * \left(\frac{T}{300}\right)^{-2.25} \tag{68}$$

$$N_{ref}(T) = 1.12 * 10^{17} * \left(\frac{T}{300}\right)^{3.2} \tag{69}$$

$$\gamma(T) = 0.72 * \left(\frac{T}{300}\right)^{0.065} \tag{70}$$

which evaluates well for Silicon. There exists so far no reliable expressions for the SiGe alloy and instead a value of 200 cm^2/Vs has been used in alloys where x>0.10 [13]. A recent publication [27] discusses however the topic and an expression could possibly be derived to a further development of the model. The value of the mobility of interest presented in [27] is however very close to the above used, at alloys with x=0.3 and high doping concentration (10^{20} cm^{-3}), which is the configuration mainly found in components studied so far.

Hole diffusion constant has been calculated as:

$$D_X = 1.14 * 10^5 * N_X^{-0.25} \tag{71}$$

which is an approximate expression derived from doping dependent hole mobility given in [3].

DELAYS

The delays for the carrier transport through the transistor originates essentially in two regions: the baselayer, caused by a diffusion transit time and in the base-collector SCR, caused by a drift transit time. It is important to distinguish between a transit time and a transit time delay where the delay is generally defined as [28]:

$$\tau = \frac{\partial Q}{\partial I}\Big|_{V\,constant} \tag{72}$$

The diffusion delay is calculated as [29]:

$$\tau_B = \frac{W_{Beff}^{\ 2}}{\eta_B D_B} \tag{73}$$

The constant in the denominator (η_B) relates to the carrier distribution within the base and is here set to η_B =2.43. For a rectangular concentration profile of the doping impurities, the number would be 2 [3] and for a structure where a built-in field

accelerates the carriers, η_B can increase drastically and thus lower the diffusion delay. The reference that was used for finding eq. 73 [29] calculated the cut-off angular frequency for which τ_B should be the reciprocal. Due to the brief paper it is unclear why $\eta_B \neq 2$ as for a rectangular profile. There might be an additional multiplying factor of 1.215 (to achieve the value of 2.43) which is related to the derivation of the cut-off frequency [29]. The value $\eta_B = 2.43$ is included here since there is no obvious explanation why τ_B should not be the reciprocal of the cut-off frequency. Other publications [30] indicate that the constant should be included as $\eta_B = 2.43$.
The drift delay through the base-collector SCR (τ_C) is calculated as [28]:

$$\tau_C = \frac{X_{jC} + X_{jBC}}{2v_s} \tag{74}$$

where X_{jBC} is the SCR within the base, adjacent to the collector SCR. This is usually negligible in comparison to the value of X_{jC}. The derivation of this delay assumes that the length of the SCR is fairly independent of current which may not always be the case at high injections, see earlier discussion about collector SCR width at large-signal operation.

INTERNAL POWER DISSIPATION AND JUNCTION TEMPERATURE

To be able to calculate the junction temperature, the internal power dissipation needs to be calculated. Following the classical expression, it is calculated as:

$$P = i_C * v_{CE} + i_B * v_{BE} \tag{75}$$

The value of P is then output as a current through one of the ports in the SDD where it can be processed further in an external device, e.g., a resistor which then gives a voltage drop equivalent to the temperature rise, see Fig. 18. An internal evaluation of the junction temperature corresponding to a circuit as the one in Fig. 18a is also possible and it would save two ports in the SDD which can be very valuable, but the restrictions this impose on the possibilities of using different, possibly non-linear (see Fig. 18b), expressions for the junction temperature and the possibilities of thermal cascading of several devices as in a multi emitter-finger device (see Fig. 18c) makes this approach less interesting.

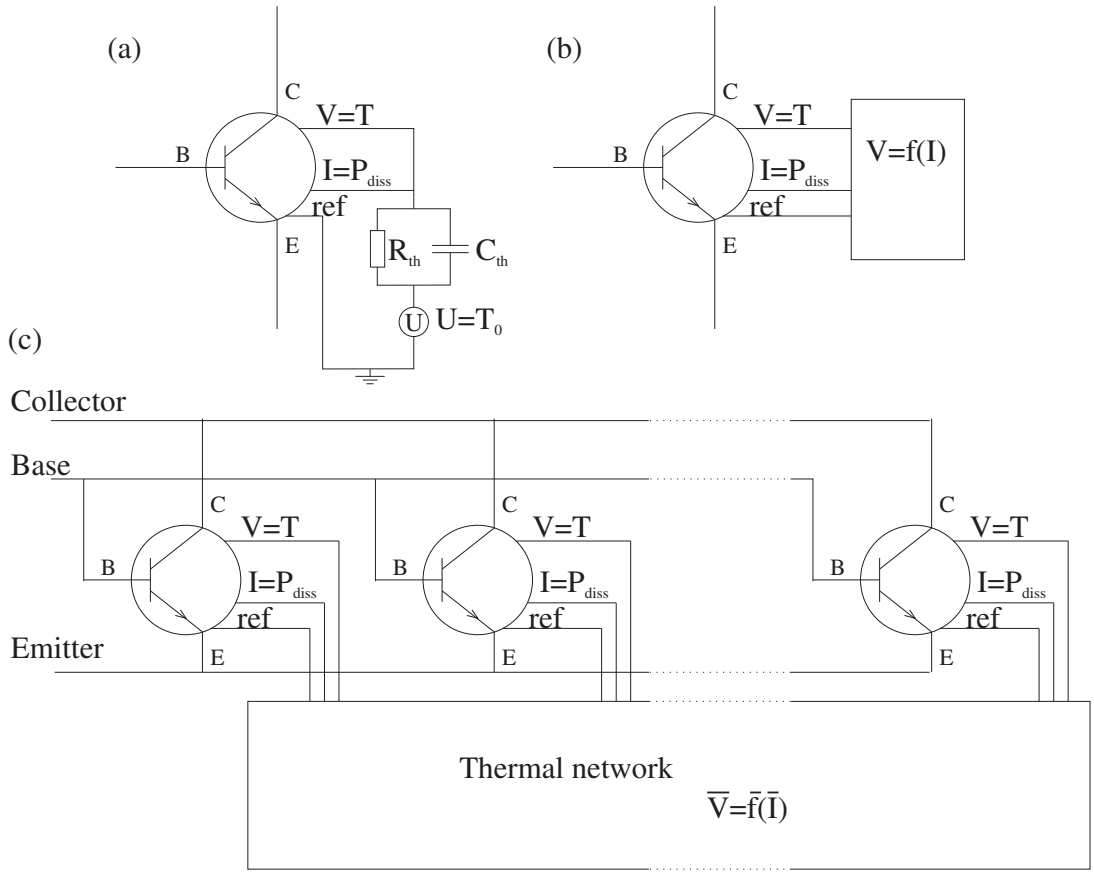

Fig. 18 Schematic of different thermal models. (a) thermal RC-circuit, (b) 'black box' where output voltage is calculated as a function of the input current, (c) example how a multi emitter-finger transistor can be realised through a thermal coupling.

FITTING

A natural step following the calculation of initial parameters for the studied device is to refine the values to fit an existing transistor. The studied transistors differ in electrical characteristics which necessitates the acquisition of individual model parameters for each transistor. As an example, 14 transistors with identical design have been measured on two different wafers and the resulting Gummel plots can be seen in Fig. 19. Although the devices are situated within an area less than 10x10 mm^2, the currents differ by as much as a factor of 5 which indicates that several parameter will need to be fitted or extracted to achieve a good correspondence between calculated and measured data for a specific device. With the coupling of the model parameters to the physical device, it should however still be possible to use the model to indicate how changes of the transistor design would affect the device performance. In the following discussion the word ‘extraction’ should be interpreted as the means of finding a value for a certain parameter which is within a given range. It is thus not a pure extraction in the sense that no initial value is defined. The extraction serves rather as a verification of the calculations and as a pointer for the direction where to adjust the parameters.

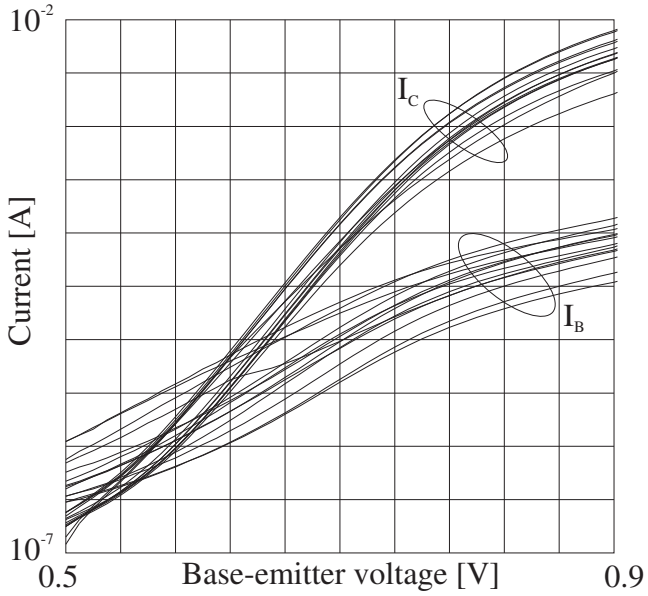

Fig. 19 Gummel plot of 14 transistors of the same design.

PROCEDURE

The extraction procedure can schematically be seen in Fig. 20. A theoretically derived transistor serves as an initial raw device whose parameters are varied within adequate limits. The base-emitter junction area can be expected to vary within, e.g., 0 and -50% of nominal values and an adjustment can thus be used to fit the calculated collector current to measured data. An emphasis has been put in trying to use only measurements where the device has somewhat the same bias as it will have during normal operation. It is more interesting to find a somewhat good fitting of a parameter at a bias which reflects normal operation than a very good match for a parameter which is critical for an unrealistic bias setting. The risk with extracting parameters at extreme bias settings is that one tries to draw conclusions from simplified models. This means that these model parameters may have to be extrapolated back to a point of normal bias operation. This extrapolation is undesirable since the circumstances existing when extracting at an extreme bias may include effects that are not considered by the model, but will affect the fitting of the used parameters. An example of this can be the base-emitter junction capacitance which in a reverse bias condition can give a distinct result which is not applicable for the high forward bias prevalent during normal operation of an HBT.

The fitting procedure is also an iterative process where already fitted parameters are further refined towards the same measurement results due to a coupling between model parameters, where calculated data from a subsequent fitting indicates that a parameter should be refitted. This may appear contradictive, but it is necessary since the effects of variations in different parameters are coupled. As an example, the parameters for the collector current need to be refitted after a variation in the thermal resistance which defines the temperature elevation of the junction caused by the internal power dissipation.

The practical process of performing a fitting involves the optimisation feature of MDS. A parameter that will be fitted is entered as a nominal value with boundaries. These can be defined in the following ways:

relative:	x */ y	x/y < x < x*y
absolute	x +- y	x-y < x < x+y
definite:	a<x<b	

The optimiser within MDS thus varies the parameter in order to make a given error function, dependent of e.g. a small signal RF simulation, as small as possible. Several parameters can be fitted during one optimisation, but the number of necessary simulations increase drastically with increasing number of parameters. With many degrees of freedom, the results can also become odd since the optimiser treats all parameters as equally important in the sense that only the given boundaries are of importance. It is thus necessary to only optimise parameters whose impact on a certain error function is directly related. If certain parameters are only weakly affecting the error function, a set of these parameters where all are on their respective boundaries, can be found to give a slightly better result than not changing the parameters at all. It is questionable whether that result is a physically better solution.

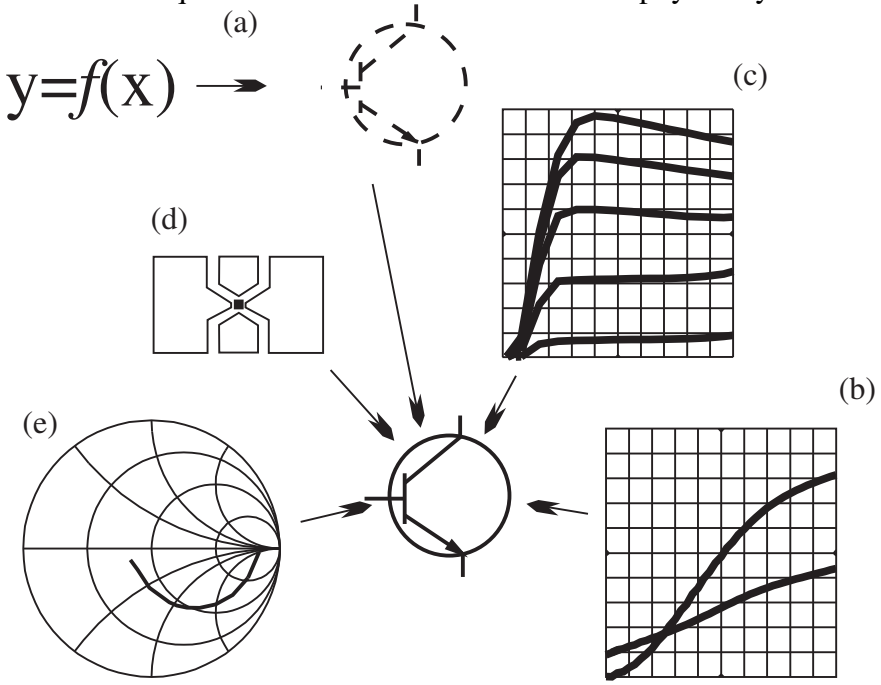

Fig. 20 A schematic picture of the fitting procedure. (a) parameters with calculated values for the transistor are used for an initial device description. (b) using Gummel measurements, (c) IV-curves, (d) measurements of test structures and finally (e) measured S-parameters, a closer fit to a real device is possible.

FITTING TOWARDS THE GUMMEL PLOT

The first step in the procedure is to find a good characterisation of the currents in the device. These give valuable information of the intrinsic device geometries, e.g., emitter area and layer structure. The effects of varying the parameters are somewhat interconnected and it is thus necessary to put an order in where parameters with the strongest impact are primarily varied for the coarse adjustment. Some parameters are also having tighter limits (e.g. layer thicknesses who are grown using MBE which gives accurate dimensions) which makes their optimisation boundaries small. This means that their total impact on the fitting is small. As a conclusion, both the impact from a parameter and the range in which it is allowed to vary needs to be considered for finding the relative importance between the different parameters.

In addition, the base current is the only component which is used for extracting artificial data, unique for each transistor, i.e., the leakage currents between base and emitter.

The measurements for the fitting is preferably performed at different temperatures to see the thermal effects which come out strongly due to the exponential effects (see eq. 40 and eq. 5) as can be seen in Fig. 13.

The gummel plot can be divided into three different regions as discussed earlier and the different parameters are fitted to measurements in the region where their impact on the currents are the biggest. Due to the coupling between the different currents, the fitting procedure for the parameters may need to be run in parallel for parameters affecting the collector current and parameters affecting the base current in the same region respectively, see below for extraction of ρ_E.

The fitting procedure is usually performed for the parameters in the following order:

Collector current: A_E, N_B, W_B, n_F, ρ_E.

Base current: N_E, artificial currents.

During the measurements, leakage currents that are possibly outside the actual transistor can occur which can be seen as the almost voltage independent part of the current at low V_{BE} (see Fig. 12). The origin of these currents can be in the bleed-resistors of the bias-T's, surface currents between the different contacting pads of the transistor or on the actual transistor, or from generation-recombination (GR) processes in the SCR of the base-collector junction. These currents can have an impact on the result when performing fitting of parameters at current levels where these parasitic currents can not be considered negligible. The resulting error in the fitting of parameters will then affect the circuit behaviour at higher currents, i.e., at normal bias conditions. For accuracy reasons in the fitting it can thus be worthwhile to account for the parasitic currents as constant current generators in the base-emitter and base-collector junction although they can be of negligible interest from a circuit point of view and can be possibly discarded in the final model, depending on the size of the current. The bleed-resistors of the bias-T's are also included as external elements outside the transistor, but their impact is small since the parasitic currents often are much bigger than what would be expected from the bleed resistors.

Since the coupling between the currents is fairly small in region I (see Fig. 12), A_E, N_B, W_B and n_F can there be fitted independently of the value of the base current. It is however necessary to assure that ρ_E is small since it otherwise can limit the collector current and thus affect the fitting. The three first parameters are varied to fit the absolute value of the collector current to the measured data whereas the fourth (n_F) is used for finding the correct slope. The emitter area and ideality factor are independently varied as parameters whereas base width and doping are more closely related from fabricational reasons. To prevent the usually high base doping from diffusing into the emitter and collector, a low doped barrier (so called spacers or set-back layers) are grown on each side of the base. These occupy together approximately 10% to 30% of the grown base-width and they will be doped during later fabrication steps because of the necessary heat treatment that the device has to undertake. For this reason the electrical base-width can actually increase upto 40%. This effect must however then also include that the total doping goes down with an equal factor, i.e., the Gummel number remains constant. An initial assumption has been that all of the set-back layers have been doped by outdiffusion since the fabrication process is optimised for the electrical junction (doping level) and the metallurgical junction (interface of Silicon and Silicon Germanium alloy) to coincide.
Due to the exponential dependence of n_F and that the fitting is performed at a voltage where the value of the exponential function varies strongly with n_F, this parameter will have a strong impact on the absolute value of the current. It is therefore important to fit the parameters (A_E, N_B, W_B and n_F) affecting the collector current iteratively. In the purely exponential region (the collector current above the beginning of region II, see Fig. 12), it suffices to use three evenly spread points for the simulation part of the optimisation.

Table 2
Initial model parameters taken mainly from fabricational data.
Values that have been estimated are marked with a "*".

W_E [cm]	$.070*10^{-4}$	W_B [cm]	$.030*10^{-4}$	W_C [cm]	$.300*10^{-4}$
N_E [cm^{-3}]	$2*10^{18}$	N_B [cm^{-3}]	$1*10^{20}$	N_C [cm^{-3}]	$5*10^{16}$
A_E [cm^2]	$20*10^{-8}$	x_{Ge}	0.30	A_C [cm^2]	$40*10^{-8}$
$^*\rho_E$ [Ω /cm^2]	$5.0*10^{-6}$	$^*\rho_B$ [Ω /cm^2]	$5.0*10^{-6}$		
W_F [cm]	$20*10^{-4}$				
$^*L_F$ [cm]	$3*10^{-4}$	$^*L_B$ [cm]	$2.0*10^{-4}$	$^*R_C$ [Ω]	5
J_{E1} [A/cm^2]	0	K_{Ie}	1	$I_{BCextleak0}$ [A]	0
n_{E1}	1	K_{Ih}	1	$n_{BCextleak}$	1
$^*V_{Offset1}$ [V]	0.55	n_F	1.0		
$^*V_{therm1}$ [V]	0.20	n_R	1.0		

Using the collector current at the highest values of V_{BE} (see Fig. 12), the emitter resistivity (ρ_E), is adjusted. The value can be found fairly easily at high collector

currents because of the strongly limiting effect it has. Care must be taken to also have a correct base current in this region since it is the sum of these currents that cause the voltage drop over the emitter resistance and thus limits the voltage drop of the base-emitter junction. An iterative process where the parameters for the different currents are adjusted consecutively works well.
Applying the above discussion on a typical transistor (in this case a B3603_120Z), a fitting of the model parameters towards the Gummel plot has been done. The original data for the model parameters can be seen in Table 2 and the resulting Gummel plot is shown in Fig. 21.

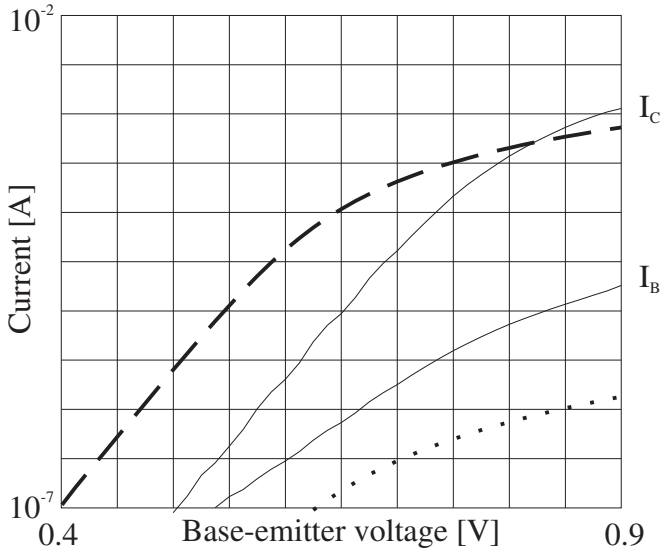

Fig. 21 Gummel plot with calculated and measured data for the modelled transistor. The model parameters are taken from fabricational data and from estimations where immediate values are not available. Dashed lines correspond to calculated data and solid lines correspond to measured data.

The collector current is strongly overestimated compared to the measured data (see Fig. 21) and the base current exhibits a more ideal behaviour compared to the measured data. Concentrating on finding a correct collector current, the emitter area (A_E) is adjusted to account for the apparent overetch to $10*10^{-8}cm^2$ which gives a decrease in current by a factor of 2, see Fig. 22.
A smaller A_E is unlikely and thus the Gummel number of the base is adjusted. With the assumption that the base doping (N_B) may vary with a factor of two, N_B is thus set to $2*10^{20}$ cm^{-3}. At these high doping levels, the classical expression for apparent band-gap narrowing [31] overestimates the actual value with a too high calculated injection as result [19]. For this reason I_{Ee} need to be limited by a factor (K_{IEe}). From Fig. 4 in [19], a value of 0.3 is chosen. The resulting gummel plot can be seen in Fig. 23.

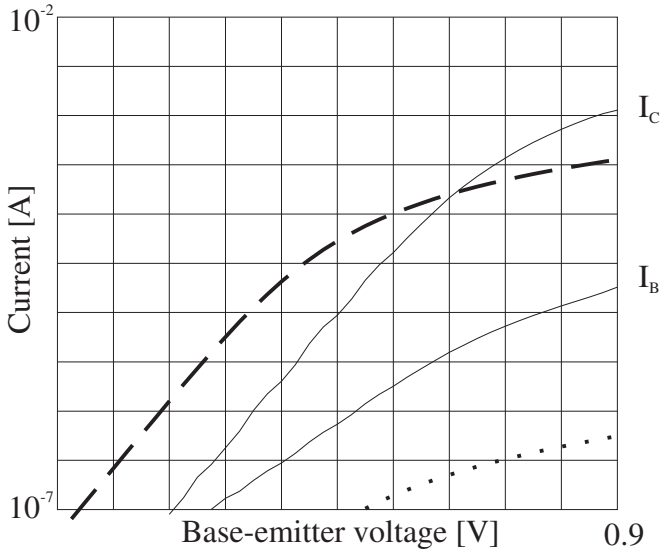

Fig. 22 Gummel plot where the parameter A_E has been decreased to $10*10^{-8}$ cm^2. The lines are defined as in Fig. 21.

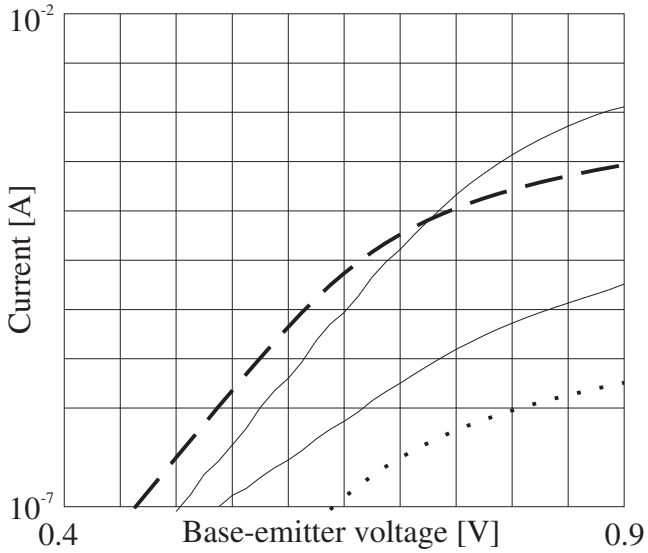

Fig. 23 Gummel plot where N_B has been set to $2*10^{20}$ cm^{-3} and K_{IEe} has been set to 0.3. The lines are defined as in Fig. 21.

The collector current is still overestimated, but the strong limitation at high V_{BE} in comparison with the measured data also indicates that the contact resistivity of the emitter contact is too high. This will not affect the collector current at lower V_{BE}, but the ideal region of the collector current (corresponding to the collector current above region II in Fig. 12) will be smaller than necessary and thus a shorter range in V_{BE} can be utilised for the optimisation of the ideality factor (n_F). In order to prepare for the subsequent optimisation for n_F, ρ_{Econt} is changed from the estimated $5*10^{-6}$ Ωcm^2 to $5*10^{-7}$ Ωcm^2 which should be a lower limit. This value is possibly too low for a real contact [13], indicating that the contact resistance for the moment is negligible. The calculated collector current in Fig. 24 is higher than the measured which could be

interpreted as a too low contact resistance is chosen. Subsequent fitting will however show that the assumed value works well.

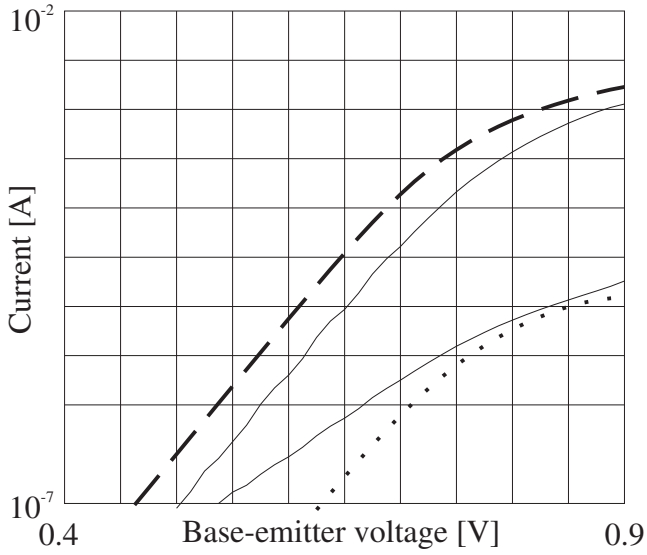

Fig. 24 Gummel plot where ρ_{Econt} has been set to $5*10^{-7}$ Ωcm^2. The lines are defined as in Fig. 21.

To find a collector current that corresponds well with measured data, n_F and K_{IEe} are adjusted. It is unlikely that only an adjustment of n_F would lead to a successful match between calculated and measured collector current as an offset still exists, see Fig. 24. That the offset can be ascribed only to an overestimation of the bandgap contraction when K_{IEe} already is set to 0.3 is not clear. However, other effects that would block an injection, e.g., a small spike in the conduction band caused by a slight offset between the electrical and metallurgical junctions, can here empirically be included. Altering K_{IEe} from 0.3 to 0.2 and setting n_F to 1.036 gives a calculated collector current which well corresponds to the measured, see Fig. 25.

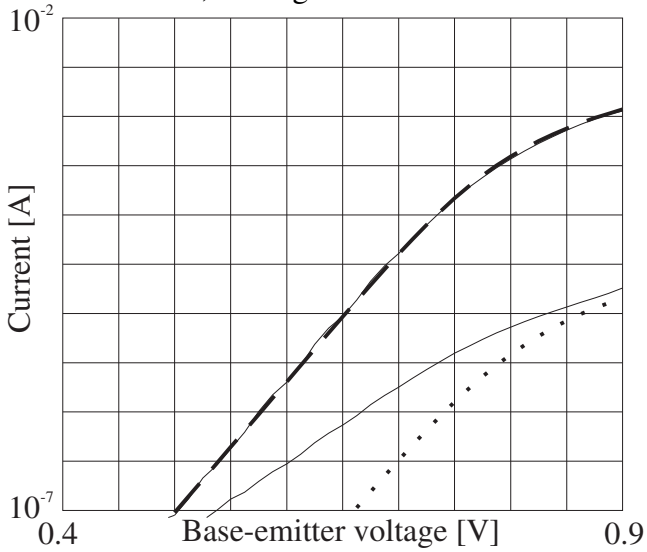

Fig. 25 Gummel plot where K_{IEe} is set to 0.2 and n_F is set to 1.036. The lines are defined as in Fig. 21.

To get a better match between calculated and measured base-current, an artificial current source needs to be introduced as discussed earlier. As can be seen in Fig. 25, the calculated base-current is very close to the measured one at high V_{BE} which means that an added current source would risk to create a too big calculated base-current. However, it is necessary to have a such a current source at low V_{BE} in order to model the base-current correctly. Thus, the ideal part of the base-current is decreased by a factor K_{IEh}. With K_{IEh}=0.5, J_{E10}=2.663 A/cm^2, n_{10}=1.814 and V_{T10}=0.20, a good match between calculated and measured data is acquired, see Fig. 26. In order to verify the validity of the match, also collector current versus collector-emitter voltage is calculated, see Fig. 26.

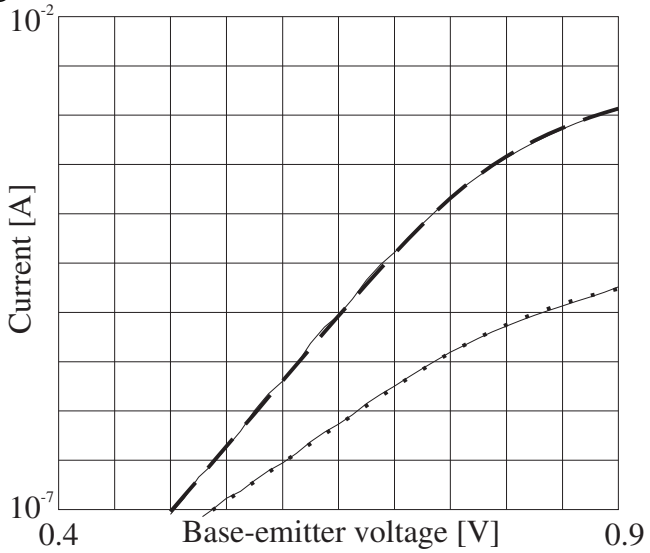

Fig. 26 Gummel plot where K_{IEh}=0.5, J_{E10}=2.663 A/cm^2, n_{10}=1.814 and V_{T10}=0.20. The lines are defined as in Fig. 21.

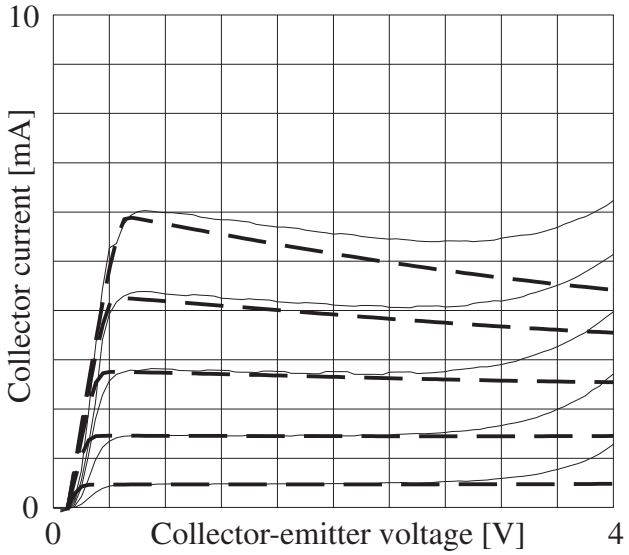

Fig. 27 Collector current versus collector-emitter voltage for base currents from 20 µA to 100 µA in steps of 20 µA. Dashed lines correspond to calculated data and solid lines correspond to measured data.

With the good match between calculated and measured data for both the collector and base current, a fine tuning of ρ_{Econt} can be made which gives a result of $\rho_{Econt}=5.31*10^{-7}\ \Omega cm^2$. Such a small deviation from the previously assumed one does not give a distinguishable change in the Gummel plot.

FITTING TOWARDS PLOT OF COLLECTOR CURRENT VERSUS COLLECTOR-EMITTER VOLTAGE

Following the gummel plot, the DC parameters are fitted against the IV-curve. Using the slope of a high collector current at a collector-emitter voltage around 1.5 V (beyond the saturation region of the transistor), the thermal resistance is adjusted. Due to the thermal dependencies for the base and collector current in an HBT, this area will exhibit a negative differential resistance. The base current increases quicker with temperature than the collector current, or conversely, for a constant base current, the collector current decreases with increasing temperature. When the slope changes in the IV-curve, also the difference between measured and calculated data increases in the Gummel plot and further fitting using the gummel plot can become necessary. Although the internal power dissipation during the gummel measurement is small because of the low base-collector voltage, the thermal effect can be noticeable at high currents and must therefore be accounted for.

A fine tuning of the base and collector currents in the active bias region can also be done using the IV-curve. Since the gummel plot uses logarithmic values, the dynamic range is big, but accuracy can become difficult, especially in the narrow range of V_{BE} which defines the typical active region. When adjusting parameters towards the IV-curve, accuracy can be increased and more importantly, the adjustments are made towards the region in which the device later will operate. Care must then also be taken that the fit against the gummel curve is maintained. When altering parameters in the model for a current to better fit in the IV-curve, the gummel plot will change. Although there is a seemingly good fit in the IV-curve, both currents in the gummel plot can be offset from the measured value. As long as the interdependence between I_B and I_C (which defines β) is maintained, the calculated IV-curve will correspond to measured values and not indicate the discrepancy between measurement and calculated values in the gummel plot. It is thus important to be very restrictive in the fitting of parameters towards the IV-curve.

An effect of smaller significance is the slightly varying offset in V_{CE} for the different curves of the collector current. This can be well modelled with a diode between the base and collector pad and the effect is likely to be caused by leakage currents on the surface of the collector. The current generator inside the SDD is not appropriate for handling this current since the surface of the collector exists outside the base-lead resistances and the extrinsic base-collector junction (see Fig. 6 and 9). Additionally, the voltage drop occurring over the collector-lead resistance (R_C in Fig. 10) need not affect this leakage current. By adjusting the saturation current, the offset voltage can be changed, a high saturation current corresponds to a high offset voltage. The

sharpness in the transition from saturation region to ohmic region is controlled by the ideality factor of the diode. A value close to unity corresponds to a sharp transition and a high value corresponds to a slow transition.

The collector lead resistance (R_C) is adjusted towards the slope of the collector current at low collector-emitter voltage and high base current, i.e., in the saturation region.

Continuing the fitting procedure of the studied device, it can be seen in Fig. 27 that the slope of the calculated collector current is steeper than that of the measured one at high currents. This indicates a too high thermal resistance (R_{th}) of the simulated device. Adjusting R_{th} to 1200 K/W creates a slope which corresponds well to measured data, see Fig. 28. Due to this change however, it is necessary to verify that the Gummel plot has not changed so that the measured and calculated data still correspond well.

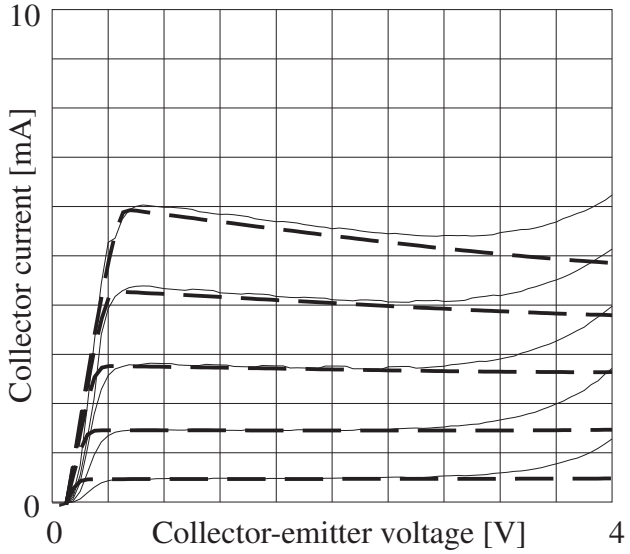

Fig. 28 Collector current versus collector-emitter voltage for base currents from 20 µA to 100 µA in steps of 20 µA. The thermal resistance (R_{th}) is set to 1200 K/W. The lines are defined as in Fig. 27.

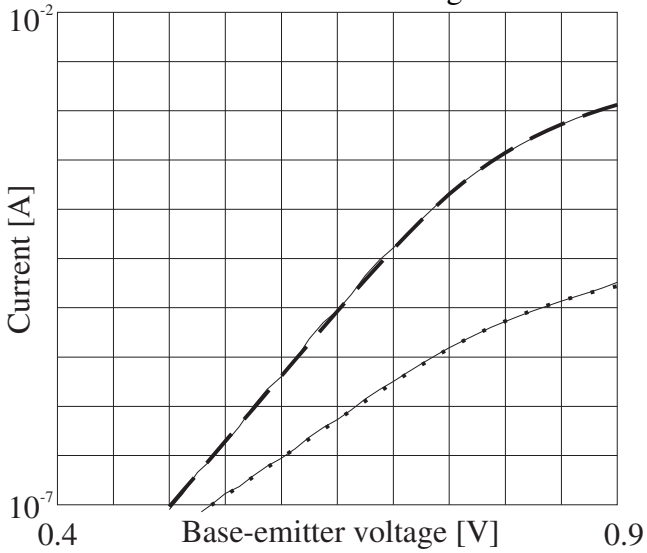

Fig. 29 Gummel plot where R_{th}=1200K/W. The lines are defined as in Fig. 21.

As can be seen in Fig. 29, the variation in base and collector current is very small and the model can retain its parameter values.
The calculated collector current exhibits no breakdown effects, occurring as quickly increasing collector current with increasing collector-emitter voltage in the ohmic region, which the measured data does as can be seen in Fig. 28. A breakdown effect is however included in the model, but this will for the current doping appear at higher collector-emitter voltage. By adjusting the calculated breakdown voltage by a factor of 0.5, a collector current that exhibits characteristics similar to the measured can be achieved, see Fig. 30. The strong decrease of the breakdown voltage indicates that the current modelling does not correctly account for the physical breakdown processes that occur in the device. The empirical approach of lowering the breakdown voltage can however work sufficiently well in simulations since the device should not be operated in the breakdown region as this is likely to destroy the device.

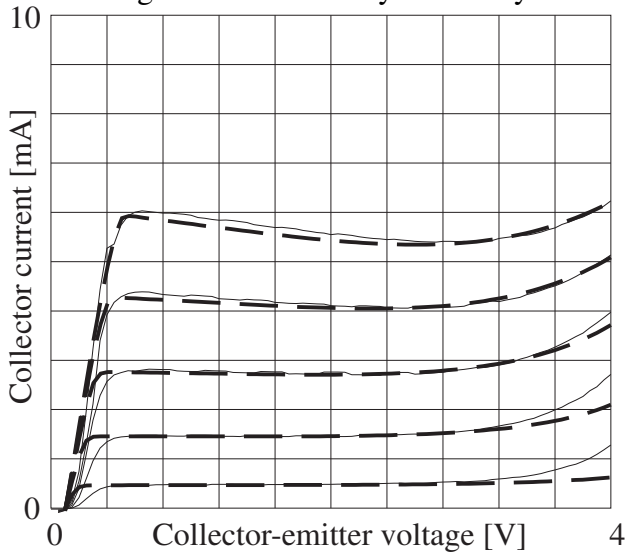

Fig. 30 Collector current versus collector-emitter voltage for base currents from 20 µA to 100 µA in steps of 20 µA. The analytically calculated collector breakdown voltage has been multiplied by a factor of 0.5. The lines are defined as in Fig. 27.

The last step of the fitting for the DC-parameters is to adjust the offset voltage which can be seen as the collector-emitter voltage where the transistor starts conducting a collector current. With $I_{BCextleak0}=0.8*10^{-8}$A and $n_{BCextleak}=2.5$ the calculated and simulated values for the collector current in the saturated region agree well and there is not a need to adjust the collector-lead resistance from the initially estimated one, see Fig. 31.

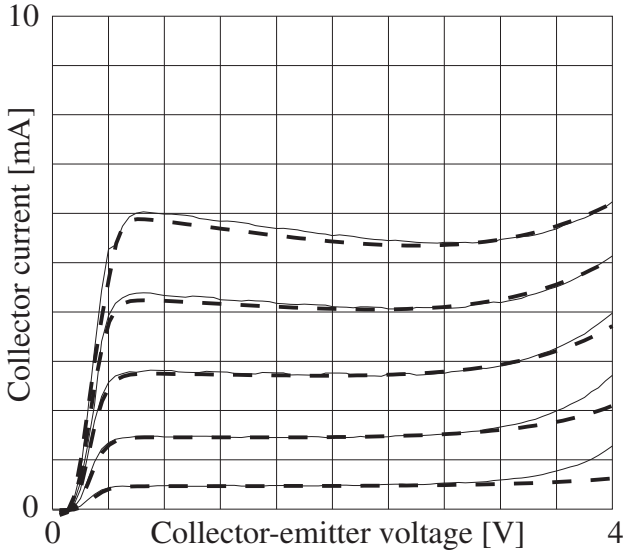

Fig. 31 Collector current versus collector-emitter voltage for base currents from 20 μA to 100 μA in steps of 20 μA. The extrinsic base-collector leakage current has been added as $I_{BCextleak0}=0.8*10^{-8}$A and $n_{BCextleak}=2.5$. The lines are defined as in Fig. 27.

FITTING TOWARDS SCATTERING PARAMETERS

The final step for the fitting is to adjust values towards measured S-parameters. The difficulty or what should be stressed here is the importance of using the measured data for comparison efficiently. As in the case of steady state, characteristics can be presented in different ways. For input and output matching the Smith chart suffices as it spans the whole impedance range with high resolution for the impedances of interest (assuming a 50 Ω system). The transmission parameters can similarly be presented well with polar plots. The benefit with this representation is that both magnitude and phase can be compared simultaneously. The limitation, however is that the frequency dependence will be slightly obscured and the risk of having a seemingly good correspondence between a calculated and a measured data point, although their frequencies do not match should not be neglected. For this reason it is also important to look at a graph where data is plotted directly versus frequency. These graphs do not necessarily show a very good accordance between calculated and measured data, although a polar plot has done so and a further tuning towards this kind of plot has to be done. This is especially true at higher frequencies. Another kind of presentation that can be of big importance is the plot of h_{21} and unilateral gain (MUG) to find f_t and f_{max} who both are very important parameters for the device as they define an upper limit for where efficient operation in circuits can be accomplished. A matching between calculated and measured data for one bias point is here reasonably easy to accomplish and there has been several methods presented for doing this [32][33][34]. What is important however is to have the same set of model parameters making the model match calculated and measured data for different bias points. By acquiring this set of model parameters, large signal modelling can be

facilitated to a certain extent. Some large signal effects require a more complete description than the one used in this model. One example of this is the drift delay through the collector SCR at current variations high enough to vary the depletion width during a constant voltage drop. This should however not be confused with the static collector bias current which causes a static SCR expansion as discussed earlier. The very high powers where these effects cannot be modelled sufficiently with the present model seem not to occur at normal modes of non-linear operations. Modelling of large signal effects with the model has so far given adequate results [22] as discussed earlier.

Due to the complexity and the coupling between the different model parameters there is no straight procedure in which parameters are found in a consecutive order. This section will instead present examples of how a variation in a parameter affects the calculated S-parameter and how this can be used to get a better match between calculated and measured data. From the previous fitting for DC-parameters however, the calculated S_{21} should compare reasonably well with measured data for different bias points since S_{21} is closely related to β.

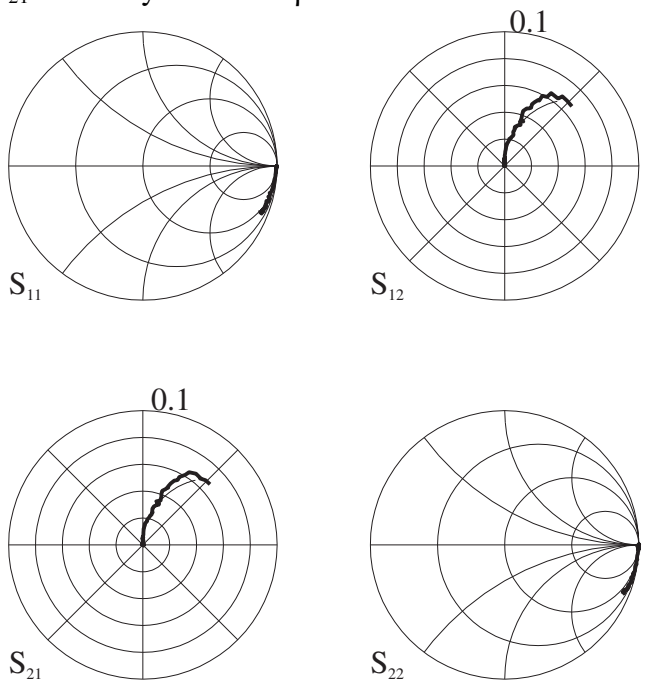

Fig. 32 Measured and calculated S-parameters for a test structure near the studied device. The frequency is from 200 MHz to 50 GHz. Thick lines denotes measured data, thin lines denote calculated data. For S_{11} and S_{22}, measured and calculated data overlap.

The first step of fitting considers the embedding shell which involves measurements of test structures to find a good electrical description of how the contacting pads behave. Ideally, components with an open and shorted termination and a through-line should be measured to find information about cross-coupling, inductances, resistances and losses. An example of a measured data for a test structure with open termination situated near the fitted device can be seen in Fig. 32 where also calculated data is

shown. The corresponding parameters for the components can be seen in Table 3. It can be noticed there that the resistances corresponding to the losses (R_{BEloss}, R_{CEloss}, R_{Eloss} and R_{Closs} respectively) have negligible effect which speaks for that this device has low losses outside the actual transistor. This corresponds well to the measurements which show a reflection coefficient of almost unity, see Fig. 32. The length of the two transmission lines agrees well with what can be expected. As no through line or shorted structure was available, the values of the inductances and lead resistances are estimated values found for similar devices.

Table 3
Data for parameters of the embedding shell to fit the measured open test structure.

Parameter	Value	Parameter	Value	Parameter	Value
L_{Bpad}	9.5 pH	L_{Cpad}	4.4 pH	L_{Epad}	11.0 pH
C_{BE}	2.17 fF	C_{BC}	2.25 fF	C_{CE}	1.00 fF
R_{BE}	2493 Ω	R_{BC}	428 Ω	R_{CE}	4227 Ω
R_{Bpad}	0.05 Ω	R_{Cpad}	0.05 Ω	R_{Epad}	0.05 Ω
R_{Bprobe}	0.05 Ω	R_{Cprobe}	0.05 Ω	R_{Eprobe}	0.05 Ω
R_{BEloss}	50 kΩ	R_{CEloss}	50 kΩ	L_{TLB}	63 μm
R_{Eloss}	0.05 Ω	R_{Closs}	0.05 Ω	L_{TLB}	66 μm

Studying the actual device, the calculated transmission parameter S_{21} should compare well with the measured one. It is however important to study this parameter closely at high frequencies and here the polar plot might give ambiguous results. Due to the comparably high frequency even a very short transmission line, e.g., the contacting pads, will cause a phase shift as discussed above. The difficulty is to define where the transmission line begins since the probes that are used at the measurements will contact the pads at slightly different points. Thus a certain amount of inaccuracy is here probably unavoidable unless a very sophisticated measurement method can be employed. For this reason a slight discrepancy in phase below 15^{o}, corresponding to a CPWTL of 50 μm at 50 GHz, between calculated and measured data should be accepted (for a contact pad where probes are separated approx. 100 to 200 μm) and emphasis should be put on studying the magnitude. Due to the impact on parameters like f_t and f_{max}, several parameters affecting the high frequency performance need to have an adequate fit in order to be able to estimate the device performance correctly.

For the studied device, S-parameters have been calculated for different bias points which covers bias for normal operation, see Fig. 33, 34 and 35. The calculated data agrees well with measured data as can be seen in the figures and although a further tuning may result in a better match, it would also mean deviations from the initial assumptions of device parameters. As there is no clear partition between the different parameters in how they affect the RF-performance, a variation in parameters may improve the matching although the improvement is based on an erroneous

adjustment. However, where the agreement between calculated and measured data is worse than what has been found for the studied device, adjustments can be made where the impact of a single parameter clearly can improve the match for different bias points and it is thus more probable that the parameter indeed should be altered.
To give an impression on how different parameters affect the RF-performance, different parameters have been varied, one at a time, around its nominal value by the factors of 0.1, 1 (nominal value) and 10. With these parameter settings, S-parameters have been calculated and are shown in appendix 2.

Table 4
Parameter values for the fitted model.

W_E	[cm]	$.070*10^{-4}$	W_B	[cm]	$.030*10^{-4}$	W_C	[cm]	$.300*10^{-4}$
N_E	[cm^{-3}]	$2*10^{18}$	N_B	[cm^{-3}]	$2*10^{20}$	N_C	[cm^{-3}]	$5*10^{16}$
A_E	[cm^2]	$10*10^{-8}$	x_{Ge}		0.30	A_C	[cm^2]	$40*10^{-8}$
ρ_E	[Ω /cm^2]	$5.31*10^{-6}$	ρ_B	[Ω /cm^2]	$5.0*10^{-6}$			
W_F	[cm]	$20*10^{-4}$						
L_F	[cm]	$3*10^{-4}$	L_B	[cm]	$1.0*10^{-4}$	R_C	[Ω]	5
J_{E1}	[A/cm^2]	2.91	T_0	[K]	293	$I_{BCextleak0}$		$0.8*10^{-8}$
n_{E1}		1.845	K_{Ie}		0.2	$n_{BCextleak}$		2.5
$V_{Offset1}$	[V]	0.55	K_{Ih}		0.5			
V_{therm1}	[V]	0.20	n_F		1.036			
			n_R		1.000			
			τ_F	[s]	$0.1*10^{-12}$			

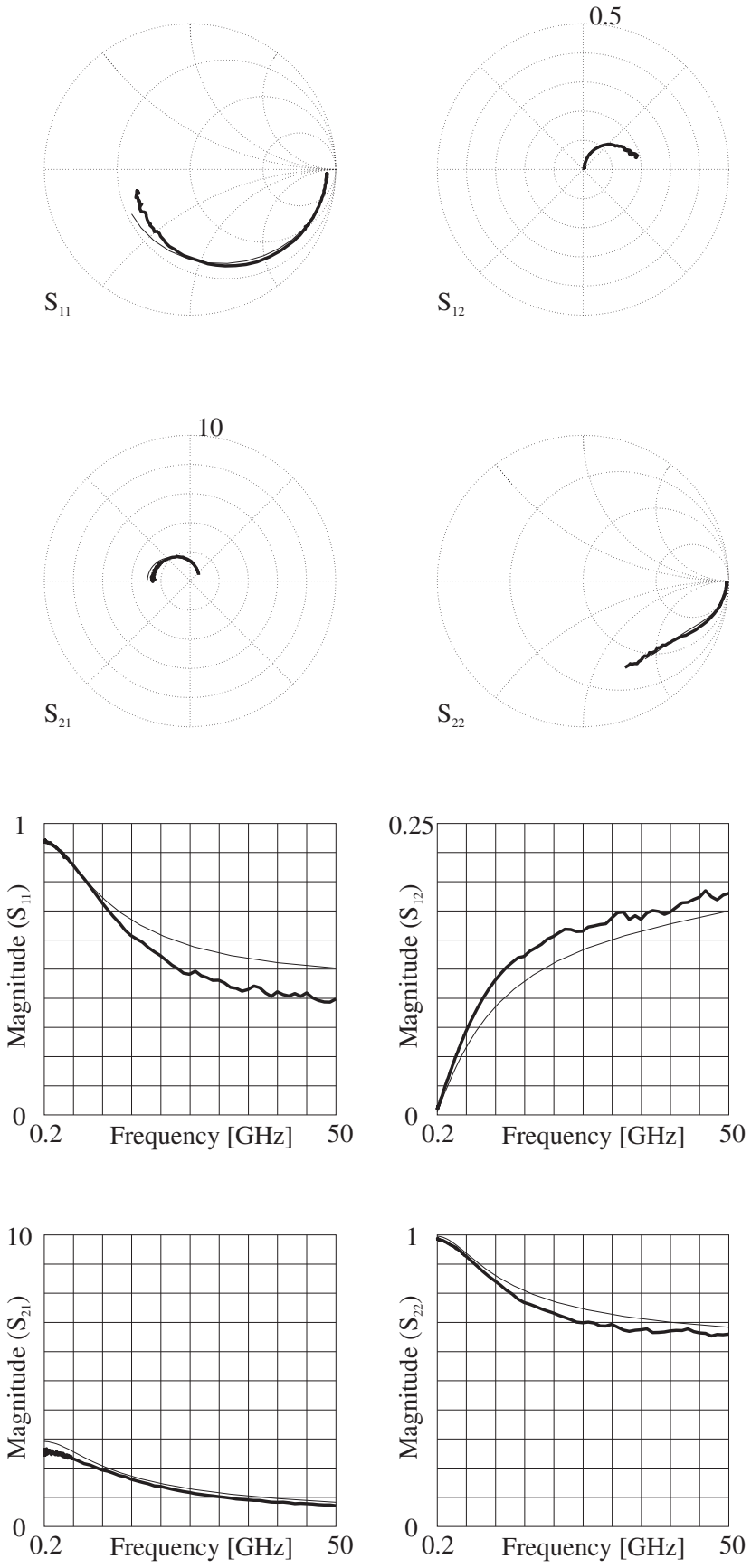

Fig. 33 Measured and calculated S-parameters at I_C=1 mA, V_{CE}=2V. Frequency is from 200 MHz to 50 GHz, all curves in polar plots move clockwise with increasing frequency.

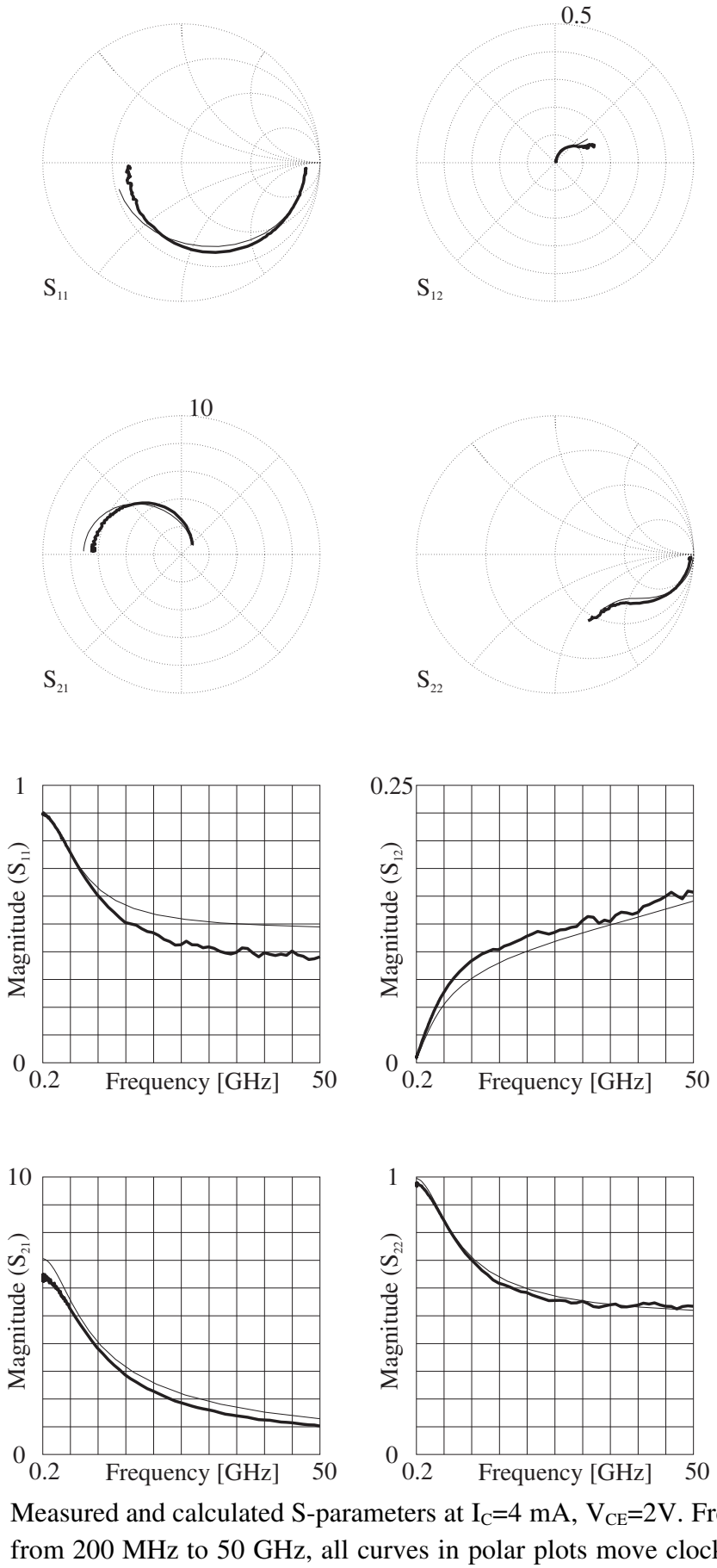

Fig. 34 Measured and calculated S-parameters at I_C=4 mA, V_{CE}=2V. Frequency is from 200 MHz to 50 GHz, all curves in polar plots move clockwise with increasing frequency.

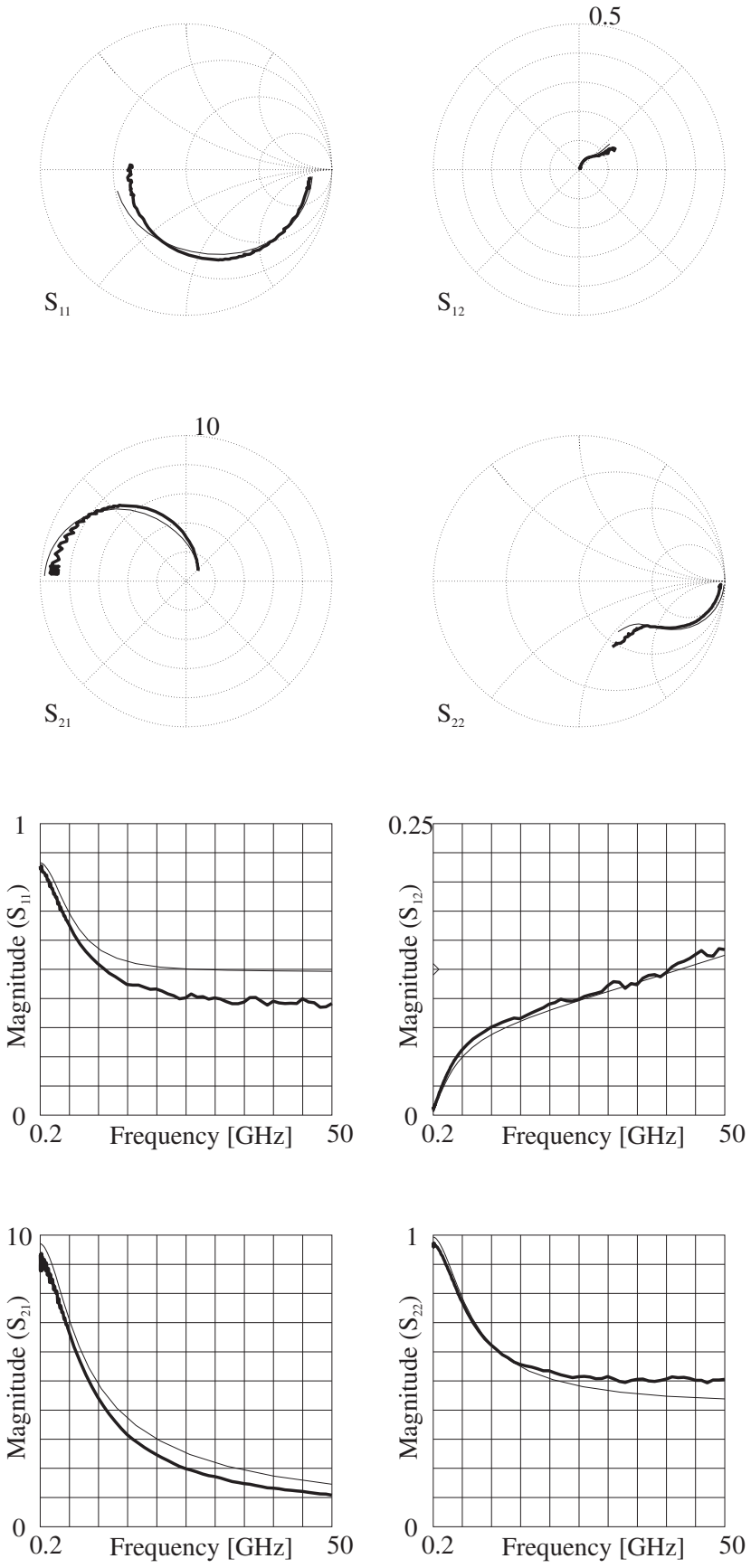

Fig. 35 Measured and calculated S-parameters at I_C=10 mA, V_{CE}=2V. Frequency is from 200 MHz to 50 GHz, all curves in polar plots move clockwise with increasing frequency.

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APPENDIX 1:
NOMENCLATURE

BJT	Bipolar Junction Transistor
DHBT	Double Heterojunction Bipolar Transistor
FEM	Finite Element Method
HBT	Heterojunction Bipolar Transistor
MDS	Microwave Design System
SCR	Space Charge Region
SDD	Symbolically Defined Device
SEM	Scanning Electron Microscopy
SHBT	Single Heterojunction Bipolar Transistor
SIMS	Secondary Ion Mass Spectroscopy

Variables:

$_I_n$	node variables related to the SDD
$_V_n$	node variables related to the SDD
A_B	base contact area [cm^2]
A_C	total area of base-collector junction [cm^2]
A_E	area of base-emitter junction [cm^2]
A_{Econt}	area of emitter contact [cm^2]
α_F	forward base transport factor
α_R	reverse base transport factor
β	DC current gain
β_{HBT}	DC current gain for HBT
C_{j0}	junction capacitance at zero bias [F]
C_{BC}	capacitance in intrinsic base-collector junction [F]
C_{BCext}	junction capacitance in extrinsic base-collector junction [F]
$C_{BCext00}$	junction capacitance in extrinsic base-collector junction at zero bias and ambient temperature [F]
C_{BCpad}	capacitance between base and collector pad [F]
C_{BCtot}	total base-collector capacitance [F]
C_{BE}	capacitance in intrinsic base-emitter junction [F]
C_{BEpad}	capacitance between base and emitter pad [F]
C_{Bshunt}	capacitance shunting the base contact resistance [F]
C_{CEpad}	capacitance between collector and emitter pad [F]
$C_{DCblock}$	capacitance for blocking of DC [F]
C_j	junction capacitance [F]
$C_{RFshunt}$	capacitance for shunting RF-signals [F]
X_B	electron affinity in base [V]
X_C	electron affinity in collector [V]
X_E	electron affinity in emitter [V]
D_{eB}	diffusion constant for electrons in base [cm^2s^{-1}]

D_{hC}	diffusion constant for holes in collector [cm^2s^{-1}]
D_{hE}	diffusion constant for holes in emitter [cm^2s^{-1}]
ΔV_B	potential difference between fermilevel and valence band in base [V]
ΔV_C	potential difference between fermilevel and conduction band in collector [V]
ΔV_E	potential difference between fermilevel and conduction band in emitter [V]
ε	dielectric constant [As/Vcm]
ε_0	dielectric constant in free space $8.854*10^{-14}$ [As/Vcm]
ε_B	dielectric constant in base [As/Vcm]
ε_C	dielectric constant in collector [As/Vcm]
ε_E	dielectric constant in emitter [As/Vcm]
E_1	constant for calculating doping induced bandgap contraction [eV]
E_{Cbreak}	electric breakdown field in collector [V/cm]
ΔE_g	difference in bandgap between two different materials [eV]
ΔE_{gX}	bandgap contraction due to doping [eV]
E_g	bandgap energy difference [eV]
E_{gB}	bandgap in base [eV]
E_{gB0}	bandgap in base at fixed temperature [eV]
E_{gC}	bandgap in collector [eV]
E_{gC0}	bandgap in collector at fixed temperature [eV]
E_{gE}	bandgap in emitter [eV]
E_{gE0}	bandgap in emitter at fixed temperature [eV]
f_t	frequency where current gain reaches unity [Hz]
f_{max}	maximum frequency of oscillation [Hz]
Φ_B	potential difference from fermilevel to vacuum level in base [V]
Φ_C	potential difference from fermilevel to vacuum level in collector [V]
Φ_E	potential difference from fermilevel to vacuum level in emitter [V]
γ	constant for calculating doping and temperature dependent electron mobility in Silicon
g_{BC}	DC transconductance
η_B	constant for calculating base diffusion delay
i_B	total base current [A]
I_B	DC base current [A]
i_{BCext}	diode current in extrinsic base-collector junction [A]
$I_{BCext00}$	saturation current for current in external base-collector junction diode [A]
$i_{BCextleak}$	leakage current occurring between base and collector [A]
$I_{BCextleak}$	Saturation current for external leakage current between base and collector [A]
i_C	total collector current [A]
I_C	DC collector current [A]
i_{Ce}	electron injection current into base from collector [A]
I_{Ce0}	electron saturation current in base-collector diode [A]
i_{Ch}	hole injection current into collector from base [A]
I_{Ch0}	hole saturation current in base-collector diode [A]
I_E	DC emitter current [A]

i_{Ee}	electron injection current into base from emitter [A]
I_{Ee0}	electron saturation current in base-emitter diode [A]
i_{Eh}	hole injection current into emitter from base [A]
I_{Eh0}	hole saturation current in base-emitter diode [A]
I_{LBC}	leakage currents occurring in the intrinsic base-collector junction [A]
I_{LBE}	leakage currents occurring in the intrinsic base-emitter junction [A]
I_m	current components for the non-ideal current in the intrinsic transistor [A]
φ	factor introduced in the frequency domain to account for delays [rad]
j	imaginary constant
J_{0e}	electron saturation current density [A/cm^2]
J_{Em}	emitter leakage saturation current density [A/cm^2]
K_{IEe}	constant to account for a reduction of electron injection current into the base from the emitter
K_{IEh}	constant to account for a reduction of hole injection current into the emitter from the base
K_{ICe}	constant to account for a reduction of electron injection current into the base from the collector
K_{ICh}	constant to account for a reduction of hole injection current into the collector from the base
k_B	Boltzmanns constant = $1.381*10^{-23}$ [Js/K]
L_B	effective length between base contact metallisation and intrinsic base [cm]
L_{Bpad}	inductance in base pad [H]
L_{Cpad}	inductance in collector pad [H]
L_{Epad}	inductance in emitter pad [H]
$L_{DCshunt}$	inductance for shunting of DC [H]
L_F	emitter length in the direction of the base current flow [cm]
M_C	multiplication factor for collector avalanche breakdown
μ_{eC}	electron mobility in collector [cm^{2}V^{-1}s^{-1}]
μ_{eC0}	electron mobility in collector at fixed ambient temperature [cm^{2}V^{-1}s^{-1}]
μ_{eE}	electron mobility in emitter [cm^{2}V^{-1}s^{-1}]
μ_{hB}	hole mobility in base [cm^{2}V^{-1}s^{-1}]
$\mu_{hBtrans}$	transverse (parallel to the surface) hole mobility in strained base [cm^{2}V^{-1}s^{-1}]
μ_{n0}	constant for calculating doping and temperature dependent electron mobility in Silicon [cm^{2}V^{-1}s^{-1}]
μ_{n1}	constant for calculating doping and temperature dependent electron mobility in Silicon [cm^{2}V^{-1}s^{-1}]
$m_{hhSiGestrain}$	mass of heavy holes in strained SiGe [kg]
$m_{lhSiGestrain}$	mass of light holes in strained SiGe [kg]
N_0	constant for calculation of doping induced bandgap contraction [cm^{-3}]
N_B	doping concentration in base [cm^{-3}]
N_C	doping concentration in collector [cm^{-3}]
N_E	doping concentration in emitter [cm^{-3}]
$n_{BCextleak}$	ideality constant for the leakage current occurring between base and collector

N_{cond}	density of states in the conduction band [cm^{-3}]
$N_{cSiGeLStrain}$	density of states in the L-valley of the conduction band of strained SiGe [cm^{-3}]
$N_{cSiGeStrain}$	total density of states in the conduction band of strained SiGe [cm^{-3}]
$N_{cSiGeXStrain}$	density of states in the X-valley of the conduction band of strained SiGe [cm^{-3}]
n_F	ideality constant for the diodes in the base-emitter junction modelling electron and hole injection
n_R	ideality constant for the diodes in the base-collector junction modelling electron and hole injection
n_i	intrinsic carrier concentration [cm^{-3}]
n_{iB}	intrinsic carrier concentration in base [cm^{-3}]
n_{iC}	intrinsic carrier concentration in collector [cm^{-3}]
n_{iE}	intrinsic carrier concentration in emitter [cm^{-3}]
n_m	ideality constant for the different current components of the non-ideal current in the intrinsic transistor
N_{ref}	constant for calculating doping and temperature dependent electron mobility in Silicon [cm^{-3}]
N_{val}	density of states in the valence band [cm^{-3}]
$N_{vSiGehhStrain}$	density of states for heavy holes in the valence band of strained SiGe [cm^{-3}]
$N_{vSiGelhStrain}$	density of states for light holes in the valence band of strained SiGe [cm^{-3}]
$N_{vSiGeStrain}$	total density of states in the valence band of strained SiGe [cm^{-3}]
π	constant = 3.141...
P	internally dissipated power [W]
Q	charge [As]
q	unity charge = $1.602*10^{-18}$ [As]
QE_g	temperature dependent multiplication factor for energy bandgap
Q_f	charge build-up in non-reverse biased junction capacitance [As]
Q_G	total base charge [As]
Q_r	charge build-up in reverse biased junction capacitance [As]
ρ_B	base contact resistivity [Ωcm^2]
R_B	total base-lead resistance [Ω]
R_{BCext}	series resistance in extrinsic base-collector junction [Ω]
R_{Bcont}	base contact resistance [Ω]
R_{BCpad}	resistance between base and collector pad [Ω]
R_{BEloss}	resistance for modelling shunting loss between base and emitter in the extrinsic part of the transistor [Ω]
R_{BEpad}	resistance between base and emitter pad [Ω]
R_{Blead}	resistance of base sheet leading in to intrinsic transistor [Ω]
R_{Bpad}	resistance in base pad [Ω]
R_{Bprobe}	resistance in probe connecting to the base pad [Ω]
R_C	collector contact and subcollector resistance [Ω]
R_{CEloss}	resistance for modelling shunting loss between collector and emitter in the extrinsic part of the transistor [Ω]
R_{CEpad}	resistance between collector and emitter pad [Ω]

R_{Closs}	resistance for modelling loss in the collector lead of the extrinsic part of the transistor [Ω]
R_{Cpad}	resistance in collector pad [Ω]
R_{Cprobe}	resistance in probe connecting to the collector pad [Ω]
$R_{Cundepl}$	resistance of undepleted part of collector [Ω]
ρ_E	emitter contact resistivity [Ωcm^2]
R_{Econt}	emitter contact resistance [Ω]
R_{Eloss}	resistance for modelling loss in the emitter-lead of the extrinsic part of the transistor [Ω]
R_{Epad}	resistance in emitter pad [Ω]
R_{Eprobe}	resistance in probe connecting to the emitter pad [Ω]
$R_{Eundepl}$	resistance of undepleted part of emitter [Ω]
S_{11}	scattering parameter
S_{12}	scattering parameter
S_{21}	scattering parameter
S_{22}	scattering parameter
T	junction temperature [K]
τ	total delay [s]
T_0	ambient temperature [K]
τ_B	base diffusion delay [s]
τ_C	collector transit time delay [s]
τ_F	adjustment parameter for delay [s]
v	applied voltage [V]
v_{BC}	total base-collector voltage [V]
v_{BE}	total base-emitter voltage [V]
v_{CE}	total collector-emitter voltage [V]
V_{BC}	DC-part of base-collector voltage [V]
V_{BE}	DC part of base-emitter voltage [V]
V_{Cbreak}	collector breakdown voltage [V]
V_j	built-in voltage [V]
V_{jC0}	built-in voltage in base-collector junction [V]
V_{jC00}	built-in voltage in base-collector junction at fixed ambient temperature [V]
V_{jE0}	built-in voltage in base-emitter junction [V]
$V_{Offsetm}$	offset voltages used to simplify extraction of non-ideal current components in the intrinsic transistor [V]
v_S	electron saturation velocity in silicon [cm/s]
V_T	thermal voltage [V]
V_{T0}	thermal voltage at ambient temperature [V]
V_{thermm}	model parameters for thermal dependence of non-ideal current components in the intrinsic transistor [V]
ω	angular frequency [rad/s]
W_B	total base width [cm]
W_{Beff}	effective base width [cm]

W_C	total collector width [cm]
W_E	total emitter width [cm]
W_F	width of emitter in direction perpendicular to the base current [cm]
x_{GE}	fraction of Germanium content in the base
X_j	depletion width [cm]
X_{j0}	depletion width at zero bias [cm]
X_{jBC}	depletion width in base on collector side [cm]
X_{jC}	depletion width in collector SCR [cm]
X_{jC00}	depletion width in collector SCR at zero bias and ambient temperature [cm]
X_{jE}	depletion width in emitter SCR [cm]

APPENDIX 2:
VARIATION IN S-PARAMETERS FROM A VARIATION IN MODEL PARAMETERS

This appendix will show the impact on S-parameter from a variation in different circuit parameters as seen in Fig. 10 and Fig. 11. Only the parameters that show a distinguishable difference in the S-parameters when varying the circuit parameter have been included. The values of the circuit parameters have been varied one at a time around its nominal value with a factor of 10, i.e., curves corresponding to 0.1, 1 and 10 times the nominal value are shown for each S-parameter. Other circuit parameters has then been kept at their nominal values.

The reason for varying the circuit parameters rather than physical parameters is to facilitate the identification of the impact each circuit parameter has which in turn can lead to understanding of how the underlying physical or technological parameters should be altered in the case of, e.g., a fitting procedure. The S-parameters relate to small signal circuits and the interpretation is thus easiest done using the circuit parameters of the model.

The S-parameters have been calculated with the transistor in a common emitter configuration, connecting port 1 to the base and port 2 to the collector. Port impedance is set to 50 Ω . All S-parameters have been calculated in a frequency range from 200 MHz to 50 GHz. Common for all graphs is that frequency increases clockwise in the curves. To facilitate the interpratation of the S-parameters, simplified eqivalent circuits are shown in Fig. 36 for the case when measurements are done from port 1 and port 2, corresponding to Fig. 36 a and b, respectively. The nominal values of the different lumped elements can be seen in Table 5.

Table 5. Nominal values for components in Fig. 36.
Bias for the component is: V_{CE}=2 V, I_C=4.0 mA

R_{Bcont}	[Ω]	17	C_{BC}	[fF]	4.9
C_{shunt}	[fF]	750	$^{*}C_{BE}$	[fF]	220
R_{Blead}	[Ω]	12	$^{**}r_{BE}$	[Ω]	360
R_{BCext}	[Ω]	4.0	$R_{Eundepl}$	[Ω]	0.92
C_{BCext}	[fF]	40	R_{Econt}	[Ω]	5.3
R_C	[Ω]	5.0	$^{***}\beta$		69
$R_{Cundepl}$	[Ω]	12			

* includes junction and diffusion capacitance. They are approximately equal.

** dynamic resistance of base-emitter junction.

*** current amplification factor.

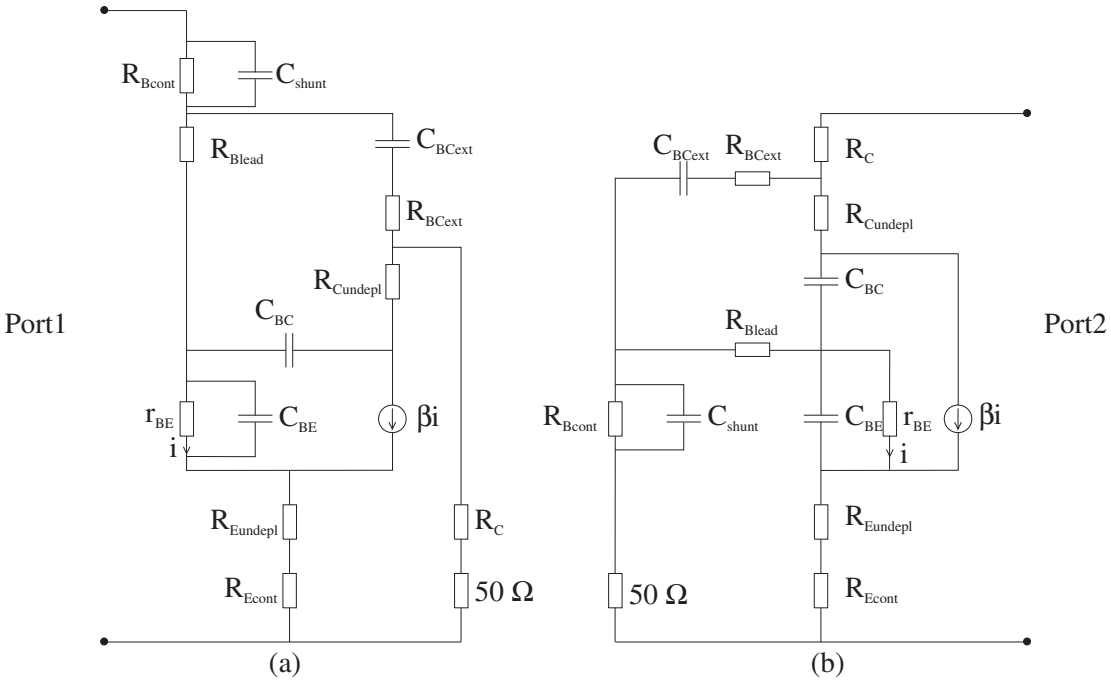

Fig. 36 Simplified equivalent circuits identifying the relative positions of the different components in the transistor when performing measurements from (a) port1 or (b) port2.

The impact on the S-parameters from a variation in R_{Bcont} can be seen in Fig. 37. At high values of R_{Bcont}, the magnitude of the forward coupling (S_{21}) exhibit a different behaviour from the two other curves. An explanation to this can be that at the very low frequencies, no capacitances shunts any part of the transistor and the high value in the base-lead is thus affecting the performance to a certain amount as can be seen in Fig. 37 S_{21}. At frequencies above the very low however, capacitances within the transistor begin to load and thus cause a voltage drop over R_{Bcont} which lowers the forward coupling. With increasing frequency C_{Bshunt} starts shunting R_{Bcont} and the impact from R_{Bcont} is decreased, thus the curve more resembles the one of R_{Bcont} at lower values.

The impact on S_{11} from a variation of C_{Bshunt} indicates the validity of modelling the base contact with a shunting capacitance. At low values of C_{Bshunt} the resistance R_{Bcont} is included in the base-lead resistance which leads to a higher resistance at higher frequencies (see Fig. 38) compared to the case of a nominal or high value of C_{Bshunt}. At a high value of C_{Bshunt}, the resistance R_{Bcont} is instead shunted at all frequencies, see Fig. 38. Using the nominal value of C_{Bshunt}, R_{Bcont} is at low frequencies part of the base-lead resistance and thus following the curve corresponding to a low value of C_{Bshunt}. With increasing frequency, the reactance of the capacitance decreases and R_{Bcont} becomes increasingly shunted, thus the curve of the nominal C_{Bshunt} migrates at higher frequencies towards the curve of the higher value of C_{Bshunt}, see Fig. 38.

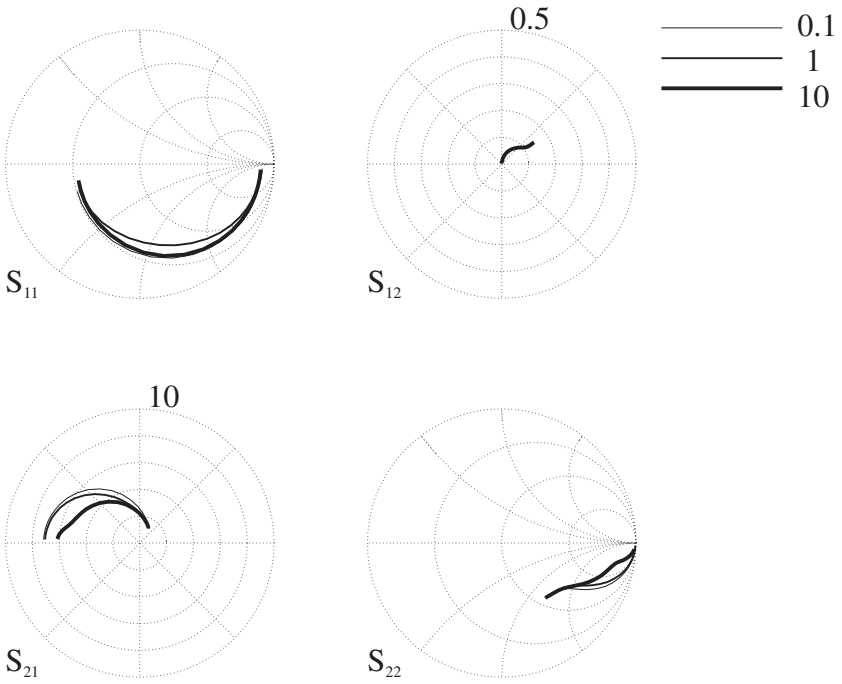

Fig. 37 Calculated S-parameters for three different values of R_{Bcont}

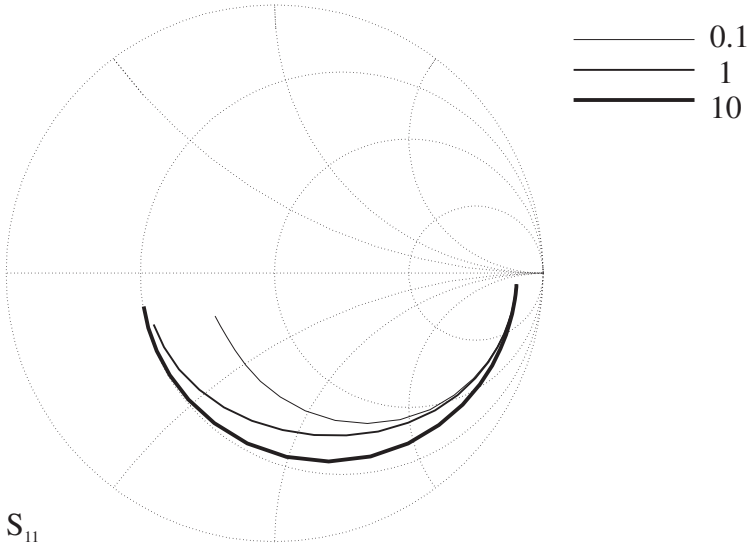

Fig. 38 Calculated S_{11} for three different values of C_{Bshunt}.

The parameter C_{BCext} has a greater impact on S_{22} than it has on S_{11}. It can however be observed that at high values of C_{BCext}, the input impedance at port 1 is shunted to port 2 which is terminated in 50 Ω thus causing the kink in S_{11} at higher frequencies, see Fig. 39 S_{11}. The shunting effect can be verified in S_{12} where the feedback coupling varies strongly with the different values of C_{BCext}. Due to the coupling in S_{12}, S_{22} is also strongly affected. At low C_{BCext}, the intrinsic transistor is not shunted which can be seen as a high impedance, see Fig. 39 S_{22}. At high values of C_{BCext} the intrinsic transistor is fully shunted and S_{22} corresponds instead to a parallel circuit consisting of the port 1 impedance (50 Ω) and the base-emitter impedance, thus giving a total impedance at port 2 which is slightly less than 50 Ω , see Fig. 39 S_{22}.

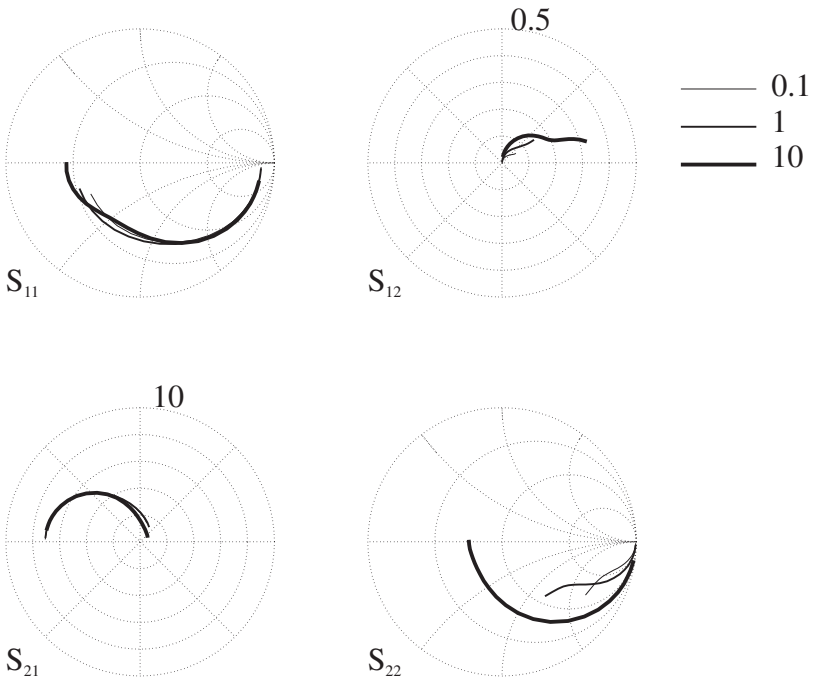

Fig. 39 Calculated S-parameters for three different values of C_{BCext}.

Input impedance from port 1 is clearly affected by R_{Blead}. At a high value the shunting via C_{BCext} will come into effect at high frequencies, see Fig. 40 S_{11}, where the impedance is that of the lead consisting of C_{BCext}, R_{BCext}, R_C and the impedance of port 2 (50 Ω). This shunting can also be seen in Fig. 40 S_{12} where the feedback coupling increases at high values of R_{Blead}. The forward coupling (S_{21}) goes also down at high values of R_{Blead} which intuitively can be explained with that less signal becomes available to the intrinsic transistor, see Fig. 40 S_{21}.

The interpretation of the impedance at port 2, see Fig. 40 S_{22}, gives that at high values of R_{Blead}, feedback coupling through the intrinsic part of the transistor via C_{BC} is blocked, thus giving a high impedance. At higher frequency the intrinsic transistor in series with R_{Blead} is is shunted by C_{BCext}. It should be pointed out that the effective impedance seen from port 2 is at all frequencies higher for the high value of R_{Blead} than for the other values of R_{Blead}. The crossing of the different curves in the Smith chart for S_{22}, see Fig. 40 S_{22}, can thus not be used for immediate conclusions of the impedance.

The collector-lead resistance, $R_{Cundepl}$, has mainly an impact on the impedance at port 2 which increases with increasing $R_{Cundepl}$, see Fig. 41 S_{22}. Similar variation as the one caused by a variation of $R_{Cundepl}$ in S_{22} is seen from a variation of R_C. The impact on S_{11} is however then negligible.

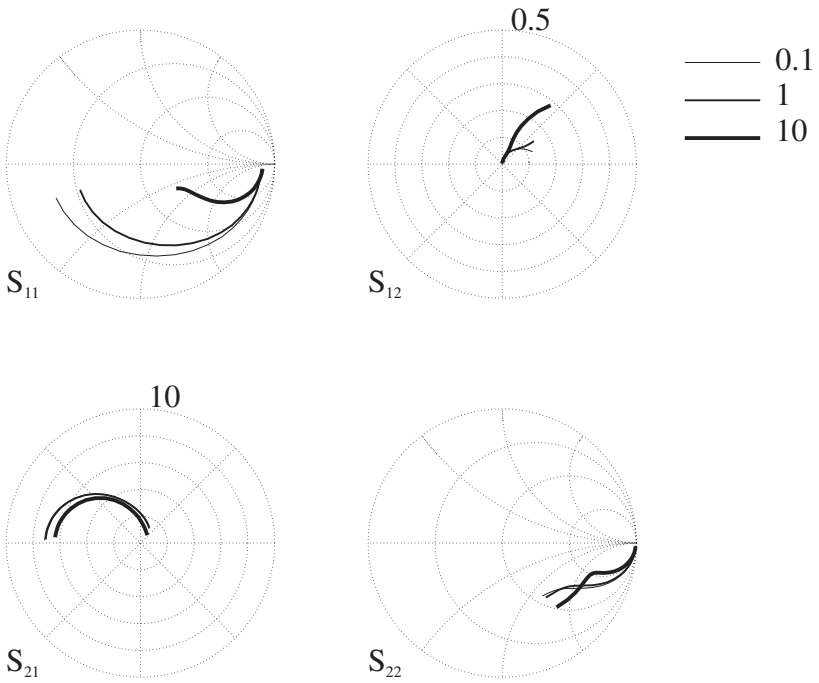

Fig. 40 Calculated S-parameters for three different values of R_{Blead}.

An increase in $R_{Cundepl}$ appear to increase the impedance at port 1, see Fig. 41 S_{11}, but the magnitude of the impedance is instead decreasing with an increasing $R_{Cundepl}$ except for very high frequencies (above 40 GHz). This can not be clearly distinguished from the Smith chart as it does not contain any direct frequency information. An explanation for the decrease in impedance with an increasing $R_{Cundepl}$ can be found in how the current i, see Fig. 36 a, is shunted from r_{BE} via $R_{Cundepl}$. With a lower shunt of i, the current generator (βi) also conducts more current which is interpreted as a lower impedance. The fact that a variation of R_C does not affect S_{11} supports this explanation.

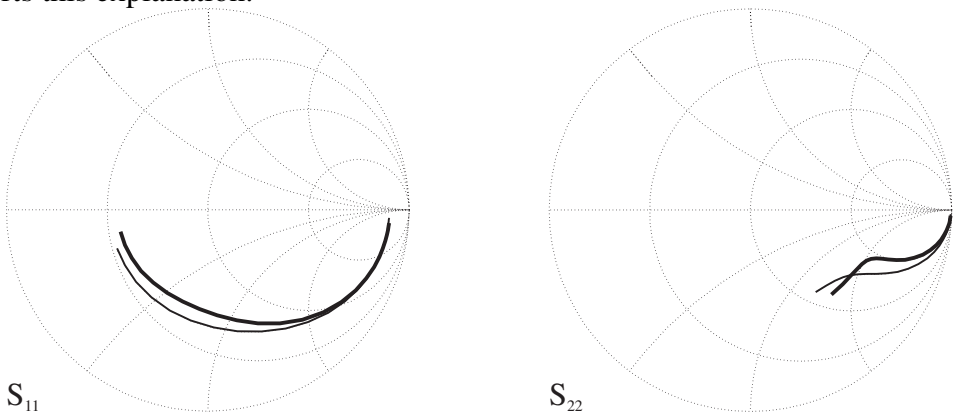

Fig. 41 Calculated S_{22} for three different values of $R_{Cundepl}$.

The emitter-contact resistance, R_{Econt}, has a great impact on several parameters, also parameters related to DC, e.g., collector current and thus the bias point, which makes it very difficult to make any simple interpretation of the result of a variation of this parameter. The curves in Fig. 42 are included to point out directions of the different

S-parameters for a variation of R_{Econt}. Similar variation can be noticed for a variation of $R_{Eundepl}$ and the resulting S-parameters for a variation of $R_{Eundepl}$ has thus not been included.

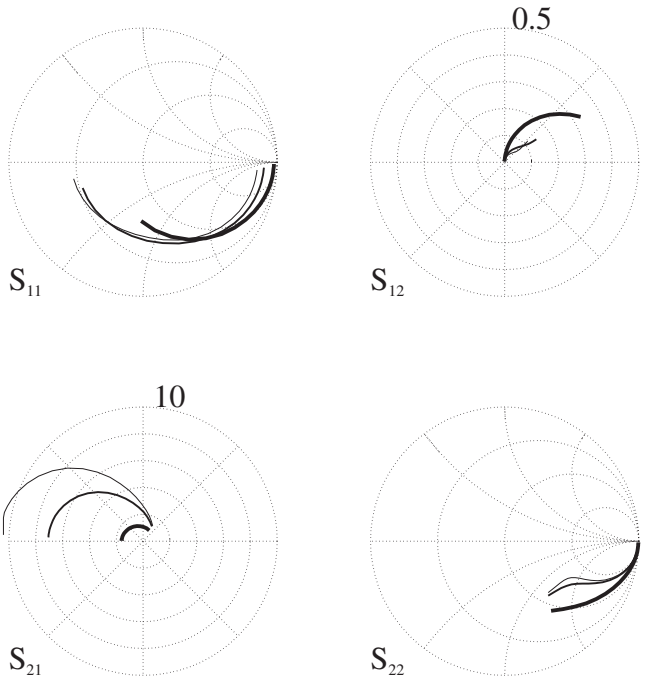

Fig. 42 Calculated S-parameters for three different values of R_{Econt}. Legend is the same as in Fig. 37.

The intrinsic base-collector capacitance (C_{BC}) has an impact on the input impedance of port 1. Indeed, the input impedance calculated from S_{11} in Fig. 43 shows a decrease with increasing capacitance for all but the highest frequencies (i.e., frequencies below 45 GHz) as would be expected. At the highest frequencies, the delays in the transistor seems to act as inductances which may cause resonance phenomenons together with the capacitances thus increasing the impedance. This was verified by setting the delays in the transistor to zero which yielded the same behaviour at higher frequencies as the one described for lower ones. Due to the absence of immediate frequency information in the Smith chart, the impact of a capacitance variation is not obvious in Fig. 43 S_{11}.

The shunting can clearly be seen in Fig. 43 S_{22} which indicates a lowering in impedance seen from port 2. At higher frequencies the base-emitter impedance becomes dominant which leads to a further decrease of the impedance, seen as a kink for all three curves in Fig. 43 S_{22}.

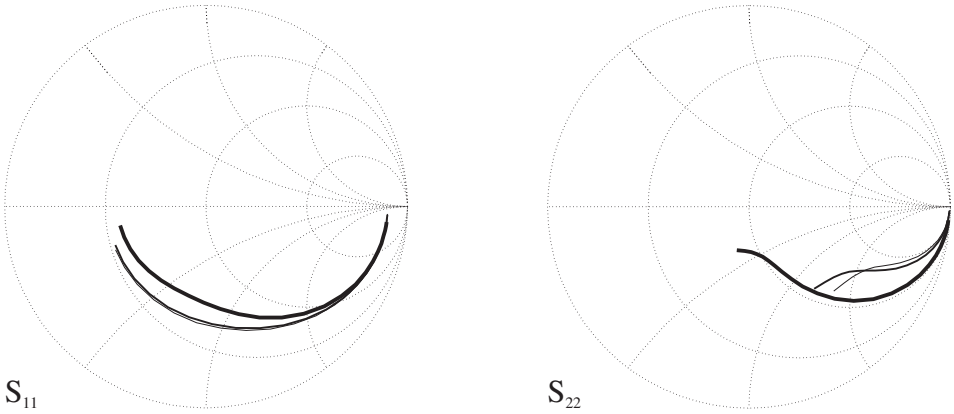

Fig. 43 Calculated S-parameters for three different values of C_{BC}. Legend is the same as in Fig. 37.

In a similar way as the input impedance on port1 is affected by a variation of C_{BC}, it is also affected by a variation of C_{BE}, see Fig. 44 S_{11}. The magnitude of the impedance is however continuously decreasing with increasing C_{BE} for all frequencies. The input impedance of port 2 is also strongly affected, see Fig. 44 S_{22}. It is slightly counterintuitive that a higher capacitance should result in a higher impedance, which however is the case, see Fig. 44 S_{22}. The capacitance is shunting the base-emitter junction and is thus also affecting the injection of carriers into the base. This causes a decrease of current in the collector lead for a given voltage variation which is interpreted as an increase in impedance.

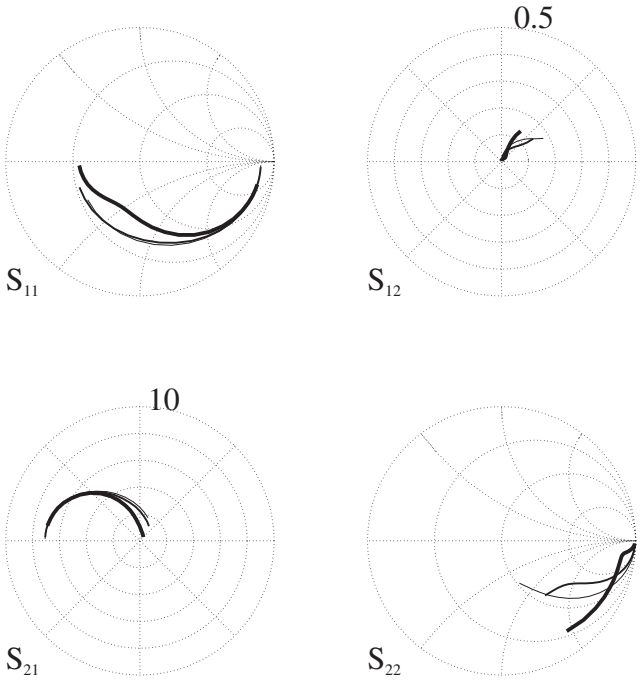

Fig. 44 Calculated S-parameters for three different values of C_{BE}. Legend is the same as in Fig. 37.

The impact from a variation of the total delay through the transistor, τ, has similarities to those of variations of C_{BE} and C_{BC}. Conclusions are however difficult to

draw from the S-parameters and the curves are thus here included to indicate the effects of variations in τ.

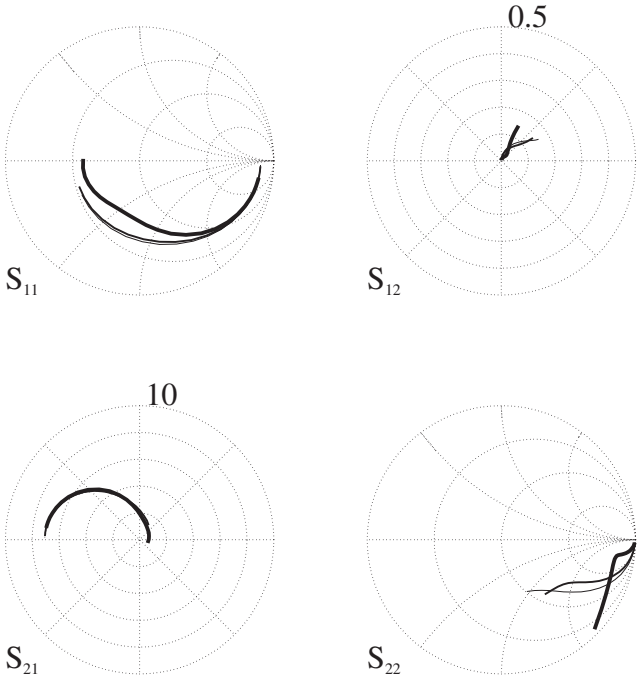

Fig. 45 Calculated S-parameters for three different values of τ. Legend is the same as in Fig. 37.