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Silicon Germanium Heterojunction Bipolar Transistors

Large-Signal Modeling and Low-Frequency Noise Characterization Aspects

BY

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ABSTRACT

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In this thesis, aspects of the Silicon Germanium (SiGe) Heterojunction Bipolar Transistor (HBT) are addressed. A physics-based electrical large-signal model including thermal dependence has been developed and is implemented using a commercially available simulator package. Good agreement is found between calculated data using the model and measured data. Equations for the electrical parameters based on physical data and a fitting procedure for finding parameter values concerning parasitic effects are presented. In addition, a technique for extracting very short thermal time constants using small signal measurements is presented.
Using the large-signal model, a frequency multiplier employing a single SiGe HBT as the non-linear device has been designed and fabricated. The doubler operates with an output frequency of 55 GHz and performance can be well explained using the model.
Low-frequency noise in the SiGe HBT has been studied, primarily using transimpedance amplifiers. Problems related to the measurement of low-frequency noise are discussed. The dominant noise source in a SiGe HBT is discriminated using direct two-channel noise measurements for a sweep of base resistance terminations of the device. By employing a device temperature variation, the temperature dependence of the dominant source is further studied. A method for improved coherence measurements during a sweep of base resistance terminations is presented. A method for modeling low-frequency noise in a SPICE based simulator and aspects of the noise corner frequency are discussed.

Key-words: Silicon Germanium, SiGe, Heterojunction Bipolar Transistor, HBT, Large-signal modeling, thermal time constant, low-frequency noise, coherence, transimpedance amplifier.

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List of papers

I. S. Bruce, A. Rydberg, H. Schumacher, U. Erben, J-F. Luy, M. Karlsteen, and M. Willander, "Development, implementation and verification of a physics-based Si/SiGe HBT model for millimeter-wave non-linear circuit simulations," in *Proceedings of the 26th European Microwave Conference*, Prague, Czech Republic, 1996, vol. 2, pp. 903–905.

II. S. Bruce, M. Kim, A. Rydberg, K. M. Strohm, and F. Beißwanger, "On the design of a 55 GHz Si/SiGe HBT frequency doubler operating close to f_{max}," in *Proceedings of the 26th European Microwave Conference*, Prague, Czech Republic, 1996, vol. 1, pp. 297–299.

III. S. Bruce, A. Trasser, M. Birk, A. Rydberg, and H. Schumacher, "Extraction of thermal time constant in HBTs using small signal measurements," *Electronics Letters*, vol. 33, pp. 165 – 167, 1997.

IV. S. Bruce, A. Rydberg, M. Kim, F. Beiβwanger, J. F. Luy, H. Schumacher, U. Erben, M. Willander, and M. Karlsteen, "Design and realization of a millimeter-wave Si/SiGe HBT frequency multiplier," *IEEE Trans. Microwave Theory Tech.*, vol. 46, no. 5, pp. 695 – 700, May 1998.

V. S. Bruce, L. K. J. Vandamme, and A. Rydberg, "Measurement of low-frequency base and collector current noise and coherence in SiGe heterojunction bipolar transistors using transimpedance amplifiers," *IEEE Trans. Elec. Devices*, vol. 46, pp. 993–1000, May 1999.

VI. S. Bruce, A. Rydberg, and L. K. J. Vandamme, "Temperature dependence and electrical properties of dominant low-frequency noise source in SiGe HBT," To be submitted.

VII. S. Bruce, A. Rydberg, and L. K. J. Vandamme, "Improved coherence measurements using voltage and transimpedance amplifiers in noise characterization of bipolar transistors," To be submitted.

VIII. S. Bruce, A. Rydberg, and L. K. J. Vandamme, "Simulation of noise in SPICE-like simulators using AC voltage and current sources only," To be submitted.

List of related papers

The following papers are related to work presented in this thesis, but have not been included.

I. S. Bruce, A. Rydberg, W. Seibt, and M. Willander, "Single and multi-section CTL and branch-line CPW directional couplers with broadband performances for SIMMWIC," *Int. J. of Infrared and Millimeter Waves*, vol. 15, pp. 751–761, 1994.

II. A. Rydberg, S. Bruce, and W. Seibt, "Passive CPW components for SIMMWIC applications," in *Proc. workshop on "Silicon Based High Frequency Devices and Circuits"*, Günzburg, Germany, November 1994.

III. S. Bruce, A. Rydberg, J-F. Luy, F. Schäffler, M. Karlsteen, M. Willander, and W. Seibt, "A modified Ebers-Moll model for millimeter-wave Si/SiGe HBT's," in *Proc. workshop on "Silicon Based High Frequency Devices and Circuits"*, Günzburg, Germany, November 1994.

IV. S. Bruce, A. Rydberg, W. Seibt, and M. Willander, "Single and multi-section CPW couplers with broadband performances for SIMMWIC," in *Proc. GigaHertz 94*, Linköping, Sweden, 1994.

V. S. Bruce, M. Kim, E. Bak, A. Rydberg, K. M. Strohm, and F. Beiβwanger, "A 55 GHz SIMMWIC Si/SiGe HBT frequency multiplier," in *Proc. workshop on "Low-Power Microwave Electronics"*, Ulm, Germany, 1995.

VI. S. Bruce, A. Rydberg, H. Schumacher, U. Erben, J.-F. Luy, F. Schäffler, M. Karlsteen, and M. Willander, "A physics-based large-signal Si/SiGe HBT model for millimeter-wave non-linear circuit simulations," in *Proc. GigaHertz 95*, Göteborg, Sweden, October 1995.

VII. A. Rydberg and S. Bruce, "Silicon-based technology for millimeter-wave applications," in *Proc. RVK 96*, Luleå, Sweden, 1996.

VIII. S. Bruce, A. Trasser, M. Birk, A. Rydberg, and H. Schumacher, "Extraction of thermal time constant in devices exhibiting conductivity modulation caused by thermal effects," in *Proc. GigaHertz 97*, Kista, Sweden, 1997.

Preface

This thesis represents a summary of the research performed by Staffan Bruce at Uppsala University between 1994 and 1999. The work concerns in part the modeling of the Silicon Germanium heterojunction bipolar transistor with its applications to high frequency circuits. In part the work has also been directed towards the low-frequency noise properties of the SiGe HBT; measurement techniques and development of the understanding of the noise sources from a circuit point of view.

The contribution made by Staffan Bruce to the appended papers are:

Paper I:	Developing model, measurements, writing the manuscript.
Paper II:	Partly designing the circuit, measurements, writing the manuscript.
Paper III:	Developing method, measurements, writing the manuscript.
Paper IV:	Developing model, simulation strategy, measurements, writing the manuscript.
Paper V:	Developing method, measurements, interpretation, writing the manuscript.
Paper VI:	Developing method, measurements, interpretation, writing the manuscript.
Paper VII:	Developing method, measurements, interpretation, writing the manuscript.
Paper VIII:	Idea, writing the manuscript.

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There are many people who, in different ways, have helped me in my way towards this thesis.

It is to me clear that my advisor, Doc. Anders Rydberg, deserves a special acknowledgement. Throughout my time as a Ph.D. student I have consequently felt a great support and freedom to develop in my own direction for which I am very grateful.

My Ph.D. studies would however not have been possible without Prof. Sören Berg accepting me as a Ph.D. student in Electronics.

My office location has been with the Signals and Systems group. Listing all my colleagues here would unfortunately be too long so I would like to thank them all for all interesting discussions on both professional and not so professional topics. A special thanks goes to Prof. Anders Ahlén for continuously providing a very nice working atmosphere.

Throughout my Ph.D. studies I have had the opportunity to work outside Sweden at two departments where I have felt very welcome.

I would like to thank Prof. Hermann Schumacher and all co-workers at Department of Electron Devices and Circuits at University of Ulm in Germany for helping me in all ways during my stays there. I am especially thankful to Prof. Schumacher for always welcoming me to the department for shorter or longer stays. My thanks also to Dr. Uwe Erben, Dr. Andreas Trasser and Dr. Martin Birk for all help and many interesting discussions.

I would also like to thank Dr. Lode Vandamme and all co-workers at the Department of Electrical Engineering at the Technical University of Eindhoven in The Netherlands for the excellent help during my stays at their department. I would like especially to thank Dr. Lode Vandamme for his hospitality, his great help in introducing me to low-frequency noise measurements and his thorough proof-reading of several manuscripts. I'm indebted to M.Sc. Otto Stoelinga, M.Sc. Joost Briaire, M.Sc. Ewout Vandamme and M.Sc. Rene Jonkers for very interesting discussions of various kinds. M.Sc. Rene Jonkers was the person who finally got me interested in LaTeX which is something I am very happy – and sometimes frustrated – about.

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I sincerely thank the Linux community for creating an operating system which not only is free, but also very powerful and easy to use. My personal development in this area has benefited greatly from Mr. Ove Ewerlids patient help which I am very grateful for.

On the more personal plane I would like to thank two families with whom I have a very good time and who mean very much to me: my parents Åke and Ingar Bruce and my sisters and brother Annika, Karin and Håkan, and my wonderful girlfriends parents and sister, Kjell and Gunilla Ragnarsson and Anna.

Finally I would like to thank my girlfriend Malin Ragnarsson for all her love – it is reciprocated.

To all those people whom I have not named explicitly or inadvertently left out, thank you.

Introduction

With the progress in Silicon Germanium (SiGe) technology, fabrication of high performance heterojunction bipolar transistors (HBTs) has become feasible and devices with f_{max} of 90 GHz in a common-emitter configuration [1] have been achieved with repeatability. This gives the possibilities of designing circuits operating in the millimeter-wave frequency region using the SiGe HBT as the active device. This thesis will deal with different aspects of the device.

Large-signal model of the HBT

Electrical large-signal modeling spanning from steady state (often called "DC") to high-frequency (often called "RF") forms one very important part of the work presented in this thesis.

In order to be able to account for large-signal effects occurring in various high-frequency applications, e.g., power amplifiers, mixers and doublers, a large-signal model has been developed. The model is described in the thesis text and is also presented in *Paper I* and partly in *Paper IV*.

The model is based on a modified Ebers-Moll model, where emphasis has been put on deriving model parameters from technological data, e.g., device geometry, and semiconductor physics. By partitioning the currents in the device between holes and electrons respectively, effects of the band-gap difference within the device are effectively accounted for which leads, e.g., to an easier modeling of the thermal effects. The thermal model is connected to the electrical model through an interface. Through the interface the internal power dissipation of the device is output as a current which, in the thermal model, is converted to a voltage corresponding to a temperature elevation of the device that is fed back to the electrical model. With the separation of the two models improved convergence is achieved in the simulations. It is also possible to model different types of devices through a variation in thermal modeling. A multi emitter-finger device can for example be modeled by coupling several electric model via a thermal network. Comparisons between measured and calculated data of both DC and RF characteristics show that the model well predicts device performance within normal bias ranges, given a fitting of fundamental parameters towards measured data. The fitting towards measured data is necessary in order to account for variations in the fabrication process and to model currents caused by parasitic elements of the device.

Design of a Si/SiGe HBT frequency doubler operating close to f_{max}

As an application for the large-signal transistor model, a frequency doubler for millimeter-wave applications has been designed and is described in *Paper II* and *IV*. With an output frequency of 55 GHz it operates close to f_{max} of the transistor which in this case is 67 GHz. The rule of thumb for an oscillator is that the operating frequency should be smaller than one third of f_{max}. It would thus mean that an f_{max} of approximately 165 GHz would be necessary. Such devices have been fabricated, but to achieve a higher reproducibility the demands should be lowered to an f_{max} of about 80 to 100 GHz which would yield an oscillator operating with, at highest, 30 GHz of output frequency. With an active frequency doubler it is however possible to use gain in the device to amplify at the comparably low fundamental frequency which then is converted to its second harmonic. A signal generator like the one designed can be used in for example car-to-road communication or car radar (operating at 60 GHz and 77 GHz respectively). With the operating frequency of 55 GHz, the frequency doubler suits well to the radio link frequency allocated at 55 GHz.

The design of the circuit has been done in MDS. To find the correct parameters for the embedding structure around the transistor, an iterative process has been employed. Ideal S-parameter blocks have initially been connected to the input and output of the transistor to find optimal matching circuits for doubler operation. With the acquired S-parameter blocks, an optimization for matching circuits consisting of coplanar waveguide (CPW) elements is done. Due to the difference between ideal S-parameters blocks and the circuits consisting of CPWs, optimization with an ideal S-parameter block for either input or output needs to be reiterated. Measured results of a fabricated doubler showed a conversion from input at 27.5 GHz to output at 55 GHz of better than -12 dB which is comparable with a doubler circuit realized with a III-V HFET as active device [2]. Performance of the doubler circuit calculated using the large-signal model compare well with measured data. Prediction by the model using harmonic balance simulation at 55 GHz shows that a conversion efficiency for the Si/SiGe HBT of about 5 dB can be expected from future optimized circuits.

Extraction of thermal time constant

So far many models incorporate thermal modeling in the shape of an RC-circuit where the capacitive part accounts for the transient effects. Due to the thermal time constant, the circuit does not reach steady state instantaneously. Some papers have been published on the extraction of the thermal resistance, but very little has been done for the capacitance, or time constant, however. The work in *Paper III* is aimed at addressing this question as it can be of great importance for applications where the large-signal effects make the power dissipation vary greatly in very short moments of time. A fast variation in power dissipation causes a variation in junction temperature which can affect operating point and thus also behavior.

The common method for finding the thermal time constant measures the actual time for heating a circuit from a low level to a high level of power dissipation. This method necessitates a good control of the power fed to the device during a very short period of time. In larger devices the time resolution in the extraction procedure can be allowed to decrease somewhat, but in applications using very small components, the time constant itself makes well controlled measurements in the time domain more difficult to control and a different method needs to be employed. The benefit with the new technique is that it operates in the frequency domain using small signal measurements which makes the need of a good power control somewhat unnecessary. Furthermore the proposed method facilitates measurements of time constants down to 1 μs with very simple equipment. Refinements of the measurement equipment can expand the range. The common method should however not be ruled out as it gives a probably more accurate value of the overall large-signal thermal time constant in structures. Due to the actual heating of the device, the method may also account for secondary effects like cross-heating between devices. This is a very slow process compared to the internal heating and will also not occur during small signal measurements. A complete characterization should therefore employ both methods. In a wider perspective the proposed method should be usable for other three-terminal devices where the transition between steady state and transient operation regarding the thermal effects can be clearly distinguished. Transitions relating to electrical effects, e.g., parasitics with similar time constants to the one of the thermal may obscure the results and complicate the extraction.

Low-frequency noise aspects

The low-frequency noise aspects of the SiGe HBT is important to investigate for two major reasons: its degrading effect on circuit performance and its use as a sensitive diagnostic tool. The work presented in the thesis text and *Paper V-VIII* deals mainly with measurement aspects and interpretation of the low-frequency noise as such.

Due to non-linearities within almost any high-frequency circuit, the low-frequency noise will be converted to a considerably higher frequency where it may disturb the functionality of the designed circuit. Thus, a good understanding of how the low-frequency noise is affected by circuitry external to the actual device and also a an understanding of the location of the noise sources within the device is important. By understanding what parameters are affecting the low-frequency noise, measures may be taken in the design of a RF circuit in order to lower the impact of the low-frequency noise.

Using direct measurements of the low-frequency noise of the device, valuable information can be extracted. By sweeping external parameters like bias, device temperature or input termination resistance, device parameters and location of different noise sources can be extracted. In *Paper V* a method of using transimpedance amplifiers (converting an input current to an output voltage), at both the input and the output of the device, is presented. The transimpedance amplifier as equipment is not new, but the incorporation in a two-channel measurement, where the correlation between the two signals is used for interpretation, seems not to have been employed earlier.

The low-frequency measurement procedure in itself poses several problems. Due to the very weak signals that the noise consist of, external interference is very difficult to remove. Different methods to improve the measurement methods and also comments on problems that occur have been addressed in the thesis text and in *Paper VII*. The text in the thesis should be seen as information, important in the view of the author, for performing low-frequency noise measurements of bipolar transistors. A special chapter is also included where specific measurement situations and interpretation methods are presented. Each part of the chapter addresses a specific topic. They correspond to specific parts of the performed research and are presented more thoroughly in *Paper V* and *VI*.

During the work with low-frequency noise, the use of simulation tools has been important for simplifying the interpretation of the measured data. Specifically the correlation between different simulated noise signals has been of great importance to calculate correctly. The possibility to calculate the correlation between different signals has not been directly available in the more general purpose simulators like, e.g., in SPICE. Thus a general method has been developed to simulate low-frequency noise which allows a calculation of the correlation between signals. This is presented in *Paper VIII*.

An important figure of merit often found in discussions of low-frequency noise in transistors is the corner frequency (f_c). A fairly clear definition of this term exists, but in the view of the author the ways of measuring this parameter appears not clearly defined. A chapter is thus included in the thesis text which aims at shedding light on parameters which will affect f_c. The text is not intended to define f_c, or define the way of finding its value for a specific device. The text should rather be seen as a comment on where f_c serves as a figure of merit and why it should not be used as a general figure of merit when comparing widely different devices.

Chapter 1

Introduction to the device model

1.1 The physics of the heterojunction bipolar transistor

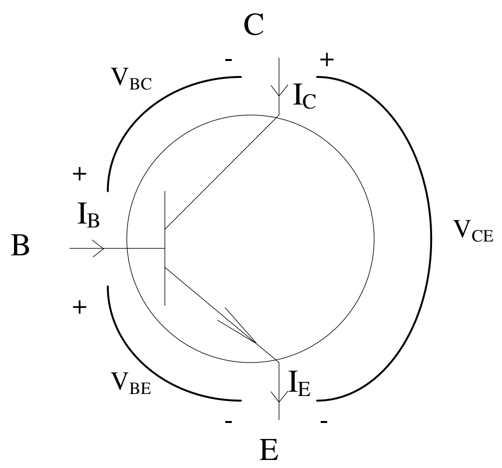

Figure 1.1: Schematic picture of the NPN transistor. Currents and voltages for the device are defined.

The bipolar junction transistor (BJT) is generally treated as a current controlled device where the current amplification factor, β, is defined as [3]:

$$\beta = \frac{\delta I_C}{\delta I_B} \tag{1.1}$$

where I_C and I_B are defined as in Fig. 1.1. Equation 1.1 can be translated to more physical terms as [3]:

$$\beta = \frac{D_{eB} n_{iB}^2}{W_B N_B} \frac{W_E N_E}{D_{hE} n_{iE}^2} \tag{1.2}$$

where a short base and emitter and a negligible base recombination has been assumed. The intrinsic carrier concentrations, n_{iE} and n_{iB} can for a BJT be considered to be equal.

The device can also be treated as a voltage controlled device where the transconductance, g_{BC} is defined as:

$$g_{BC} = \frac{\delta I_C}{\delta V_{BE}} \tag{1.3}$$

From a physics point of view, this is a more correct description of the device. The current on the output is clearly controlled by the voltage on the input, from the injection of electrons from the emitter into the base. Due to the well defined reverse injection of holes from the base to the emitter which creates a current on the input and the strict relation between the input and output current (in the ideal case), however, this definition stands back for the previously described.

Equation 1.2 shows the relation between the injection of carriers from the emitter into the base and the injection of carriers from the base to the emitter. If a large β is desired, the numerator should be as large as possible and the denominator as small as possible. In an ordinary BJT the possibilities are to set $N_E \gg N_B$ and/or making W_B small. A wide emitter does not improve the behavior very much as W_E in eq. 1.2 would be substituted for the diffusion length of the minority carriers (holes in an NPN structure) when W_E becomes too big. This puts rather strong constraints on the device and a good trade-off between the parameters is necessary. For the current amplification, a low N_B and small W_B is desirable, but at the same time the doping and width of the base must be large enough to withstand the depletion occurring in the junctions so that a punch-through of the base does not result. Furthermore a high base doping allows a higher current density before high injection effects occur caused by the minority carriers concentration reaching the doping level in the base. A high base doping in combination with a large base width gives a low base lead-resistance which is important. At the same time though it is necessary to keep the base-width low so that the delay caused by the diffusion of the minority carriers through the base is kept low. In conclusion it can be said that the device is highly dependent on the design of the base.

In the heterojunction bipolar transistor (HBT), a band-gap difference has been introduced between the emitter and base, see Fig. 1.2, to increase the degrees of freedom for the design. The band-gap difference can be accomplished by having two different material combinations like AlGaAs in the emitter and GaAs in the base and collector which gives a single heterojunction bipolar transistor (SHBT), see Fig. 1.2b. It is also possible to just introduce a different material in the base as is done in the SiGe HBT, where a strained layer of SiGe is grown. This creates then a double heterojunction bipolar transistor (DHBT) since both emitter and collector consist only of Si, see Fig. 1.2a.

The concept of increasing device performance by introducing different band-gap structures was suggested early by Shockley [3], but due to limitations in the fabrication technology the practical development of the HBT did not begin until the early seventies when the technology of molecular beam epitaxy (MBE) developed [4].

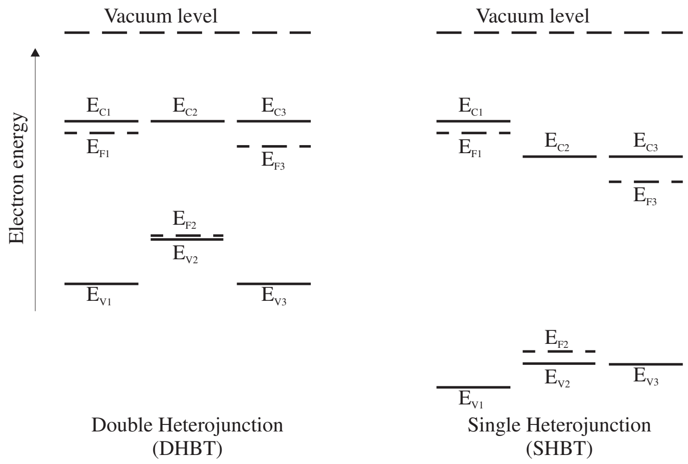

Figure 1.2: Comparison of band diagrams for Si/SiGe/Si DHBT and an AlGaAs/GaAs/GaAs SHBT where both transistors are of NPN-type. $\mathrm{E_V}$, $\mathrm{E_F}$ *and* $\mathrm{E_C}$ *define valence band-, Fermi- and conduction band level, respectively. The energy levels are drawn to scale for a comparison between the two structures (distance to vacuum level is decreased to fit the figure).*

The resulting effect is the same for the both types of heterojunctions: β increases drastically with increasing band-gap difference. The reason for this can be seen in eq. 1.2 and eq. 1.4. The intrinsic carrier concentration is strongly dependent on the band-gap in the following way [3]:

$$n_i \propto \sqrt{e^{\frac{-E_g}{qV_T}}} \tag{1.4}$$

$$V_T = \frac{k_B T}{q} \tag{1.5}$$

Thus the current amplification factor for the HBT can be defined as:

$$\beta_{HBT} = \frac{D_{eB}}{W_B N_B} \frac{W_E N_E}{D_{hE}} e^{\frac{\Delta E_g}{k_B T}} \tag{1.6}$$

where $\Delta \mathrm{E_g}$ is the difference in band-gap between the emitter and base. Depletion width of the base-emitter junction has been considered negligible in comparison to $\mathrm{W_B}$ and $\mathrm{W_E}$ since the junction is forward biased. As the second term in eq. 1.6

can amount to several orders of magnitude it is no longer necessary to keep the constraints put on the BJT. Most importantly, the base doping can be increased to values above the emitter doping and still maintain an adequate gain. This means that the base width can be lowered without risking neither punch-through nor a too high base lead-resistance. The current density can also be increased which means that an HBT can be made smaller compared to a BJT which also decreases parasitics. Thanks to these changes the unity current gain frequency (f_t) increases and more importantly for microwave applications, the maximum frequency of oscillation (f_{max}) increases. A big impact here has the base lead-resistance which can be seen from the expression [5]:

$$f_{max} = \sqrt{\frac{f_t}{8\pi R_B C_{BC}}} \tag{1.7}$$

where R_B is the whole base-lead resistance and C_{BC} is the collector capacitance. There are also approaches to grade the band-gap of the base to create a drift field for the minority carriers in order to decrease the base delay, but this would unfortunately result in a lower band-gap difference at the base emitter junction which is not desirable. A trade-off between high β_{HBT} and low base delay could here be considered.

1.2 The studied device

In this work, mainly double mesa devices (see Fig. 1.3) fabricated by Daimler Benz Research Center (DBRC) in Ulm, Germany have been studied. With this design DBRC has at present the world record of f_{max} [6]. Sub-micron dimensions are achieved with optical lithography by employing a self-aligning process, see Fig. 1.3. Using MBE, the process facilitates well controlled and very steep doping profiles in thin layers, see Fig. 1.4,1.5.

To get a the base contact close to the intrinsic base and thus minimize the base lead resistance, a self-alignment procedure has been employed. In the first step the emitter contact has been defined which can be seen as the highest lying metal in Fig. 1.3. By using this metallization as etch-mask when removing the emitter-layer, a slight undercut can be accommodated which assures that the subsequent metal deposition for the base-metal will not short-circuit the device, see Fig. 1.4. A very short base-lead from the extrinsic base contact to the intrinsic transistor can thus be accomplished with optical lithography. The undercut of the emitter can be estimated to between 0.1 and 0.2 μm. To isolate the device, a deep groove is etched around the whole transistor, see Fig. 1.3. To facilitate access for the etchant under the wide base contact, the metallization is made with holes, see Fig. 1.3. What can be noticed is that not all material has been removed under the base-metallization and that the device has a fairly large amount of open surfaces. This can give rise to parasitic currents.

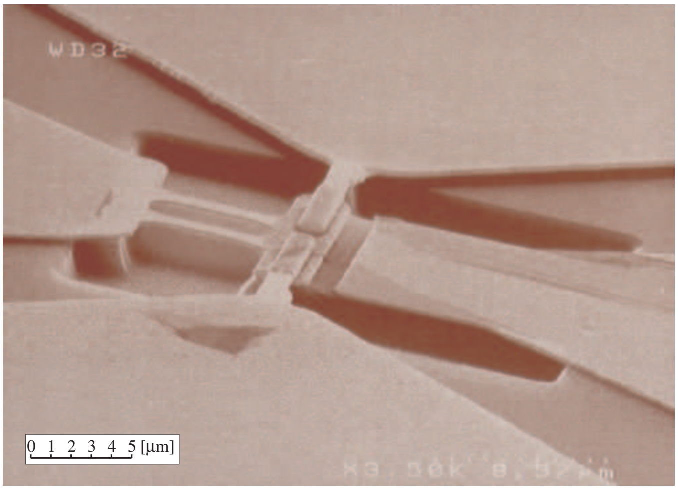

Figure 1.3: Scanning electron microscopy (SEM) picture of a transistor fabricated by DBRC. Base contact metallization is on the left side. Collector contact metallization is on the right side.

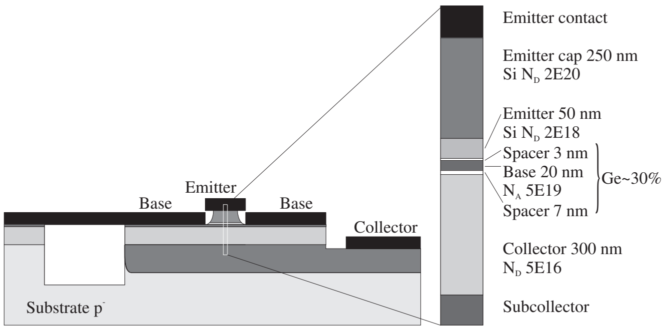

Figure 1.4: Schematic picture of the inner part of the transistor. Doping profile and thicknesses are generic values.

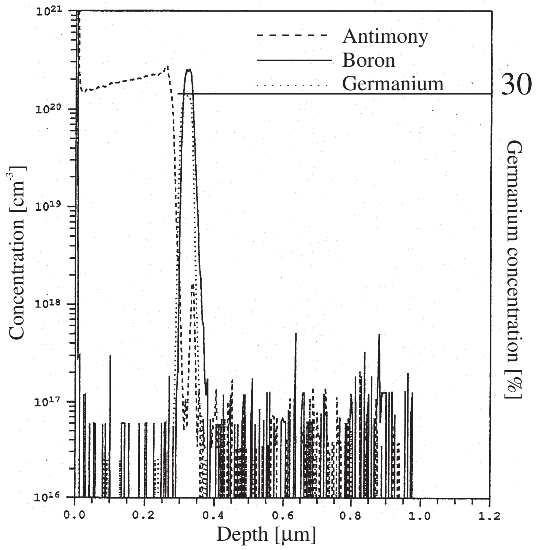

Figure 1.5: Measured data of doping and alloy levels in a sample of Si/SiGe, aimed for HBT fabrication, using secondary ion mass spectroscopy (SIMS).

1.3 Different device models

A device model is an important tool in any kind of design work. Some different types have been presented for the BJT and in general these can be considered to be aimed for two purposes [7]: to describe how the device interacts within a circuit with other devices and/or to relate device behavior to device physics. Depending on what kind of application the model is developed for, the approach in defining the model differ; from purely physical or mathematical to empirical or phenomenological. An important issue for models is the trade-off between accuracy and complexity. A good prediction of device or circuit behavior is naturally important, but by using a more complex model the computing effort and thus also time consumption increases. Fortunately the computing power has steadily increased since the advent of the computers, but this has also been accompanied by increasing complexity in the models and, not to underestimate, the complexity in the designed circuits of which one device only is a small part. With an increasing amount of elements in a device model there are also more degrees of freedom. These are unfortunately seldom orthogonal which means that there does not necessarily need to be a unique parameter set for a certain solution, or in other words, during extraction or other type of method for finding the parameters, it's not obvious how to set the relative importance or impact between the different elements that make up the model.

1.3.1 Ebers-Moll

The first model to be presented for the BJT was the Ebers-Moll model (EM) [3]. It is a physical model and in its most fundamental version there are only two diodes in parallel with two current generators. The diodes correspond to the two junctions, causing injection of carriers into the base. The current generators model how these carriers are swept through the depletion region of the opposite junction. Due to losses, e.g., recombination in the base, this current is slightly smaller and this is accounted for by the current transport factor (α). In a slightly expanded version, series resistors are added to the three terminals and two capacitors are added in parallel with the junctions. These elements can physically be related to contact and lead resistances for the resistors and junction- together with parasitic capacitances for the capacitors.

1.3.2 Gummel-Poon

In the Gummel-Poon model (GP) the terminal currents are related to the stored minority charge in the base rather than the injected currents into the base which is the case in the EM model [3]. The GP thus treats the device from a more physics-based point of view compared to the engineering-wise very intuitive EM.

Both the EM and GP have been extended from their initial definitions and they are basically equivalent, comparing the EM3 and the extended GP [8].

1.3.3 VBIC, MEXTRAM

New models for BJTs have been developed where the aim has been directed at creating a model which is easily implemented in a circuit simulator. This means having model equations that are continuous for all values of the variables and are explicit functions of only internal branch voltages, thus preventing any iterative solutions. Furthermore the equation parameters must be easily extracted from well defined measurements. As an industrial model it is also important to, to some respect, be standardized in order to facilitate portability and comparability. The Mextram model [9, 10] from Philips Research, The Netherlands and the VBIC model [10, 11] from the VBIC Consortium (with members from the major companies in the semiconductor industry) are the two major candidates for replacing the so far essentially solitaire GP in circuit simulators, e.g., SPICE. Due to the origin in industrial applications the goal has been to achieve an as correct modeling of device behavior as possible on the sacrifice of relation between model parameters and physical understanding.

Chapter 2

The developed model

2.1 Background

The initial reason for creating a model has been an interest in microwave applications and the possibility of studying designs using the HBT for these. Previously, several small signal models have been proposed, but at the start of this project, essentially no model including large-signal effects was available for the SiGe HBT. Of interest for this model was to have an as versatile set-up as possible in order to make it possible to account for many different devices (or types of devices). From a scientific (research) point of view it is also interesting to have a model which makes it possible to relate parameters to the actually model-led device in order to create a feedback from the final design to the fundamental component. This could give information on how the device could be altered to improve the performance in a particular application or, which might be even more important, to understand what part of the device/design made the application not work as desired. To meet these demands, the model should contain components that independently describe different effects or processes in the transistor in a way that makes it possible to study certain parts more thoroughly or add components to account for new effects. Furthermore, to make the model more general, the equations should not be dedicated to a certain alloy concentration of SiGe, but rather account for a variable combination where a special case should be a regular Si BJT.

2.2 Concept and idea

The Ebers-Moll model was chosen as foundation for further development into a suitable model. From an early point the choice in favor of a model consisting of physics related lumped elements was clear. With the possibility of modeling the different physical processes inside the device with different components, a clear partitioning between the different effects is possible and an intuitive understanding of the device function is also facilitated. By using physical processes to describe the function of the device, the values of the initial parameters should also be possible to calculate from data defining the actual device, e.g., device geometry, layer structure and specific parameters for contacts (contact resistivity) etc. A drawback with a physics related model consisting of lumped elements can be that certain distributed effects are difficult to model properly. This is however a general problem and where practical aspects necessitates it, phenomenological or even empirical models for the physical effects can be implemented. Preferably this approach is only done during the process of developing a more correct description based on physics, but the trade-off between research investment and accuracy pay-off must clearly be taken into consideration. The usage of lumped elements should however not be seen as an absolute decision. If computing power allows and the understanding of the physical effects is not obscured, one could consider a hybrid model where more complex or distributed parts are modeled, using for example finite element analysis (FEM).

2.3 Concept for the implementation

From a physical point of view the transistor can be divided into three different levels or complexities: the embedding part connecting the device, the extrinsic part of the transistor and the intrinsic part of the transistor, see Fig. 2.1, compare with Fig. 1.3. In the same way the model has been divided into three different shells corresponding to these levels. The reason for this can be found in the complexity of the model and in how different parts of the model have been implemented. The embedding part consists of only linear and passive elements who are immediately extracted and thus not calculated from technological data. Further on these passive elements do not scale with transistor dimensions since they essentially have a fixed, much larger dimension independent from the transistor type, see Fig. 2.1 a. The extrinsic part of the transistor (see Fig. 2.1 b) has in addition to the passive and linear elements also non-linear elements that are initially calculated from parameters related to the physical device, but not momentarily updated during simulations. Finally there is the inner core (see Fig. 2.1 c) which relates mainly to the intrinsic device. Using a special feature of the implementation program, the symbolically defined device (SDD), this part is continuously updated throughout a simulation. This means that it is possible to find for example a junction temperature rise caused by an internal power dissipation both from a DC-bias and RF power.

2.3.1 A note on accuracy in the calculations

In the following equations and expressions the number of significant digits vary. This is caused by the variation of digits in the equations found in the literature. Empirical expressions may not be possible to evaluate with more than two digits of accuracy whereas some analytical expressions may have constants that can have very high accuracy; which not necessarily assures a correct result as the model itself might be incomplete. For practical reasons a final result with an accuracy of two digits is often sufficient and for this reason it is desirable to use at least three digits within the equations, but more digits are clearly useful. In the expressions that follows, the

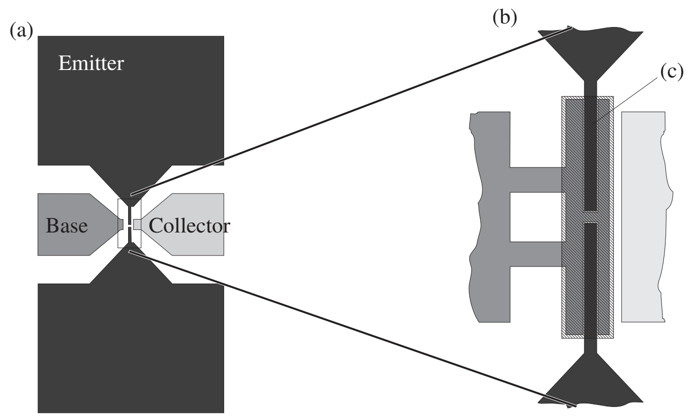

Figure 2.1: Top view of a typical transistor. (a) the left figure shows the contacting pads. (b) a close-up showing the actual transistor (shaded part) can be seen in the right figure. (c) intrinsic part of the transistor is defined as the part immediately under the emitter-finger. Base-metallization can be seen on both sides of the emitter-finger.

amount of significant digits in the expressions reflect therefore what has been found in the literature.

2.3.2 The embedding shell

The embedding shell corresponds to the parasitic elements related to the contacting pads, see Fig. 2.1 and 2.4. This means shunting capacitances between the pads (C_{BEpad}, C_{CEpad} and C_{BCpad} respectively) in series with a possible substrate resistance (R_{BEpad}, R_{CEpad} and R_{BCpad} respectively) and series inductances and resistances (L_{Bpad}, R_{Bpad}, L_{Cpad}, R_{Cpad}, L_{Epad} and R_{Epad} respectively) for each connecting terminal, see Fig. 2.4. The shunting capacitances are created through the semiconductor and are weakly bias dependent. The resistances and inductances contacting each node of the transistor originates solely in the contacting metal (see Fig. 2.1) and are thus completely bias independent.

So far the studied devices have been realized on substrates with high enough resistivity for any essential coupling to the substrate not to occur, see Fig. 2.3 which shows S_{11} of open structures. The collector pad lies immediately on the substrate, the base pad lies on the base layer which is on top of the collector layer, see Fig. 2.2. Under the base pad is thus a large base-collector junction in connection with the collector pad through the substrate. This should ensure a good insulation between the different terminals due to the high resistivity in the substrate. In a similar way the emitter and base layers are removed outside the pad metallization and thus there is essentially no connection between their corresponding pads since there will at least be one reverse biased junction to prevent current from flowing. For the collector pad

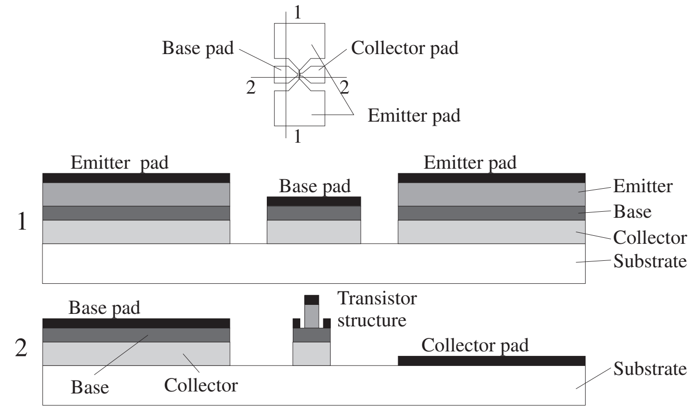

Figure 2.2: Schematic picture of how the pads are put on the substrate. The thickness of the different layers is strongly exaggerated for clarity. The numbers indicate the different cross sections.

there can possibly be a shunting load to ground as the substrate can be mounted on a grounded carrier. The deviation in the measured phase value, as seen in Fig. 2.3 a, from that of an ideal open structure (corresponding to a single point at magnitude one and phase zero) can be attributed to the very short transmission line, about 50-100 μm, that actually exist from the probe connector to the physical open structure. As can be seen in Fig. 2.1, an open structure corresponds to a pad structure where the metallization for the inner transistor (see Fig. 2.1) has been omitted. This deviation has been verified using a method of moments simulator (Momentum from HP), see Fig. 2.3c. A distance of 100 μm would correspond to a phase shift of approximately 25° (30°) at 40 (50) GHz in the Smith chart which compares well with an analytical calculation of the phase shift assuming a coplanar waveguide. The dielectric constant is then assumed to be the arithmetic mean of the dielectric constant in air and the one of Silicon. In the model, these transmission lines have been included as coplanar waveguides (CPW) in the base- and collector lead, assuming a pad configuration as in Fig. 2.1. Had there been any coupling to the substrate, this would have appeared as a measured result closer to a short-circuit. The coupling to the substrate should however be further studied if material with lower resistivity is to be used, e.g. 10 Ωcm which is more common material for regular fabrication of Si devices [12]. The doping can there create shunting parasitics who drastically affect performance in a degrading manner. As an example, a pad size of 100x100μm^2 laying on top of a 1 μm oxide as insulator could give rise to a capacitance of 345 fF. The resulting S_{11} of such a capacitance connected immediately to ground can be seen in Fig. 2.3d. This shunting effect can however be decreased with a thicker insulator. One method is to put the pads on a 10 μm thick polyamide. With high ohmic substrates there can also be a possibility of bulk currents due to a large space charge region (SCR) between base and collector in which generation-recombination (GR) processes can occur. At the outer end of each node (see Fig. 2.4) is an RC parallel circuit, e.g. R_{Bprobe} in parallel with $C_{RFshunt}$ for the base node, connected to model the effects caused by the connection between the measurement equipment and the device. At DC- measurements, the resistive load can have an impact whereas at S-parameter measurements the calibration process assures that measurement data present the result at the probe tips. With a good measurement set-up consisting of high quality cables, these resistances can usually be neglected.

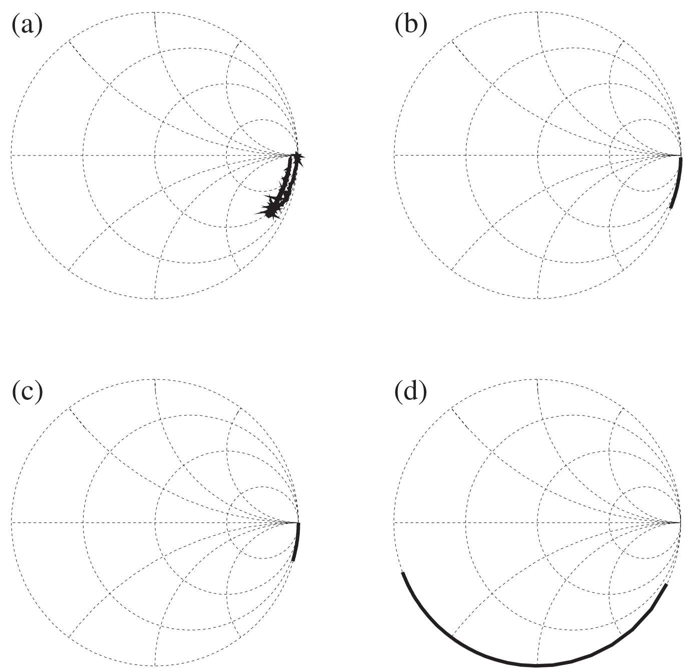

Figure 2.3: Measured and calculated S_{11} *for different circuits. (a) measured data for two 'open' test structures: lossy (non-ideal) structure with a reflection coefficient (radius) smaller than unity for all frequencies and an almost ideal open structure with a reflection coefficient close to unity, (b) calculated data for a short transmission line terminated in a high impedance (open), (c) calculated data for a 2D pad-structure using the Momentum (from HP) simulator, (d) calculated data for a short transmission line in parallel with a 345 fF capacitance (open with connection via the substrate to ground). Frequency is from 1 to 50 GHz except for the measurement of the non-ideal open structure where the frequency is from 1 to 40 GHz.*

In some measurements of test structures, losses can be noticed as a magnitude of S_{11} and S_{22} which is smaller than unity, see Fig. 2.3 (a). These can generally not be attributed to losses in the transmission lines as these are fabricated on high impedance substrate. Losses physically related to the area of the actual transistor is then more likely as this part of the wafer undergoes more processing steps unprotected. A tentative approach at modeling these losses has been done with the shunting and series resistances nearest to the actual transistor (R_{BEloss}, R_{CEloss}, R_{Eloss} and R_{Closs} respectively). The capacitances and inductances related to these resistors ($C_{DCblock}$ and $L_{DCshunt}$ respectively) are included to prevent these lossy effects to have an impact on the DC performance. The resistance in the base-lead (which should be called R_{Bloss}) has been omitted since the current approach has from experience been sufficient for modeling the lossy test circuits. The shunting resistances (R_{BEloss} and R_{CEloss} respectively) reflect the common emitter configuration of the pad structure. Depending on device fabrication, the losses can vary and often the lossy effects need not to be included. Thus the redundancy of resistors in each terminal connection can be explained with handling different situations. For modeling the different test structures (open, short and through), the nodes 'Base', 'Collector' and 'Emitter' in Fig. 2.4 are connected differently. For open, all nodes are disconnected. For short all nodes are connected to each other and for through, 'Base' and 'Collector' are connected to each other while 'Emitter' is disconnected.

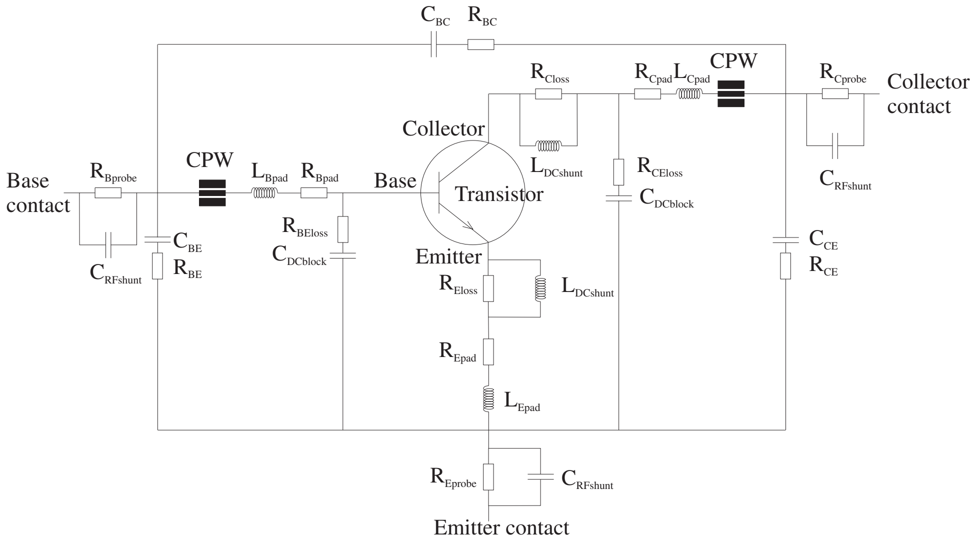

Figure 2.4: Schematic of the embedding shell. The transistor symbol depicts where the transistor is to be connected. The components 'CPW' are coplanar transmission lines.

2.3.3 The extrinsic shell

The extrinsic part of the transistor, see Fig. 2.5, form the surrounding shell around the intrinsic transistor. In a general 'collector down' design this means that the extrinsic base-collector junction and the distributed base connection is accounted for here. In addition, the contact resistances for the three terminals are accounted for. In the base lead, a metal-semiconductor resistance (R_{Bcont}) in parallel with a depletion region capacitance (C_{Bshunt}) connects the metal pad with the base layer. Immediately under this contact lies physically the extrinsic part of the collector which has been modeled with a diode (i_{BCext}) in parallel with a shunting capacitance (C_{BCext}) and finally a series resistance to account for the undepleted part of the collector (R_{BCext}). In the simulator, the sub-circuit consisting of C_{BCext}, i_{BCext} and R_{BCext} are substituted with a diode element taking these three components into account. The base sheet leading from the contact into the intrinsic base is modeled with a single resistance (R_{Blead}). Using a lumped element works well at high base doping. The voltage drop along the base sheet inside the intrinsic transistor is then very small and thus also the variation of the injection currents due to variation in base-emitter voltage.

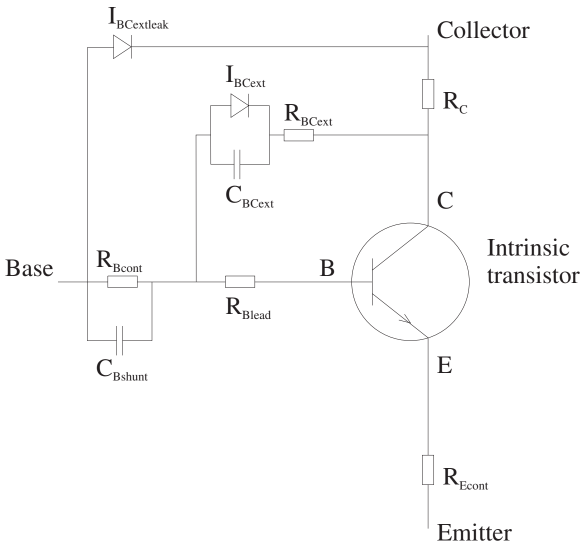

Figure 2.5: Schematic of how the extrinsic part of the transistor has been modeled. The transistor symbol shows the connection to the intrinsic device.

Care should however be taken when modeling transistors with low base doping (e.g. pure Si). A rough estimate of minimal base doping where the voltage drop can be neglected can be made assuming that the voltage drop between any two points inside the intrinsic transistor should be lower than $V_T = \frac{k_B T}{q}$ which corresponds to a variation in collector current of approximately the natural exponent (e), see eq. 2.2 and 2.3. Assuming a finger-shaped intrinsic transistor (see Fig. 2.1), a minimum base doping (N_B) can be defined as:

$$N_B > \frac{L_F I_B}{2 * 2qV_T W_B W_F \mu_{hBtrans}} \tag{2.1}$$

where L_F is the length (in the direction of the base current flow) of the intrinsic emitter finger from one side to the other and W_F is the width of the finger, compare with the similar definition in an FET. $\mu_{hBtrans}$ is the hole mobility parallel to the base layer. The other terms are common definitions. The base is also assumed to be contacted from both sides of the finger (see Fig. 1.4), thus causing the current to be splitted and the distance for the current to flow to be half of L_F. For a device with $\frac{L_F}{W_F}$=0.05, $W_B = 100 * 10^{-7}$ cm, $\mu_{hBtrans}$=125 cm^{2}V^{-1}s^{-1} [13] and I_B=10 μA, the base doping must thus be larger than:

$$N_B > \frac{0.05 * 10 * 10^{-6}}{2 * 2 * 1.602 * 10^{-19} * 0.0259 * 100 * 10^{-7} * 125}$$

$> 2.4 * 10^{16}$ cm^{-3}.

It should be remembered that this is a lower limit and that L_F can be considerably bigger (caused, e.g., by contacting from only one side). For the contacting of the collector and emitter layers, there are also resistances (R_{Econt} and R_C respectively). The value of the collector contact resistivity is not so critical since the buried sub-collector facilitates a large contacting area and the device performance is not very much affected by the value of the resulting contact resistance as long as it is small compared to resistances outside the device. The resistance of the sub-collector is also included in R_C, thus the index 'C' instead of 'C_{cont}'. The actual resistance of the sub-collector is difficult to extract due to the position in the circuit and a value of 5 Ω has been used as a typical value [14]. The emitter contact resistance is more critical as a voltage drop over this component immediately affects the injection over the base-emitter junction.

In addition to the diode modeling the extrinsic part of the base-collector junction there is also a diode ($i_{BCextleak}$) to account for the possible leakage currents occurring on the surfaces of the mesa structure between the base and collector contact, see Fig. 1.3. The usage of a diode implies a current flowing in only one direction which does not have to be the case for this current. The diode model element works however well for modeling the impact of this current on transistor behavior throughout the studied bias ranges.

2.3.4 The intrinsic shell

The intrinsic transistor is the most thoroughly modeled part and it consists of several different components to account for the different physical processes occurring. In each junction, two different diodes model the electron and hole injection respectively (i_{Ee} and i_{Eh} for injection in the base-emitter junction and i_{Ce} and i_{Ch} for injection in the base-collector). The reason for treating the two kinds of injections separately is due to their dependence on different energy band-gaps. The electron injection from the emitter and collector into the base is inversely proportional (through the intrinsic carrier concentration, n_i) to the exponential of the band-gap in the base through the following relation:

$$J_{0e} = \frac{qD_{eB}n_{iB}^2}{N_B W_B} \tag{2.2}$$

where n_i^2 is defined as:

$$n_{iB}^2 = N_{Cond} N_{Val} e^{\frac{-E_{gB}}{k_B T}} \tag{2.3}$$

q, D_{eB} and W_B can be considered as independent of T whereas $N_{Cond} * N_{Val}$ is proportional to T^3. This gives the band-gap dependence of the electron injection. Similar expressions are valid for the hole injection from the base into the emitter and the collector. The conduction band throughout the transistor has been assumed to be continuous thus not creating any band-spikes (existing for example in abrupt AlGaAs/GaAs junctions). Heavy doping could have an effect on the conduction band continuity [15], but a proper fabrication process seem to make the impact of these effects small. The ideality factor of the collector current is very close to unity in Gummel measurements which would not be the case with a band spike occurring [16]. A very small band offset can not be excluded, but it can not be identified as a distinct effect and is thus not included in the model.

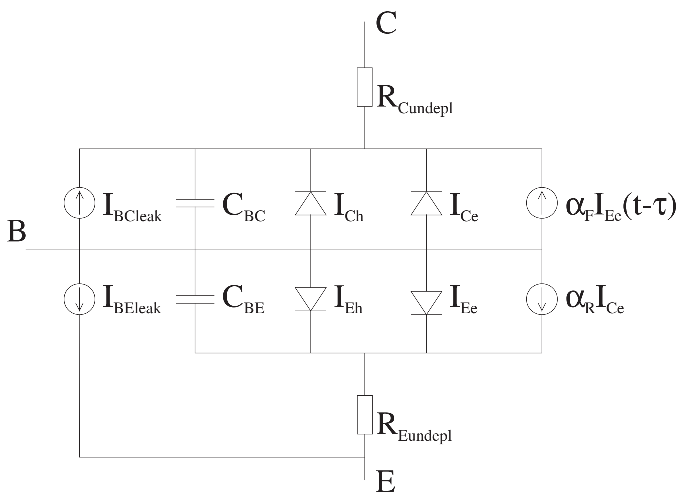

Figure 2.6: Schematic of how the intrinsic part of the transistor has been modeled. The terminals C, B and E denotes the points where the intrinsic part connects to the extrinsic part (see Fig. 2.5).

Due to the temperature dependence in the exponential, eq. 2.2 is strongly temperature dependent. Since there are different energy band-gaps in the emitter and the base, the saturation currents and thus also the injection currents will vary differently with temperature. By modeling the currents in this physics related way, the electron current is readily available and since this is the only part that is swept through the base to the collector, the current generator corresponding to this mechanism only need to account for an electron loss due to recombination in the base layer which, compared to the exponential term in eq. 2.2, can be considered fairly constant with respect to temperature. In the approach where both injections are considered in the same diode, a more complex expression for the then temperature dependent a for the current generators, see Fig. 2.6, needs to be defined (which also obscures the physical connection). The two capacitors (C_{BE} and C_{BC} for the base-emitter junction and the base-collector junction respectively) account for the junction capacitance and are based on the expression used in SPICE [17]. During normal operation of the HBT however, the current density in the collector SCR can become so high that the injected majority carriers compensate the charge of the ionized impurity atoms (note that local charge neutrality does not exist in the SCR). In this case more impurity atoms need to be ionized in order to keep global charge neutrality which has an expanding SCR as result. This means that the junction capacitance decreases and also the collector transit time should increase. So far, only modeling of the collector capacitance lowering has been included whereas the transit time change not has been possible to implement in the simulator due to limitations in the SDD. In series with the current generators and the capacitances are the resistances that account for the undepleted regions of the collector ($R_{Cundepl}$) and emitter ($R_{Eundepl}$), respectively. The resistance in the collector will thus vary as the collector SCR varies. Since the depletion region of the emitter is extremely small during all operation, this resistance could be assumed to be constant, but for completeness also the modulation of this value is modeled. Where computing time is a key figure, this part should be possible to remove from the SDD. In each junction is also one more current generator which is voltage dependent (I_{LBE} and I_{LBC} respectively). These are modeling the leakage currents occurring. They can be related to different processes such as surface currents on mesa type devices and high injection effects causing a higher recombination in the base. Their parameter values have not been calculated as they vary between devices in a very unpredictable way, probably due to an incomplete passivation process of the devices. The empirical approach can partly be justified by that the need for these generators hopefully goes away in devices where the technology has reached a more mature stage. At the moment, the connection of the base-emitter current generator suggests to only account for surface currents as it is connected past the intrinsic bulk resistance. In the present implementation the aim has been to use explicit expressions for calculating the various parameters. This has led to that the capacitance and resistance in each side of the base (e.g. C_{BC} and $R_{Cundepl}$ for the collector side) have been calculated using junction voltages rather than using the resulting currents. In doing so, effects related to the currents (e.g. expansion of the SCR as described above) are very difficult to model in a correct way. With a new approach where the currents (primarily the collector current) are included implicitly in the simulation, a more straightforward implementation of, e.g., the capacitance could be realized. This would make the value at the same time accessible for other elements in the intrinsic device. The technique of using implicitly defined currents inside SDDs is well described in [15].

2.4 Implementation of the model into a commercial simulator

The model has been implemented in Microwave Design System (MDS) from Hewlett Packard which is a fairly complex system for design of microwave components. The essential parts are a 2.5D simulator (Momentum) for passive, distributed circuits and a simulator with SPICE like environment (DCS) for lumped element circuits. DCS also contains the SDD which facilitates modeling of currents and voltages through both explicit and implicit equations. These equations are also treated in both the frequency and time domain which makes the implementation of, e.g., time delays very straightforward. Some limitations exist however in the SDD.

2.4.1 Description of the symbolically defined device

The SDD can be seen as a tool for defining the relationship between voltage and current between two nodes. These nodes are considered to be one port. Each port has two state variables: voltage drop between the two nodes (called _Vn) and current flowing from one node to the other (called _In). For each port either an explicit expression for the current, _In where n is the index for the port, or an implicit equation relating _In to any other state variable (to any _Im and to any _Vm) can be defined. These are evaluated in both the time and frequency domain in one of the following manners:

For explicitly defined currents:

$$V(\omega) \underset{1}{\overset{FFT^{-1}}{\Longrightarrow}} v(t) \underset{2}{\overset{f}{\Longrightarrow}} \hat{\imath}(t) \underset{3}{\overset{FFT}{\Longrightarrow}} \hat{I}(\omega) \underset{4}{\overset{weighting}{\Longrightarrow}} I(\omega) \tag{2.4}$$

The variables are column vectors where the elements correspond to the individual ports. In step 1 an inverse Fourier transform of the voltage input spectrum over all connected ports is done. Their corresponding values in the time domain are thus available in all equations. At step 2 this can be used for explicitly calculating a value, also incorporating non-linear effects, for the current in the time domain. Important to note however, is that evaluation is not point-wise individual. The whole time sweep is evaluated at one time which makes functions relating values at different time points impossible. This is a drawback as, e.g., time varying time delays occurring in the base-collector SCR due to the strong variation in SCR width during big voltage swings thus are not possible to implement. At the moment this is not a big constraint since the added delay in the collector in relation to the whole delay through the transistor is fairly small, but in high power applications where a long low doped collector is used, the effect should be studied further. The current waveform is in step 3 transformed into the frequency domain where in step 4 it is multiplied with a frequency dependent function. Different operators in the time domain can thus be implemented, e.g., a time derivative which equals to jω.

For implicitly defined currents the steps are similar, however somewhat more complicated. Instead of using only the voltage spectrums as input, a vector consisting of both the voltage and current spectrums,

$$X(\omega) = \begin{bmatrix} V(\omega) \\ I(\omega) \end{bmatrix} \tag{2.5}$$

is used and instead of explicitly calculating a value for I(ω), the solver tries to minimize an error, E(ω):

$$X(\omega) \underset{1}{\overset{FFT^{-1}}{\Longrightarrow}} x(t) \underset{2}{\overset{f}{\Longrightarrow}} \hat{e}(t) \underset{3}{\overset{FFT}{\Longrightarrow}} \hat{E}(\omega) \underset{4}{\overset{weighting}{\Longrightarrow}} E(\omega) \tag{2.6}$$

In step 1 an inverse Fourier transform of the input spectrum (X) is done. At step 2, a function operates on the time series vector which yields a result e(t). This is in step 3 transformed to the frequency domain where in step 4 a weighting function as described in the explicit case is multiplied to the spectrum. The resulting spectrum is an error which the solver tries to find spectrums of X(ω) so that E(ω)=0.

2.5 Equations for finding the circuit simulation parameters

In the following section the equations used for finding parameter values to the lumped elements in the embedding shells and the actual currents (and for some cases, voltages) occurring in the SDD will be defined. The order is done from outer components going towards the intrinsic transistor. To point out relative importance, calculations of typical values have been done. When nothing else is mentioned, the values shown in Table 2.1 are used.

Table 2.1: Nominal values used in calculations.

parameter	value	parameter	value	parameter	value
W_E[cm]	$.070 * 10^{-4}$	W_B[cm]	$.030 * 10^{-4}$	W_C[cm]	$.300 * 10^{-4}$
N_E[cm^{-3}]	$2 * 10^{18}$	N_B[cm^{-3}]	$1 * 10^{20}$	N_C[cm^{-3}]	$5 * 10^{16}$
$\varepsilon_E/\varepsilon_0$	11.7	$\varepsilon_B/\varepsilon_0$	13.1	$\varepsilon_C/\varepsilon_0$	11.7
A_E[cm^2]	$20 * 10^{-8}$			A_C[cm^2]	$40 * 10^{-8}$
A_{Econt}[cm^2]	$20 * 10^{-8}$	x_{Ge}	0.30		
W_F[cm]	$20 * 10^{-4}$	T_0 [K]	293		

Some terms considering fundamental physics of the semiconductor are defined in the section following this.

2.5.1 The embedding shell

In the embedding shell all parameter values are directly extracted from measurements and has thus no expressions related to them. As mentioned before this is consistent with the model since these parts to a very low degree scale with dimensions of the actual transistor, see Fig. 2.1. Method for extraction of the values will be described in a later section.

2.5.2 The extrinsic shell

The extrinsic shell consists of the components connecting the intrinsic terminals of the transistor to the pads as described before. The metal base-layer contact (R_{Bcont}) is calculated using:

$$R_{Bcont} = \frac{\rho_B}{A_B} \tag{2.7}$$

where A_B has been defined as ($A_C - A_{\mathrm{Econt}}$) which corresponds to the base area outside the intrinsic transistor. ρ_B is the contact resistivity between metal and the heavily doped base layer. A_C is the total collector area defined by the perimeter of the base metal contact inside the etched groove. A_{Econt} is the area defined by the emitter-finger metallization. The contact resistivity can vary, but is difficult to extract unless it for some reason is high. A conservative initial value which has been chosen for the contact resistivity is ρ_B=$5 * 10^{-6}$ $\Omega\mathrm{cm}^2$ [13]. The emitter contact (A_{Econt}) can be well defined through the lithography (verified through SEM) and the value given from the design can be used as a good initial value. The collector area which is defined by a very deep etch can vary somewhat and need also to be extracted. A calculated value of R_{Bcont} is 25 Ω. In parallel with the resistance is a shunting capacitance. This was first inserted when it was noticed that the base contact resistance did not have a big impact on RF-parameters and it should thus be shunted. The origin could, in a poor contact, be related to the metal-semiconductor interface as [3]:

$$C_{Bshunt} = \sqrt{\frac{q\varepsilon_B N_B}{2V_j}} A_B \tag{2.8}$$

=0.6 pF, assuming V_j=1 V.

The assumption of V_j is not fully correct, but the impact on C_{Bshunt} from a variation in V_j is small. V_j itself can roughly vary between 0.8 V and 1.1 V, assuming a base of heavily doped Germanium or Silicon, respectively. The extrinsic diode, accounting for the pn-junction outside the intrinsic base-collector junction has a saturation current calculated as [3]:

$$I_{BCext00} = q(A_C - A_{Econt})\left(\frac{D_{eB}n_{iB}^2}{W_B N_B}\frac{D_{hC}n_{iC}^2}{(W_C - X_{jC00})N_C}\right) \tag{2.9}$$

where

$$X_{jC00} = \sqrt{\frac{2n_B \varepsilon_B \varepsilon_C J_{jC00}}{qN_C(\varepsilon_B N_B + \varepsilon_C N_C)}} \tag{2.10}$$

Only steady state thermal dependence is included. Since the current in the normally reverse biased junction is very small, this does not create any big errors. The bias dependent capacitance is the important component and this can be adequately modeled with the expression for the junction capacitance for a zero bias condition which the simulator then uses to calculate the bias dependent capacitance.

$$C_{BCext00} = \frac{\varepsilon_C A_C}{X_{jC00}} \tag{2.11}$$

In series with the capacitance is also the resistance to account for the undepleted region of the collector. The expression for this resistance is [3]:

$$R_{BCext} = \frac{W_C - X_{jC00}\sqrt{1 - \frac{V_{BC0}}{V_{jC00}}}}{q\mu_{eC0}N_C A_C} \tag{2.12}$$

All individual parameters has to be given as fixed values since the lumped elements in this part of the simulator cannot be updated throughout the simulation, therefore the added '0' as a suffix. In order to get a reasonable value, the base-collector voltage (V_{BC0}) is set to -1 V which corresponds to a collector-emitter voltage of about 2 V in an ordinary bias condition. The capacitance is not evaluated only at this voltage since the simulator automatically treats this part as bias dependent as it is part of the diode model element.

The base sheet resistance (R_{Blead}) is calculated as:

$$R_{Blead} = \frac{L_B}{2qW_F\mu_{hBtrans}\frac{W_B}{2}N_B} \tag{2.13}$$

=12.5 Ω assuming L_B=1.5 μm which is an effective length of the resistive sheet. The open distance between the base metallization and the intrinsic base is less than 1.5 μm, but to account for the distributed behavior occurring under the base contact (all current does not float in the infinitesimally narrow part that is the closest to the intrinsic base, see Fig. 1.4) a higher value has been chosen. Metallization for the base contact has been assumed on both sides of the emitter finger. The outside base layer under the metallization is assumed to have approximately half the thickness of the intrinsic base layer due to over etch [18]. The emitter contact resistance (R_{Econt}) is calculated similarly to the base contact resistance:

$$R_{Econt} = \frac{\rho_E}{A_{Econt}} \tag{2.14}$$

=25 Ω

The contact resistivity can vary and need to be extracted. An initial value which seems to be reproducible and conservative is $5 * 10^{-6}$ Ωcm^2 [13]. Extraction is however necessary since the impact on device behavior from this resistance is big at high currents (see later section describing the fitting of parameters towards the Gummel plot).

The collector resistance (R_C) includes both the contact resistance and the resistance in the sub-collector lead. These are difficult to distinguish between each other, but from a modeling point of view R_C does not play an important part. Neither f_t nor $f_{max}$is heavily affected by its value and further investigations regarding the partitioning of R_C has thus not been done. Choosing an initial value of approximately 5 Ω for small devices has been practically sufficient [14] and a possible variation, to fit a plot of I_C vs. V_{CE}, can be done.

2.5.3 The intrinsic shell

In this part all implementation has been done using the SDD as described above. Thus the expressions need to describe the actual currents and, possibly, voltages. To achieve convergence during the simulations, it is very important to have somewhat bounded and differentiable functions, preferably also with a continuous derivative [15]. A special expression for the exponential function has thus been defined which is upwards limited by a linear function and has a continuous derivative:

$$\mathrm{expon}(\_value) = \begin{cases} e^k * (\_value - k - 1) & \_value > k \\ e^{\_value} & \_value \leq k \end{cases} \tag{2.15}$$

where k is chosen to 69 ($e^{69} \approx 10^{30}$) to allow sufficiently high values in the calculations. The current through the two diodes in the base-emitter junction are thus calculated using:

$$i_{Ee} = I_{Ee0} K_{IEe} \left(\mathrm{expon} \left[\frac{v_{BE}}{V_T n_F} \right] - 1 \right) \tag{2.16}$$

$$I_{Ee0} = \frac{q A_E D_{eB} n_{iB}^2}{W_B N_B} \tag{2.17}$$

$$i_{Eh} = I_{Eh0} K_{IEh} \left(\mathrm{expon} \left[\frac{v_{BE}}{V_T n_F} \right] - 1 \right) \tag{2.18}$$

$$I_{Eh0} = \frac{q A_E D_{hE} n_{iE}^2}{W_E N_E} \tag{2.19}$$

In the base-collector junction, the currents are calculated using:

$$i_{Ce} = I_{Ce0} K_{ICe} \left(\mathrm{expon} \left[\frac{v_{BC}}{V_T n_R} \right] - 1 \right) \tag{2.20}$$

$$I_{Ce0} = \frac{q A_E D_{eB} n_{iB}^2}{W_B N_B} \tag{2.21}$$

$$i_{Ch} = I_{Ch0} K_{ICh} \left(\text{expon} \left[\frac{v_{BC}}{V_T n_R} \right] - 1 \right) \tag{2.22}$$

$$I_{Ch0} = \frac{q A_E D_{hC} n_{iC}^2}{W_C N_C} \tag{2.23}$$

It is here noticeable that the emitter area is used to define the collector current. This comes from the definition of the intrinsic transistor having the area of the base-emitter interface. The constants K_{IEe}, K_{IEh}, K_{ICe} and K_{ICh} are included to facilitate a possible reduction of the different currents. Due to lack of an accurate model for the band-gap narrowing at high doping levels and high Germanium concentrations, the value of the intrinsic carrier concentration in the base can be slightly overestimated [19] (too strong band-gap narrowing) which results in a slightly too big value of i_{Ee} and i_{Ce}. Thus these currents could be multiplied by a factor ranging from 1/3 to 1/2. After injection of electrons into the base from the emitter, these charges are swept through the base to the opposite SCR, i.e., the base-collector SCR. A slight decrease due to base recombination is accounted for by multiplying the current with the base transport factor (α_F), which is very close to unity (negligible base recombination). The term is fed by the user at the time of simulation. In the base-collector SCR the electrons can reach high enough energy to knock out more electrons when colliding with the lattice which can cause an avalanche multiplication. The multiplication factor is defined as [20]:

$$M_C = \frac{1}{1 - \left| \frac{V_{BC}}{V_{Cbreak}} \right|^4} \tag{2.24}$$

and is also added to the expression. To account for the diffusion delay through the base (τ_B) and the drift delay through the base-collector SCR (τ_C), a multiplication term (φ) for the collector current generator inside the SDD is introduced in the frequency domain as [21]:

$$\varphi = \frac{\sin(\omega \tau)}{\omega \tau} e^{-j\omega\tau} \tag{2.25}$$

$$\tau = \tau_C + 0.22 * \tau_B + \tau_F \tag{2.26}$$

which, at small ωt, corresponds to a frequency dependent phase shift. The τ_F is an adjusting parameter to make simulations at high frequencies fit with measurements. Both τ_C and τ_B are difficult to calculate exactly due to the inherent inaccuracy lying in the technological parameters. The variable ω is created by the simulator at runtime and corresponds to the angular frequency that is calculated. This gives some possibility of controlling parameters in the frequency domain like introducing a delay as a frequency dependent phase shift. Relating values calculated by the simulator between different frequency points, e.g., $I1(\omega) = f(I2(\omega + \omega_0)$, is not possible more than for very simple relations as the expressions are defined in the time domain. Relating values calculated by the simulator between different time points, e.g., $I1(t) = f(I2(t + t0))$, is not possible due to limitations in the software which is the reason for implementing the delay in the frequency domain.

Calculation of the currents through the two junction capacitances is done by using the SPICE model [17, 15]. The charge build-up on the edges of the SCR surfaces are calculated as:

$$Q = \begin{cases} Q_r(v), & v < \alpha V_j \\ Q_f(v), & v \geq \alpha V_j \end{cases} \tag{2.27}$$

where

$$Q_r(v) = -2C_{j0}\sqrt{V_j(V_j - v)} \tag{2.28}$$

$$Q_f(v) = \frac{C_{j0}}{\sqrt{1-\alpha}}\left(v - \alpha V_j + \frac{(v - \alpha V_j)^2}{4V_j(1-\alpha)}\right) + Q_r(\alpha V_j) \tag{2.29}$$

Here, V_j is the built-in voltage, v is the applied voltage and C_{j0} is the junction capacitance at zero bias ($v = 0$). Two regions have been chosen to avoid unrealistic values when applied voltage reaches the built-in voltage. These regions are defined by the constant α (not related to the current transport factor defined for the current generators). The reason for not using the classical definition of a depletion capacitance, having the following expression:

$$C_j(v) = C_0\sqrt{\frac{V_j}{V_j - v}} \tag{2.30}$$

is that it reaches infinity when v=V_j and the corresponding charge build-up is then not defined. This is thus avoided by having an expression identical to the classical at reverse bias and to a forward bias voltage αV_j from which point a linear continuation is made. This approach is very suitable for the SDD since the expression for the charge build-up can be evaluated in the time domain and later multiplied by $j\omega$ in the frequency domain which yields the spectrum of the time derivative, this being the displacement current. The calculations for both junctions use eq. 2.26. Since these capacitances only accounts for the intrinsic parts of the transistor, the emitter area is used when calculating the individual C_0 for both junctions. In the base-emitter junction, a diffusion capacitance has been included to account for the charge build-up change in the base due to the diffusion time. The charge build-up is calculated as:

$$Q = i_{Ee}\tau_B \tag{2.31}$$

The time derivative of this charge is then calculated as described above. Further on the effect of charge compensation as discussed earlier has been implemented partially for the base-collector junction. Assuming a constant doping in the collector and an evenly distributed current, the widening of the SCR can be expressed as:

$$\frac{L'}{L} = \frac{1}{1 - \frac{I_C}{qn_C A_E v_s}} \tag{2.32}$$

Where I_C is collector current and v_s (=10^7 cm/s) is the electron saturation velocity. For low currents, the expansion is very low, but at already at a current of 8 mA, the charge compensation has caused the SCR to expand by a factor of two. This is only valid for the low doped collector and as soon as the SCR reaches the sub-collector, charge compensation has no real effect. The inclusion of this effect has only been considered in the intrinsic part of the collector whereas one could intuitively expect that the electrons, from the Coulomb force, would spread through the whole of the collector. Calculations made using FEM tools (Atlas from Silvaco) show however that for the thin collectors which so far have been treated, almost all current flows immediately under the interface defining the intrinsic transistor. A problem with the implementation of the charge compensation effect is the difficulty of finding the collector current flowing through the SCR and thus causing charge compensation; displacement currents do not affect. The current has also to be found during the simulation. So far, different attempts using the complete collector current have been used which works fairly well with S-parameter simulations since the RF-part then is infinitesimal, thus not adding any displacement current in the simulation. Care must however be taken when using the collector current during large-signal RF simulations since the displacement current then can become a substantial part of the total current. Different tentative approaches to solve this problem in a direct way have been employed, but none has been quite successful. An indirect way would be to use the calculated value of the depletion region width which is used for other components, see below, and with this calculate a direct parallel plate capacitance which is multiplied with the time derivative of the applied voltage (further discussed in ref. [15], appendix A). This necessitates however a free port for evaluating the time derivative of the applied voltage in each time-point which consumes computer power and it is not quite clear how big impact this capacitance has on overall performance. Assuming a base-collector built-in voltage of 1 V, the whole collector is fully depleted at base-collector voltage of -2.5 V without any current flow. If a collector current of 6 mA is injected, the whole junction is depleted already at zero bias. Possibly, applications with low reverse base-collector voltage and high collector currents could be affected. A frequency doubler designed with the developed model could be an example of a case where this bias occurs in combination with large-signal RF [22]. Calculated data for frequency doubler using this model compared however well with measured data.

In addition to the current generators that already have been discussed, there are also generators to account for the non-idealities in the base current appearing as a base current not being parallel to the collector current in a Gummel plot, see Fig. 2.7. Since these current generators are based on purely empirical data, the primary objective has been to make them suitable for fitting. In addition to a voltage dependence, they are also depending on junction temperature which is very important for a correct modeling of the temperature dependency of the whole device, see Fig. 2.8. What is important to point out here is that these generators do not stand for the total temperature modeling of the device which in that case would make this model unphysical. However, for the overall behavior, this part need also a correct thermal modeling. In Gummel plots of an ordinary studied HBT, three essential regions of the base currents can be distinguished, see Fig. 2.7. The Gummel plot is a graph of both base and collector current versus base-emitter voltage for a constant base-collector voltage (usually set to zero). Collector and emitter can also be interchanged for a reverse Gummel measurement.

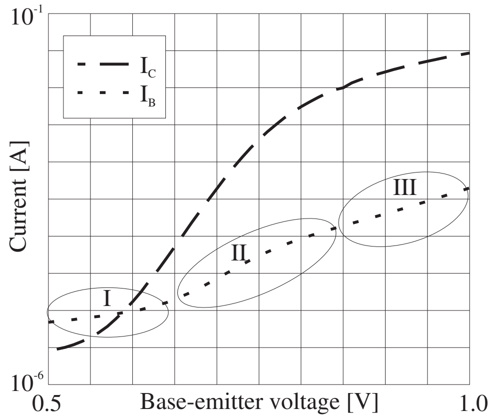

Figure 2.7: A Gummel plot of a typical HBT, showing the three important regions of the base current.

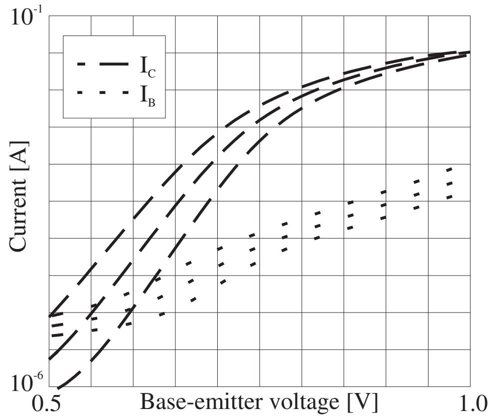

Figure 2.8: Gummel plot at three different junction temperatures (293K, 323K and 373K respectively) for a typical HBT. Increasing currents correspond to increasing temperature.

At low junction voltages a current with a very weak slope is found, see region I, Fig. 2.7. This shows dependence on light and can thus be attributed to generation processes. The following region, region II in Fig. 2.7, exhibit a more ideal behavior of the base current having an ideality factor between 1 and 2, indicating generation- recombination processes [3]. In this region essentially all biasing is made (corresponding to collector currents between 1 and 10 mA for the studied devices). The third region, region III in Fig. 2.7, exhibit high injection effects where the 'roll off' in the base current due to the voltage drop over the emitter-lead resistance is not following the collector (emitter) current which could be expected that it would. Instead it is steadily increasing. A possible explanation could lie inherently in how the Gummel measurement is made, namely in that the intrinsic base-collector junction becomes forward biased due to the voltage drop over the collector resistance. The impact from the collector resistance is however a much stronger effect than the measured one and it can thus be clearly distinguished (see Fig. 2.9).

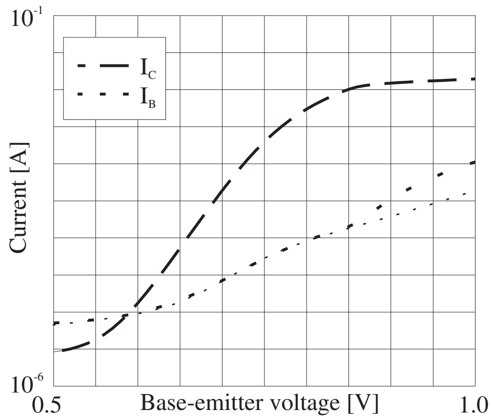

Figure 2.9: Example of a Gummel plot in which the base-collector junction has been forward biased due to the voltage drop over the collector-lead resistance. The thinner curve shows the base current when the impact from the collector-lead resistance is negligible.

The approach to model these additional parts of the base current has thus been empirical with an emphasis on facilitating easy and accurate fitting. For this reason the current generator (I_{LBE}) is decomposed into three expressions; each defining one of the above discussed regions. The expression for one of these parts is:

$$I_m(V) = J_{Em} A_E \text{expon} \left(\frac{V - V_{offset_m}}{V_T n_m} + \left[\frac{V_{therm_m}}{V_T} - \frac{V_{therm_m}}{V_{T0}} \right] \right) \tag{2.33}$$

where m=1,2 or 3. V_{offset} indicates the voltage point in the Gummel plot where the different parameters are extracted. J_E, n and V_{therm} corresponds to the current density, ideality factor and thermal dependence respectively in this voltage point. The term V_{T0} is set to the thermal voltage of the temperature where the non-thermally dependent parts are extracted. The term V_{offset} is not necessarily needed since it is possible to extract from zero voltage, the resulting extraction procedure becomes however more difficult since small variations of the terms in the exponential have a very strong impact. Depending on how the base current looks in the Gummel plot, these currents are combined differently. Usually a sum of the current in the low and intermediate voltage is performed, having the current in the high voltage region as an upper limit. Since they are one component of the base current, their impact can be slightly obscured by the hole back-injection which is the reason for the somewhat strange approach of using one current as a limiter. A physical explanation for this is not quite obvious, but a further investigation should then be concentrated on the high- current regime where the inaccuracy more likely can be attributed to an incomplete physical modeling of the intrinsic transistor, i.e., the observed effects do not necessarily disappear with an improved technology. It should however be noted that the high-current regime occur at high current densities ($J > 5 * 10^4 - 1 * 10^5$ A/cm^2) and it is questionable whether the device should be operated there. As can be seen in Fig. 2.7, the collector current exhibits a nearly ideal behavior with an ideality constant less than 1.05 in the region where the impact from the emitter-lead resistance is negligible (approximately for the base-emitter voltage corresponding to region II of the base current, see Fig. 2.7). The current generator in the base-collector junction (I_{LBC}) has so far not been used as leakage currents occurring on the surface of the device are accounted for by $I_{BCextleak}$.

The value of the resistance in the undepleted regions of the collector and emitter are calculated using:

$$R_{Cundepl} = \frac{W_C - X_{jC}}{q\mu_{eC} N_C A_E} \tag{2.34}$$

$$R_{Eundepl} = \frac{W_E - X_{jE}}{q\mu_{eE} N_E A_E} \tag{2.35}$$

where X_{jC} and X_{jE} are the width of the depletion regions in the collector and the emitter respectively. They use the common expression for space charge region as:

$$X_j = X_{j0}\sqrt{1 - \frac{V}{V_j}} \tag{2.36}$$

$$X_{j0} = \sqrt{\frac{2\varepsilon V_j}{qN}} \tag{2.37}$$

where ε, V_j, V and N are the dielectric constant, built-in voltage, applied voltage and the doping respectively in the considered SCR. This assumes a base doping that is at least one order of magnitude higher than the collector and emitter which is often the case. The addition in the expression to account for a lower doped base (most important for the emitter-base SCR) is easily accomplished and have been done when so has been needed. Care must be taken that the SCR does not evaluate to a value beyond the thickness of the material or becomes negative. The previous happens at high reverse applied voltages and the latter at positive applied voltages above the built-in voltage. To implement these restrictions, a somewhat cumbersome approach needs to be taken. In the simulator, conditional expressions can be given as:

$$Result = \text{if (cond. statement) then } Expr1 \text{ else } Expr2 \text{ endif}$$

which means that *Result* is given the value of $Expr1$ if the conditional statement is valid and the value of $Expr2$ otherwise. However, there is an important limitation included: if either of the expressions evaluates to an erroneous result, e.g., sqrt(-1) for an expected real result, then the total result is unpredictable. Even if the expression to be used according to the conditional statement evaluates correctly, the result is not clear. For this reason, one must take extra care not to evaluate any expression to an undefined value. Therefore all expressions are evaluated to an unconditionally positive (or zero) value. Using the conditional statement, the region for the input parameters are known within each restriction and it is still possible to calculate the correct final result.

The resistances are implemented as separate ports in series with the collector and emitter junction respectively. To find the currents, the voltages can be immediately divided by the calculated resistance. For this reason, the undepleted region is not allowed to vanish, but is set to a minimum of 1% of the complete layer-width. The collector current is used for calculating the internal power dissipation which in turn yields the temperature rise of the junction. This means that a direct definition of the current would give circular references. One way of solving this is to have 'parallel' parameters calculated at a given junction temperature. The parameters affected are: $\mathrm{E_{gB}}$, $\mathrm{X_{jC0}}$, μ_{nC} and $\mathrm{V_{jC0}}$. At low power dissipations and low variation in temperatures this is sufficient. For the above chosen parameters, the resistance varies from 1.3 Ω to 1.7 Ω when changing the junction temperature from 300K to 350K, having a base-collector bias of -2V. Another way to calculate the current is to use the possibility of an implicit relation. Assuming that port 1 of the SDD is used for this calculation, the following statement is made:

$$\_V_1 - \_I_1 * R_{Cundepl} = 0 \tag{2.38}$$

which iterates the correct current during simulation and $\mathrm{R_{Cundepl}}$ can still be temperature dependent although _I1 in this case is used for calculating the internal power dissipation and thus also the temperature. This approach consumes however more computing power.

2.6 Expressions used in the equations

For the equations/expressions above, several parameters are needed that are related to device physics. These will be stated, in no specific order, here and further described. In several cases both an expression for pure Silicon and an expression for an alloy is given. These expressions should give identical results in the case of no Germanium in the alloy (x=0). There is however no point in having a more complex expression than necessary and thus the expressions considering the collector and the emitter assumes x=0, i.e., pure Silicon. The expressions for the alloy assumes a strained material; relaxed layers would cause a lattice mismatch which would render the transistor more or less useless and is therefore not interesting to consider in this respect.

2.6.1 Parameters related to the band-gap

In order to get a good modeling of the thermal effects, the band-gap need to be accurately accounted for since the impact, through the often exponential terms, is very big. The band-gap for the different layers are calculated accounting for thermal variation, band-gap contraction due to heavy doping and possible strain. The last is only made for the base layer. To calculate the band-gap, the width of the doping induced contraction is subtracted from the value of the undoped semiconductor band-gap. This is performed assuming a fixed temperature of 300K. Following, the temperature dependence is accounted for by multiplying the band-gap with a scaling factor which relates the band-gap of undoped silicon at the present temperature to the band-gap of undoped silicon at 300K.

The expression for the band-gap energy is thus [23, 24]:

$$E_g(T,x,N_X) = QE_g(T) * [E_{gX0}(x) - \Delta E_{gX}(N_X)] \tag{2.39}$$

$$E_{gX0}(x) = \begin{cases} 1.124, & X\ is\ C\ or\ E \\ 0.9646 * (1.165 - 0.75x), & X\ is\ B,\ x \leq 0.30 \end{cases} \tag{2.40}$$

$$\Delta E_{gX}(N_X) = E_1 * \left[\ln\left(\frac{N_X}{N_0}\right) + \sqrt{\ln\left(\frac{N_X}{N_0}\right)^2 + 0.5} \right] \tag{2.41}$$

$$QE_g(T) = \frac{1.1785 - 9.025 * 10^{-5} * T - 3.05 * 10^{-7} * T^2}{1.124}, \quad T \leq 170\ K \tag{2.42}$$

where X is C, B and E for collector, base and emitter respectively, E_1=0.009 eV and N_0=$1 * 10^{17}$ cm^{-3}. In Fig. 2.10, the effect of doping, temperature and alloy concentration can be seen. Different expressions for the alloying dependence of the band-gap exist [23, 24] and the one in [24] has been chosen to be consistent with the expressions for n_i in strained SiGe also found in [24]. The expression for the band-gap found in [24] gives a slightly higher estimation of the value of the band-gap (maximum 0.05 eV) than the one found in [23] and it can thus be expected that the real value is somewhere in between. For the Si/SiGe interface the whole band-gap offset has been assumed to occur in the valence band in the case of a strained alloy adjacent to pure Silicon as discussed earlier. This means no conduction band spike which occurs in e.g. AlGaAs/GaAs structures and there affects the electron injection. Possibly, a small offset could be occurring which then has been attributed to a slightly smaller device area or a different ideality constant of the device.

2.6.2 Intrinsic carrier concentration, n_i

The intrinsic carrier concentration is needed for the calculation of the saturation currents and is thus an important parameter. For pure Silicon the following expression

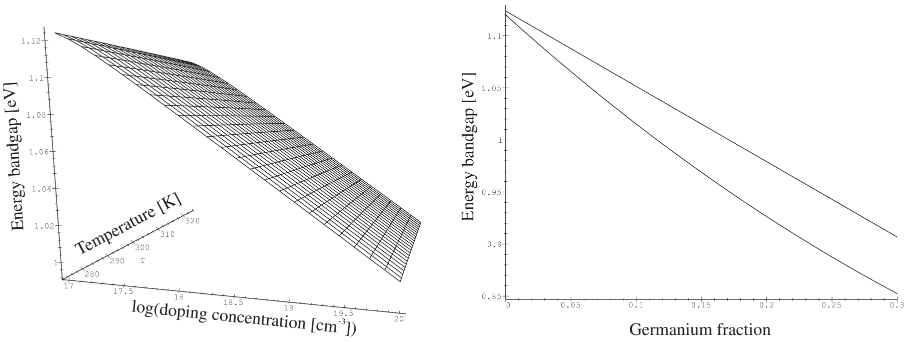

Figure 2.10: Energy band-gap versus doping, temperature and alloy combination. Left: Silicon at different doping levels and temperatures. Right: impact of alloying with Germanium, the upper curve is calculated using [24] and the lower curve is calculated using [23].

is used [3]:

$$n_i = 3.59 * 10^{19} * \left(\frac{T}{300}\right)^{3/2} e^{\frac{-E_g}{2V_T}} \tag{2.43}$$

which includes the temperature dependence. In the case of an alloy, the expression becomes more complex [24]:

$$n_i(x,T) = \sqrt{N_{cSiGeStrain}(x,T) * N_{vSiGeStrain}(x,T) * e^{\frac{-E_g}{V_T}}} \tag{2.44}$$

$$N_{cSiGeStrain}(x,T) = N_{cSiGeXStrain}(T) + N_{cSiGeLStrain}(x,T) \tag{2.45}$$

$$N_{cSiGeXStrain}(T) = 2* \left(\frac{2\pi * 0.3272 * m_0 k_B T}{h^2}\right)^{3/2} * \left(4 + 2 * e^{\frac{-0.6*x}{V_T}}\right) * 10^{-6} \tag{2.46}$$

$$N_{cSiGeLStrain}(x,T) = 2* \left(\frac{2\pi * 0.2217 * m_0 k_B T}{h^2}\right)^{3/2} * 4 * e^{\frac{-1.0709+1.366*x-0.1615*x^2}{V_T}} * 10^{-6} \tag{2.47}$$

$$N_{vSiGeStrain}(x,T) = N_{vSiGehhStrain}(x,T) + N_{vSiGelhStrain}(x,T) \tag{2.48}$$

$$N_{vSiGehhStrain}(x,T) = 2 * \left(\frac{2\pi * 0.3272 * \mu_{hhSiGeStrain}(x) k_B T}{h^2}\right)^{3/2} * 10^{-6} \tag{2.49}$$

$$N_{vSiGelhStrain}(x,T) = 2 * \left(\frac{2\pi * 0.3272 * \mu_{lhSiGeStrain}(x) k_B T}{h^2}\right)^{3/2} * e^{\frac{-0.155*x}{V_T}} * 10^{-6} \tag{2.50}$$

$$\mu_{hhSiGeStrain}(x) = \frac{1}{\frac{1-x}{0.49} + \frac{x}{0.28}} m_0 \tag{2.51}$$

$$\mu_{lhSiGeStrain}(x) = \frac{1}{\frac{1-x}{0.16} + \frac{x}{0.044}} m_0 \tag{2.52}$$

where $\mathrm{n_i}$ has been calculated using the effective conduction ($\mathrm{N_{cSiGeStrain}}$) and valence ($\mathrm{N_{vSiGeStrain}}$) band. $\mathrm{N_{cSiGeXStrain}}$ and $\mathrm{N_{cSiGeLStrain}}$ account for the division of states into the X- and L valley respectively. $\mathrm{N_{vSiGehhStrain}}$ and $\mathrm{N_{vSiGelhStrain}}$ account for the division of states in the heavy and light hole band respectively.

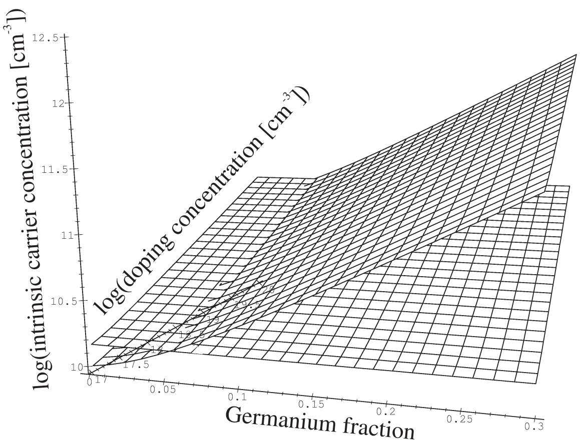

Figure 2.11: Intrinsic carrier concentration versus alloy combination and doping. The curve with higher value corresponds to eq. 2.44 (Silicon Germanium alloy) and the lower curve corresponds to eq. 2.43 (pure Silicon).

To convert the dimensions into [cm^{-3}] instead of [m^{-3}] in eq. 2.46, 2.47, 2.49 and 2.50, a factor of $(10^{-2})^3 = 10^{-6}$ is used. The effect on intrinsic carrier concentration from adding Germanium can be seen in Fig. 2.11. As can be noticed, both curves have very similar values at low Germanium fractions, thus indicating that eq. 2.44 can be used for also the case of no Germanium, i.e., pure Silicon.

2.6.3 Built-in voltage

The built-in voltage for a junction corresponds to the difference in work function for the two semiconductors, see Fig. 2.12. This can be calculated as [25]:

$$V_{jX} = \Phi_B - \Phi_X \tag{2.53}$$

Substituting for known entities, the expression becomes:

$$V_{jX} = \frac{E_{gB}}{q} - \Delta V_B - \chi_B - \Delta V_X - \chi_X \qquad (2.54)$$

where χ_B and χ_X is the electron affinity for the base and the opposite layer respectively, see Fig. 2.12.

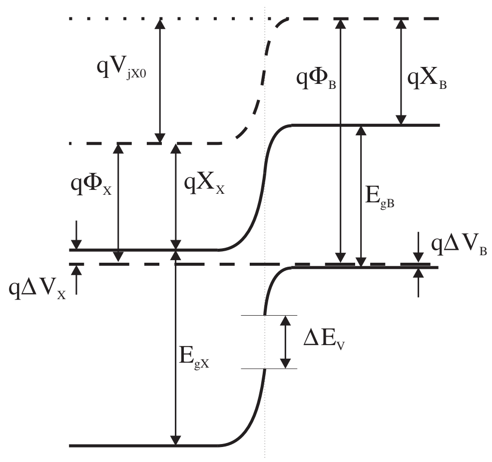

Figure 2.12: Band diagram for a zero bias junction showing how the built-in voltage has been calculated. The band levels are defined as in Fig. 1.2.

ΔV_X and ΔV_B denote the distance from either conduction band or valence band, depending on doping, to the Fermi level:

$$q\Delta V_X = \frac{E_{gX}}{2} - qV_T \ln\left(\frac{N_X}{n_{iX}}\right) \qquad (2.55)$$

assuming the Fermi level in an undoped material is in the middle of the band-gap. X is here either E, B or C. At the usually high base doping, $\Delta V_B < V_T$ and can thus be set to zero. Care needs to be taken not to achieve a negative ΔV_B which occur at high N_B. Although this indicates degenerate doping, the effects of this has not so far been treated. The impact on built-in voltage is still small. Possibly should only a part of the doping ions become electrically activated.

2.6.4 Breakdown field, breakdown voltage

For standard applications only the breakdown voltage over the collector SCR needs to be considered. This has been calculated as [20]:

$$V_{Cbreak} = \frac{\varepsilon_C E_{Cbreak}^2}{2qN_C} \qquad (2.56)$$

$$E_{Cbreak} = 2.5 * 10^5 \left(1 + \frac{[\log(N_C) - 14]^3}{14}\right) \tag{2.57}$$

The expression in eq. 2.57 differs from eq. 3.124 found in [20]. Evaluating both expressions and comparing with the graph in Fig. 3.13(b) (showing breakdown field versus background doping) of [20] shows however that eq. 2.57 gives a considerably better fit which justifies the correction. In recent communication with the author of ref. [20], a correction is suggested as [26]:

$$E_{Cbreak} = 2.5 * 10^5 \left(1 + \frac{[\log(N_C) - 14]^2}{3}\right) \tag{2.58}$$

Comparing eq. 2.57 and eq. 2.58 numerically shows that they differ at most a factor 1.5 from each other throughout the valid range of N_C.

With the comparably low doping (see Table 2.1), the theoretical value of V_{Cbreak} is fairly high (20 V), but in the structures that have been measured so far, the collector has become depleted long before the voltage reaches this value and breakdown occurs instead in the highly doped sub-collector. The highest voltage drop that can occur over the collector can roughly be calculated as:

$$V_{max} = \frac{N_C q W_C^2}{2\varepsilon_C} \tag{2.59}$$

which evaluates to approximately 3.5 V. With charge compensation in the SCR caused by an electron current flow, the effective doping of the collector goes down and the V_{max} decreases even further. The calculation of V_{Cbreak} should thus more be seen as an upper possible limit of the device. In applications where a device will operate close to breakdown, a more accurate value of V_{Cbreak} should be used which then substitutes the above calculation of V_{Cbreak}.

2.6.5 Carrier mobilities

Electron mobility has been calculated with the following expression [27]:

$$\mu_{nX}(N_X, T) = \mu_{n0}(T) + \frac{\mu_{n1}(T) - \mu_{n0}(T)}{1 + \left(\frac{N_X}{N_{ref}(T)}\right)^{\gamma(T)}} \tag{2.60}$$

$$\mu_{n0}(T) = 80 * \left(\frac{T}{300}\right)^{-0.45} \tag{2.61}$$

$$\mu_{n1}(T) = 1430 * \left(\frac{T}{300}\right)^{-2.25} \tag{2.62}$$

$$N_{ref}(T) = 1.12 * 10^{17} * \left(\frac{T}{300}\right)^{3.2} \tag{2.63}$$

$$\gamma(T) = 0.72 * \left(\frac{T}{300}\right)^{0.065} \tag{2.64}$$

which evaluates well for Silicon. There exists so far no reliable expressions for the SiGe alloy and instead a value of 200 cm^2/Vs has been used in alloys where $x > 0.10$ [13]. A publication [28] discusses however the topic and an expression could possibly be derived to a further development of the model. The value of the mobility of interest presented in [28] is however very close to the above used, at alloys with x=0.3 and high doping concentration (10^{20} cm^{-3}), which is the configuration mainly found in components studied so far.

Hole diffusion constant has been calculated as:

$$D_X = 1.14 * 10^5 * N_X^{-0.25} \tag{2.65}$$

which is an approximate expression derived from doping dependent hole mobility given in [3].

2.6.6 Delays

The delays for the carrier transport through the transistor originates essentially in two regions: the base-layer, caused by a diffusion transit time and in the base-collector SCR, caused by a drift transit time. It is important to distinguish between a transit time and a transit time delay where the delay is generally defined as [29]:

$$\tau = \left. \frac{\delta Q}{\delta I} \right|_{V\ constant} \tag{2.66}$$

The diffusion delay is calculated as [30]:

$$\tau_B = \frac{W_{Beff}^2}{\eta_B D_B} \tag{2.67}$$

The constant in the denominator (η_B) relates to the carrier distribution within the base and is here set to $\eta_B = 2.43$. For a rectangular profile of the doping impurities, the number would be 2 [3] and for a structure where a built-in field accelerates the carriers, η_B can increase drastically and thus lower the diffusion delay. The reference that was used for finding eq. 2.67 [30] calculated the cut-off angular frequency for which τ_B should be the reciprocal. Due to the brief paper it is unclear why $\eta_B \neq 2$ as for a rectangular profile. There might be an additional multiplying factor of 1.215 (to achieve the value of 2.43) which is related to the derivation of the cut-off frequency [30]. The value $\eta_B = 2.43$ is included here since there is no obvious explanation why τ_B should not be the reciprocal of the cut-off frequency. Other publications [31] indicate that the constant should be included as $\eta_B = 2.43$.

The drift delay through the base-collector SCR (τ_C) is calculated as [29]:

$$\tau_C = \frac{X_{jC} + X_{jBC}}{2v_s} \tag{2.68}$$

where X_{jBC} is the SCR within the base, adjacent to the collector SCR. This is usually negligible in comparison to the value of X_{jC}. The derivation of this delay assumes that the length of the SCR is fairly independent of current which may not always be the case at high injections, see earlier discussion about collector SCR width at large-signal operation.

2.6.7 Internal power dissipation and junction temperature

To be able to calculate the junction temperature, the internal power dissipation needs to be calculated. Following the classical expression, it is calculated as:

$$\mathrm{P} = \mathrm{i_C} * \mathrm{v_{CE}} + \mathrm{i_B} * \mathrm{v_{BE}} \tag{2.69}$$

The value of P is then output as a current through one of the ports in the SDD where it can be processed further in an external device, e.g., a resistor which then gives a voltage drop equivalent to the temperature rise, see Fig. 2.13. An internal evaluation of the junction temperature corresponding to a circuit as the one in Fig. 2.13a is also possible and it would save two ports in the SDD which can be very valuable, but the restrictions this impose on the possibilities of using different, possibly non-linear (see Fig. 2.13b), expressions for the junction temperature and the possibilities of thermal cascading of several devices as in a multi emitter-finger device (see Fig. 2.13c) makes this approach less interesting.

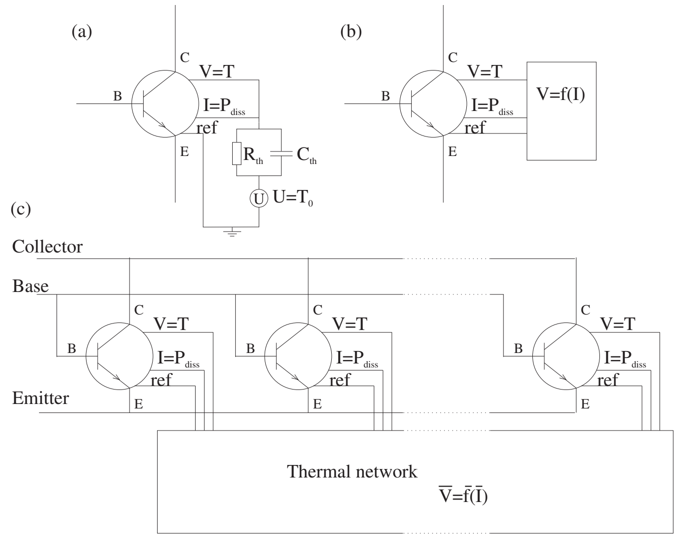

Figure 2.13: Schematic of different thermal models. (a) thermal RC-circuit, (b) 'black box' where output voltage is calculated as a function of the input current, (c) example how a multi emitter-finger transistor can be realized through a thermal coupling.

Chapter 3

Fitting of model parameters

3.1 Background

A natural step following the calculation of initial parameters for the studied device is to refine the values to fit an existing transistor. The studied transistors differ in electrical characteristics which necessitates the acquisition of individual model parameters for each transistor. As an example, 14 transistors with identical design have been measured on two different wafers and the resulting Gummel plots can be seen in Fig. 3.1. Although the devices are situated within an area less than 10x10 mm^2, the currents differ by as much as a factor of 5 which indicates that several parameter will need to be fitted or extracted to achieve a good correspondence between calculated and measured data for a specific device. With the coupling of the model parameters to the physical device, it should however still be possible to use the model to indicate how changes of the transistor design would affect the device performance. In the following discussion the word 'extraction' should be interpreted as the means of finding a value for a certain parameter which is within a given range. It is thus not a pure extraction in the sense that no initial value is defined. The extraction serves rather as a verification of the calculations and as a pointer for the direction where to adjust the parameters.

3.2 Fitting procedure

The fitting procedure can schematically be seen in Fig. 3.2. A theoretically derived transistor serves as an initial raw device whose parameters are varied within adequate limits. The base-emitter junction area can be expected to vary within, e.g., 0 and -50% of nominal values and an adjustment can thus be used to fit the calculated collector current to measured data. An emphasis has been put in trying to use only measurements where the device has somewhat the same bias as it will have during normal operation. It is more interesting to find a somewhat good fitting of a parameter at a bias which reflects normal operation than a very good match for

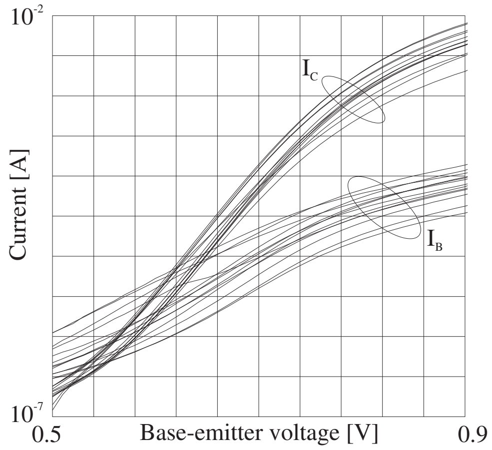

Figure 3.1: Gummel plot of 14 transistors of the same design.

a parameter which is critical for an unrealistic bias setting. The risk with extracting parameters at extreme bias settings is that one tries to draw conclusions from simplified models. This means that these model parameters may have to be extrapolated back to a point of normal bias operation. This extrapolation is undesirable since the circumstances existing when extracting at an extreme bias may include effects that are not considered by the model, but will affect the fitting of the used parameters. An example of this can be the base-emitter junction capacitance which in a reverse bias condition can give a distinct result which is not applicable for the high forward bias prevalent during normal operation of an HBT. The fitting procedure is also an iterative process where already fitted parameters are further refined towards the same measurement results due to a coupling between model parameters, where calculated data from a subsequent fitting indicates that a parameter should be re-fitted. This may appear contradictive, but it is necessary since the effects of variations in different parameters are coupled. As an example, the parameters for the collector current need to be re-fitted after a variation in the thermal resistance which defines the temperature elevation of the junction caused by the internal power dissipation. The practical process of performing a fitting involves the optimization feature of MDS. A parameter that will be fitted is entered as a nominal value with boundaries. These can be defined in the following ways:

relative:	x */ y	$x/y < x < x * y$
absolute:	x +- y	$x - y < x < x + y$
definite:		$a < x < b$

The optimizer within MDS thus varies the parameter in order to make a given error function, dependent of, e.g., a small signal RF simulation, as small as possible. Several parameters can be fitted during one optimization, but the number of necessary simulations increase drastically with increasing number of parameters. With many degrees of freedom, the results can also become odd since the optimizer treats all parameters as equally important in the sense that only the given boundaries are of importance. It is thus necessary to only optimize parameters whose impact on a certain error function is directly related. If certain parameters are only weakly affecting the error function, a set of these parameters where all are on their respective boundaries, can be found to give a slightly better result than not changing the parameters at all. It is questionable whether that result is a physically better solution.

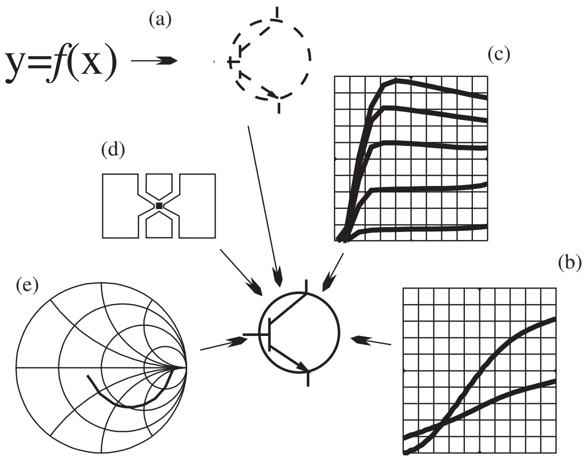

Figure 3.2: A schematic picture of the fitting procedure. (a) parameters with calculated values for the transistor are used for an initial device description. (b) using Gummel measurements, (c) IV-curves, (d) measurements of test structures and finally (e) measured S-parameters, a closer fit to a real device is possible.

3.2.1 Fitting towards the Gummel plot

The first step in the procedure is to find a good characterization of the currents in the device. These give valuable information of the intrinsic device geometries, e.g., emitter area and layer structure. The effects of varying the parameters are somewhat interconnected and it is thus necessary to put an order in where parameters with the strongest impact are primarily varied for the coarse adjustment. Some parameters are also having tighter limits (e.g. layer thicknesses who are grown using MBE which gives accurate dimensions) which makes their optimization boundaries small. This means that their total impact on the fitting may be smaller. As a conclusion, both the impact from a parameter and the range in which it is allowed to vary needs to be considered for finding the relative importance between the different parameters. In addition, the base current is the only component which is used for extracting artificial data, unique for each transistor, i.e., the leakage currents between base and emitter. The measurements for the fitting is preferably performed at different temperatures to see the thermal effects which come out strongly due to the exponential effects (see eq. 1.5 and 2.33) as can be seen in Fig. 2.8. The Gummel plot can be divided into three different regions as discussed earlier and the different parameters are fitted to measurements in the region where their impact on the currents are the biggest. Due to the coupling between the different currents, the fitting procedure for the parameters may need to be run in parallel for parameters affecting the collector current and parameters affecting the base current in the same region respectively, see below for extraction of r_E. The fitting procedure is usually performed for the parameters in the following order: Collector current: A_E, N_B, W_B, n_F, r_E. Base current: N_E, artificial currents. During the measurements, leakage currents that are possibly outside the actual transistor can occur which can be seen as the almost voltage independent part of the current at low V_{BE} (see Fig. 2.7). The origin of these currents can be in the bleed- resistors of the bias-T's, surface currents between the different contacting pads of the transistor or on the actual transistor, or from generation-recombination (GR) processes in the SCR of the base-collector junction. These currents can have an impact on the result when performing fitting of parameters at current levels where these parasitic currents can not be considered negligible. The resulting error in the fitting of parameters will then affect the circuit behavior at higher currents, i.e., at normal bias conditions. For accuracy reasons in the fitting it can thus be worthwhile to account for the parasitic currents as constant current generators in the base-emitter and base-collector junction although they can be of negligible interest from a circuit point of view and can be possibly discarded in the final model, depending on the size of the current. The bleed-resistors of the bias-T's are also included as external elements outside the transistor, but their impact is small since the parasitic currents often are much bigger than what would be expected from the bleed resistors. Since the coupling between the currents is fairly small in region I (see Fig. 2.7), A_E, N_B, W_B and n_F can there be fitted independently of the value of the base current. It is however necessary to assure that r_E is small since it otherwise can limit the collector current and thus affect the fitting. The three first parameters are varied to fit the absolute value of the collector current to the measured data whereas the fourth (n_F) is used for finding the correct slope. The emitter area and ideality factor are independently varied as parameters whereas base width and doping are more closely related from fabricational reasons. To prevent the usually high base doping from diffusing into the emitter and collector, a low doped barrier (so called spacers or set-back layers) are grown on each side of the base. These occupy together approximately 10% to 30% of the total grown base-width and they will be doped during later fabrication steps because of the necessary heat treatment that the device has to undertake. For this reason the electrical base-width can actually increase up-to 40%. This effect must however then also include that the total doping goes down with an equal factor, i.e., the Gummel number remains constant. An initial assumption has been that all of the set-back layers have been doped by out-diffusion since the fabrication process is optimized for the electrical junction (doping level) and the metallurgical junction (interface of Silicon and Silicon Germanium alloy) to coincide. Due to the exponential dependence of n_F and that the fitting is performed at a voltage where the value of the exponential function varies strongly with n_F, this parameter will have a strong impact on the absolute value of the current. It is therefore important to fit the parameters (A_E, N_B, W_B and n_F) affecting the collector current iteratively. In the purely exponential region (the collector current above the beginning of region II, see Fig. 2.7), it suffices to use three evenly spread points for the simulation part of the optimization.

Table 3.1: Initial model parameters taken mainly from fabricational data. Values that have been estimated are marked with a "".*

parameter	value	parameter	value	parameter	value
W_E[cm]	$.070 * 10^{-4}$	W_B[cm]	$.030 * 10^{-4}$	W_C[cm]	$.300 * 10^{-4}$
N_E[cm^{-3}]	$2 * 10^{18}$	N_B[cm^{-3}]	$1 * 10^{20}$	N_C[cm^{-3}]	$5 * 10^{16}$
A_E[cm^2]	$20 * 10^{-8}$	x_{Ge}	0.30	A_C[cm^2]	$40 * 10^{-8}$
ρ_E^*[Ω/cm^2]	$5.0 * 10^{-6}$	ρ_B^*[Ω/cm^2]	$5.0 * 10^{-6}$		
W_F[cm]	$.070 * 10^{-4}$				
L_F^*[cm]	$3.0 * 10^{-4}$	L_B^*[cm]	$2.0 * 10^{-4}$	R_C^*[Ω]	5
J_{E1}[A/cm^2]	0	K_{Ie}	1	$I_{BCectleak0}$[A]	0
n_{E1}	1	K_{Ih}	1	$n_{BCectleak0}$[A]	1
$V_{Offset1}^*$[V]	0.55	n_F	1.0		
V_{therm1}^*[V]	0.20	n_R	1.0		

Using the collector current at the highest values of V_{BE} (see Fig. 2.7), the emitter resistivity (r_E), is adjusted. The value can be found fairly easily at high collector currents because of the strongly limiting effect it has. Care must be taken to also have a correct base current in this region since it is the sum of these currents that cause the voltage drop over the emitter resistance and thus limits the voltage drop of the base- emitter junction. An iterative process where the parameters for the different currents are adjusted consecutively works well. Applying the above discussion on a typical transistor (in this case a B3603_120Z), a fitting of the model parameters towards the Gummel plot has been done. The original data for the model parameters can be seen in Table 3.1 and the resulting Gummel plot is shown in Fig. 3.3.

The collector current is strongly overestimated compared to the measured data (see Fig. 3.3) and the base current exhibits a more ideal behavior compared to the measured data. Concentrating on finding a correct collector current, the emitter area (A_E) is adjusted to account for the apparent over-etch to $10 * 10^{-8}$ cm^2 which gives a decrease in current by a factor of 2, see Fig. 3.4. A smaller A_E is unlikely and thus the Gummel number of the base is adjusted. With the assumption that the base doping (N_B) may vary with a factor of two, N_B is thus set to $2 * 10^{20}$ cm^{-3}. At these high doping levels, the classical expression for apparent band-gap narrowing [32] overestimates the actual value with a too high calculated injection as result [19]. For this reason I_{Ee} need to be limited by a factor (K_{IEe}). From Fig. 1.4 in [19], a

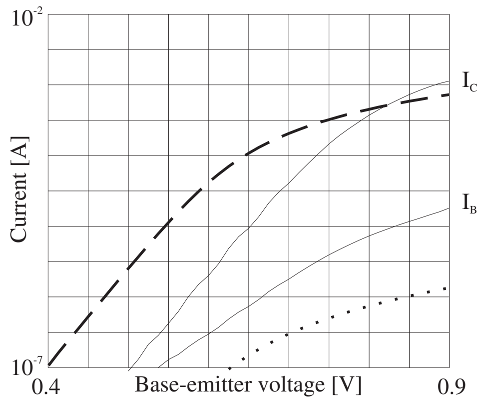

Figure 3.3: Gummel plot with calculated and measured data for the modeled transistor. The model parameters are taken from fabricational data and from estimations where immediate values are not available. Dashed lines correspond to calculated data and solid lines correspond to measured data.

value of 0.3 is chosen. The resulting Gummel plot can be seen in Fig. 3.5.

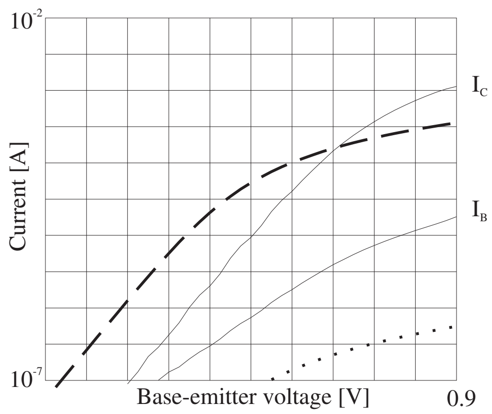

Figure 3.4: Gummel plot where the parameter $\mathrm{A_E}$ *has been decreased to* $10 * 10^{-8}$ cm^2. *The lines are defined as in Fig. 3.3.*

The collector current is still overestimated, but the strong limitation at high $\mathrm{V_{BE}}$ in comparison with the measured data also indicates that the contact resistivity of the emitter contact is too high. This will not affect the collector current at lower $\mathrm{V_{BE}}$, but the ideal region of the collector current (corresponding to the collector

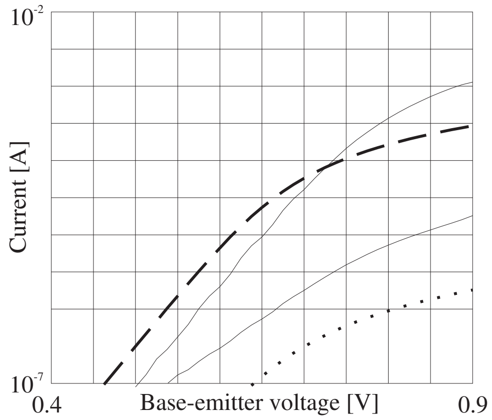

Figure 3.5: Gummel plot where $\mathrm{N_B}$ *has been set to* $2 * 10^{20}$ $\mathrm{cm^{-3}}$ *and* $\mathrm{K_{IEe}}$ *has been set to 0.3. The lines are defined as in Fig. 3.3.*

current above region II in Fig. 2.7) will be smaller than necessary and thus a shorter range in $\mathrm{V_{BE}}$ can be utilized for the optimization of the ideality factor ($\mathrm{n_F}$). In order to prepare for the subsequent optimization for $\mathrm{n_F}$, $\mathrm{r_{Econt}}$ is changed from the estimated $5 * 10^{-6}$ $\Omega\mathrm{cm}^2$ to $5 * 10^{-7}$ $\Omega\mathrm{cm}^2$ which should be a lower limit. This value is possibly too low for a real contact [13], indicating that the contact resistance for the moment is negligible. The calculated collector current in Fig. 3.6 is higher than the measured which could be interpreted as a too low contact resistance is chosen. Subsequent fitting will however show that the assumed value works well.

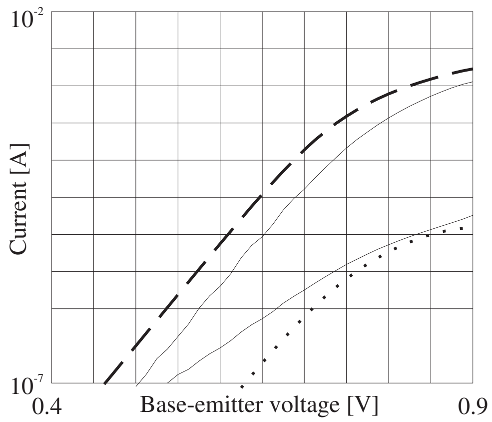

Figure 3.6: Gummel plot where $\mathrm{r_{Econt}}$ *has been set to* $5 * 10^{-7}$ $\Omega\mathrm{cm}^2$*. The lines are defined as in Fig. 3.3.*

To find a collector current that corresponds well with measured data, n_F and K_{IEe} are adjusted. It is unlikely that only an adjustment of n_F would lead to a successful match between calculated and measured collector current as an offset still exists, see Fig. 3.6. That the offset can be ascribed only to an overestimation of the band-gap contraction when K_{IEe} already is set to 0.3 is not clear. However, other effects that would block an injection, e.g., a small spike in the conduction band caused by a slight offset between the electrical and metallurgical junctions, can here empirically be included. Altering K_{IEe} from 0.3 to 0.2 and setting n_F to 1.036 gives a calculated collector current which well corresponds to the measured, see Fig. 3.7.

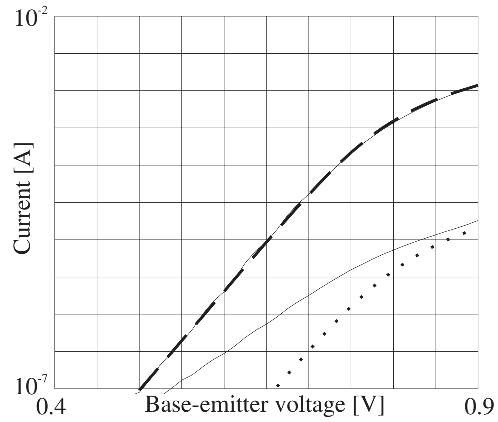

Figure 3.7: Gummel plot where K_{IEe} *is set to 0.2 and* n_F *is set to 1.036. The lines are defined as in Fig. 3.3.*

To get a better match between calculated and measured base-current, an artificial current source needs to be introduced as discussed earlier. As can be seen in Fig. 3.7, the calculated base-current is very close to the measured one at high V_{BE} which means that an added current source would risk to create a too big calculated base-current. However, it is necessary to have a such a current source at low V_{BE} in order to model the base-current correctly. Thus, the ideal part of the base-current is multiplied by a factor K_{IEh}. With K_{IEh}=0.5, J_{E10}=2.663 A/cm^2, n_{10}=1.814 and V_{T10}=0.20, a good match between calculated and measured data is acquired, see Fig. 3.8. In order to verify the validity of the match, also collector current versus collector-emitter voltage is calculated, see Fig. 3.8.

With the good match between calculated and measured data for both the collector and base current, a fine tuning of r_{Econt} can be made which gives a result of $r_{Econt}=5.31 * 10^{-7}$ Ωcm^2. Such a small deviation from the previously assumed one does not give a distinguishable change in the Gummel plot.

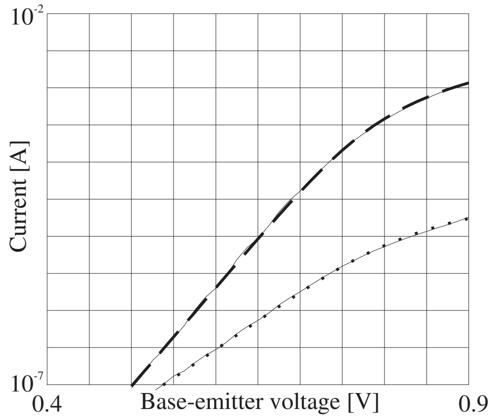

Figure 3.8: Gummel plot where K_{IEh}*=0.5,* J_{E10}*=2.663* A/cm^2*,* n_{10}*=1.814 and* V_{T10}*0=0.20. The lines are defined as in Fig. 3.3.*

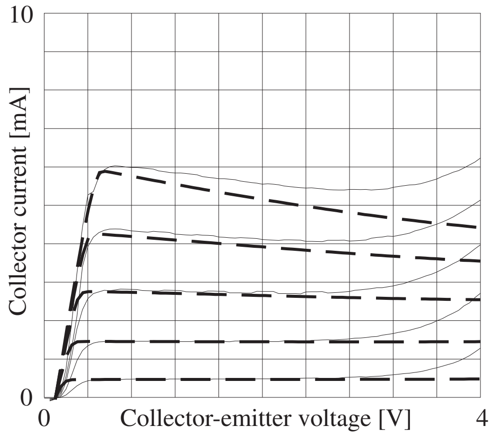

Figure 3.9: Collector current versus collector-emitter voltage for base currents from 20 μA *to 100* μA *in steps of 20* μA*. Dashed lines correspond to calculated data and solid lines correspond to measured data.*

3.2.2 Fitting towards plot of collector current versus collector-emitter voltage

Following the Gummel plot, the DC parameters are fitted against the IV-curve. Using the slope of a high collector current at a collector-emitter voltage around 1.5 V (beyond the saturation region of the transistor), the thermal resistance is adjusted. Due to the thermal dependencies for the base and collector current in an HBT, this area will exhibit a negative differential resistance. The base current increases quicker with temperature than the collector current, or conversely: for a constant base current the collector current decreases with increasing temperature. When the slope changes in the IV-curve, also the difference between measured and calculated data increases in the Gummel plot and further fitting using the Gummel plot can become necessary. Although the internal power dissipation during the Gummel measurement is small because of the low base-collector voltage, the thermal effect can be noticeable at high currents and must therefore be accounted for. A fine tuning of the base and collector currents in the active bias region can also be done using the IV-curve. Since the Gummel plot uses logarithmic values, the dynamic range is big, but accuracy can become difficult, especially in the narrow range of V_{BE} which defines the typical active region. When adjusting parameters towards the IV-curve, accuracy can be increased and more importantly, the adjustments are made towards the region in which the device later will operate. Care must then also be taken that the fit against the Gummel curve is maintained. When altering parameters in the model for a current to better fit in the IV-curve, the Gummel plot will change. Although there is a seemingly good fit in the IV-curve, both currents in the Gummel plot can be offset from the measured value. As long as the interdependence between I_B and I_C (which defines β) is maintained, the calculated IV-curve will correspond to measured values and not indicate the discrepancy between measurement and calculated values in the Gummel plot. It is thus important to be very restrictive in the fitting of parameters towards the IV-curve. An effect of smaller significance is the slightly varying offset in V_{CE} for the different curves of the collector current. This can be well modeled with a diode between the base and collector pad and the effect is likely to be caused by leakage currents on the surface of the collector. The current generator inside the SDD is not appropriate for handling this current since the surface of the collector exists outside the base-lead resistances and the extrinsic base-collector junction (see Fig. 2.1 and 2.4). Additionally, the voltage drop occurring over the collector-lead resistance (R_C in Fig. 2.5) need not affect this leakage current. By adjusting the saturation current, the offset voltage can be changed, a high saturation current corresponds to a high offset voltage. The sharpness in the transition from saturation region to ohmic region is controlled by the ideality factor of the diode. A value close to unity corresponds to a sharp transition and a high value corresponds to a slow transition. The collector lead resistance (R_C) is adjusted towards the slope of the collector current at low collector-emitter voltage and high base current, i.e., in the saturation region. Continuing the fitting procedure of the studied device, it can be seen in Fig. 3.9 that the slope of the calculated collector current is steeper than that of the measured one at high currents. This indicates a too high thermal resistance (R_{th}) of the simulated device. Adjusting R_{th} to 1200 K/W creates a slope which corresponds well to measured data, see Fig. 3.10. Due to this change however, it is necessary to verify that the Gummel plot has not changed so that the measured and calculated data still correspond well.

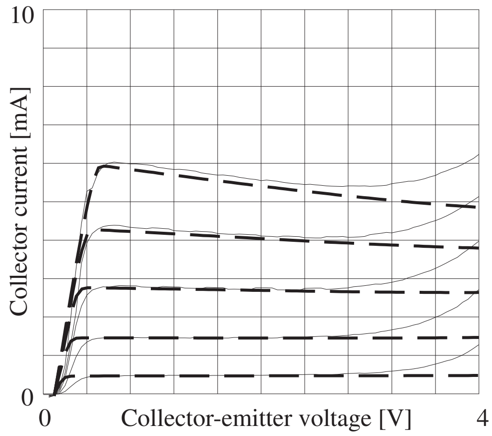

Figure 3.10: Collector current versus collector-emitter voltage for base currents from 20 μA to 100 μA in steps of 20 μA. The thermal resistance (R_{th}) is set to 1200 K/W. The lines are defined as in Fig. 3.9.

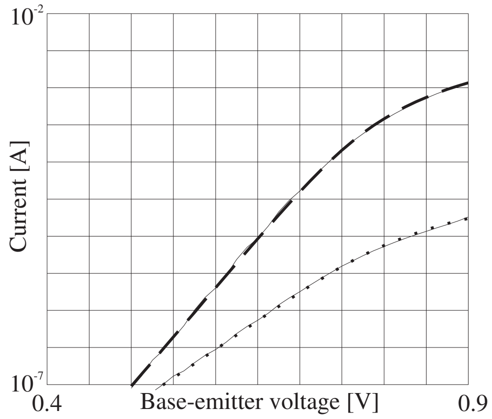

Figure 3.11: Gummel plot where R_{th}=1200 K/W. The lines are defined as in Fig. 3.3.

As can be seen in Fig. 3.11, the variation in base and collector current is very small and the model can retain its parameter values. The calculated collector current exhibits no breakdown effects, occurring as quickly increasing collector current with increasing collector-emitter voltage in the ohmic region, which the measured data does as can be seen in Fig. 3.10. A breakdown effect is however included in the model, but this will for the current doping appear at higher collector-emitter voltage. By adjusting the calculated breakdown voltage by a factor of 0.5, a collector current that exhibits characteristics similar to the measured can be achieved, see Fig. 3.12. The strong decrease of the breakdown voltage indicates that the current modeling does not correctly account for the physical breakdown processes that occur in the device. The empirical approach of lowering the breakdown voltage can however work sufficiently well in simulations since the device should not be operated in the breakdown region as this is likely to destroy the device.

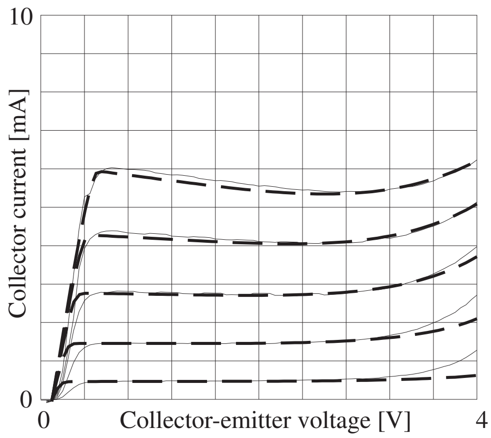

Figure 3.12: Collector current versus collector-emitter voltage for base currents from 20 μA to 100 μA in steps of 20 μA. The analytically calculated collector breakdown voltage has been multiplied by a factor of 0.5. The lines are defined as in Fig. 3.3.

The last step of the fitting for the DC-parameters is to adjust the offset voltage which can be seen as the collector-emitter voltage where the transistor starts conducting a collector current. With $I_{BCextleak0}=0.8 * 10^{-8}$ A and $n_{BCextleak}=2.5$ the calculated and simulated values for the collector current in the saturated region agree well and there is not a need to adjust the collector-lead resistance from the initially estimated one, see Fig. 3.13.

3.2.3 Fitting towards scattering parameters

The final step for the fitting is to adjust values towards measured S-parameters. The difficulty, or what should be stressed here is the importance of using the measured data for comparison efficiently. As in the case of steady state, characteristics can be presented in different ways. For input and output matching, the Smith chart suffices

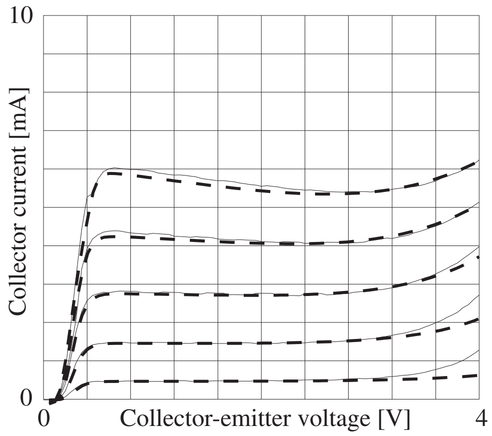

Figure 3.13: Collector current versus collector-emitter voltage for base currents from 20 μA to 100 μA in steps of 20 μA. The extrinsic base-collector leakage current has been added as $\mathrm{I_{BCextleak0}}$*=0.8 ∗ 10^{-8} A and* $\mathrm{n_{BCextleak}}$*=2.5. The lines are defined as in Fig. 3.9.*

as it spans the whole impedance range with high resolution for the impedances of interest (assuming a 50 Ω system). The transmission parameters can similarly be presented well with polar plots. The benefit with this representation is that both magnitude and phase can be compared simultaneously. The limitation, however is that the frequency dependence will be slightly obscured and the risk of having a seemingly good correspondence between a calculated and a measured data point, although their frequencies do not match should not be neglected. For this reason it is also important to look at a graph where data is plotted directly versus frequency. These graphs do not necessarily show a very good accordance between calculated and measured data, although a polar plot has done so and a further tuning towards this kind of plot has to be done. This is especially true at higher frequencies. Another kind of presentation that can be of big importance is the plot of h_{21} and unilateral gain (MUG) to find f_t and f_{max} who both are very important parameters for the device as they define an upper limit for where efficient operation in circuits can be accomplished. A matching between calculated and measured data for one bias point is here reasonably easy to accomplish and there has been several methods presented for doing this [33, 34, 35]. What is important however is to have the same set of model parameters making the model match calculated and measured data for different bias points. By acquiring this set of model parameters, large-signal modeling can be facilitated to a certain extent. Some large-signal effects require a more complete description than the one used in this model. One example of this is the drift delay through the collector SCR at current variations high enough to vary the depletion width during a constant voltage drop. This should however not be confused with the static collector bias current which causes a static SCR expansion as discussed earlier. The very high powers where these effects cannot be modeled sufficiently with the present model seem not to occur at normal modes of non-linear operations. Modeling of large-signal effects with the model has so far given adequate results [22] as discussed earlier. Due to the complexity and the coupling between the different model parameters there is no straight procedure in which parameters are found in a consecutive order. This section will instead present examples of how a variation in a parameter affects the calculated S-parameter and how this can be used to get a better match between calculated and measured data. From the previous fitting for DC-parameters however, the calculated S_{21} should compare reasonably well with measured data for different bias points since S_{21} is closely related to β.

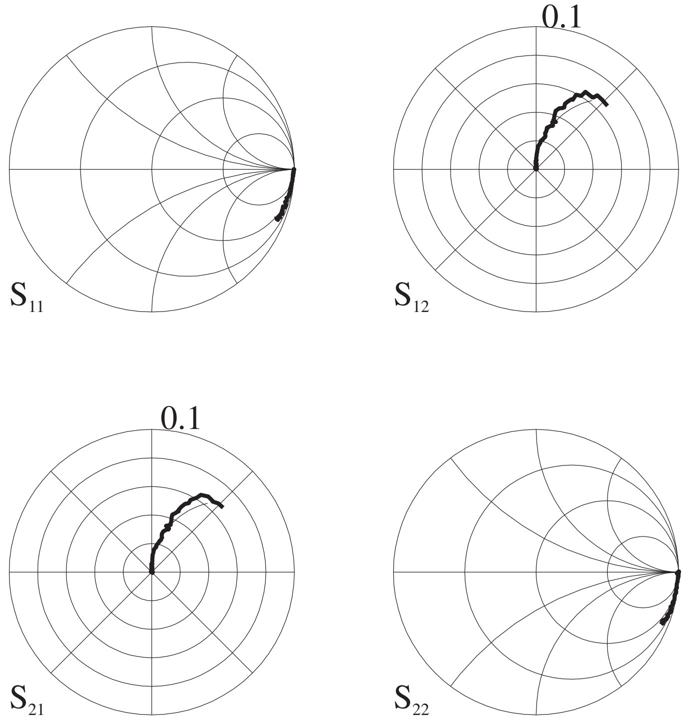

Figure 3.14: Measured and calculated S-parameters for a test structure near the studied device. The frequency is from 200 MHz to 50 GHz. Thick lines denotes measured data, thin lines denote calculated data. For S_{11} *and* S_{22}*, measured and calculated data overlap.*

The first step of fitting considers the embedding shell which involves measurements of test structures to find a good electrical description of how the contacting pads behave. Ideally, components with an open and shorted termination and a through-line should be measured to find information about cross-coupling, inductances, resistances and losses. An example of a measured data for a test structure with open termination situated near the fitted device can be seen in Fig. 3.14 where also calculated data is shown. The corresponding parameters for the components can be seen in Table 3.2. It can be noticed there that the resistances corresponding to the losses (R_{BEloss}, R_{CEloss}, R_{Eloss} and R_{Closs} respectively) have negligible effect which speaks for that this device has low losses outside the actual transistor. This corresponds well to the measurements which show a reflection coefficient of almost unity, see Fig. 3.14. The length of the two transmission lines agrees well with what can be expected. As no through line or shorted structure was available, the values of the inductances and lead resistances are estimated values found for similar devices.

Table 3.2: Data for parameters of the embedding shell to fit the measured open test structure.

parameter	value	parameter	value	parameter	value
L_{Bpad}	9.5 pH	L_{Cpad}	4.4 pH	L_{Epad}	11.0 pH
C_{BE}	2.17 fF	C_{BC}	2.25 fF	C_{CE}	1.00 fF
R_{BE}	2493 Ω	R_{BC}	428 Ω	R_{CE}	4227 Ω
R_{Bpad}	0.05 Ω	R_{Cpad}	0.05 Ω	R_{Epad}	0.05 Ω
R_{Bprobe}	0.05 Ω	R_{Cprobe}	0.05 Ω	R_{Eprobe}	0.05 Ω
R_{BEloss}	50 kΩ	R_{CEloss}	50 kΩ	L_{TLB}	63 μm
R_{Eloss}	0.05 Ω	R_{Closs}	0.05 Ω	L_{TLC}	66 μm

Studying the actual device, the calculated transmission parameter S_{21} should compare well with the measured one. It is however important to study this parameter closely at high frequencies and here the polar plot might give ambiguous results. Due to the comparably high frequency even a very short transmission line, e.g., the contacting pads, will cause a phase shift as discussed above. The difficulty is to define where the transmission line begins since the probes that are used at the measurements will contact the pads at slightly different points for different measurements. Thus a certain amount of inaccuracy is here probably unavoidable unless a very sophisticated measurement method can be employed. For this reason a slight discrepancy in phase below 15°, corresponding to a CPWTL of 50 μm at 50 GHz, between calculated and measured data should be accepted (for a contact pad where probes are separated approximately 100 to 200 μm) and emphasis should be put on studying the magnitude. Due to the impact on parameters like f_t and f_{max}, several parameters affecting the high frequency performance need to have an adequate fit in order to be able to estimate the device performance correctly.

For the studied device, S-parameters have been calculated for different bias points which covers bias for normal operation, see Fig. 3.15, 3.16 and 3.17. The calculated data agrees well with measured data as can be seen in the figures and although a further tuning may result in a better match, it would also mean deviations from the initial assumptions of device parameters. As there is no clear partition between the different parameters in how they affect the RF-performance, a variation in parameters may improve the matching although the improvement is based on an erroneous adjustment. However, where the agreement between calculated and measured data is worse than what has been found for the studied device, adjustments can be made where the impact of a single parameter clearly can improve the match for different bias points and it is thus more probable that the parameter indeed should be altered. To give an impression on how different parameters affect the RF-performance, different parameters have been varied, one at a time, around its nominal value by the factors of 0.1, 1 (nominal value) and 10. With these parameter settings, S-parameters have been calculated and are shown in 4.

Table 3.3: Parameter values for the fitted model.

parameter	value	parameter	value	parameter	value
W_E[cm]	$.070 * 10^{-4}$	W_B[cm]	$.030 * 10^{-4}$	W_C[cm]	$.300 * 10^{-4}$
$N_E[cm^{-3}]$	$2 * 10^{18}$	$N_B[cm^{-3}]$	$2 * 10^{20}$	$N_C[cm^{-3}]$	$5 * 10^{16}$
$A_E[cm^2]$	$10 * 10^{-8}$	x_{Ge}	0.30	$A_C[cm^2]$	$40 * 10^{-8}$
$\rho_E[\Omega/cm^2]$	$5.31 * 10^{-6}$	$\rho_B[\Omega/cm^2]$	$5.0 * 10^{-6}$		
W_F[cm]	$20 * 10^{-4}$				
L_F[cm]	$3.0 * 10^{-4}$	L_B[cm]	$1.0 * 10^{-4}$	$R_C[\Omega]$	5
$J_{E1}[A/cm^2]$	2.91	K_{Ie}	0.2	$I_{BCextleak0}$[A]	$0.8 * 10^{-8}$
n_{E1}	1.845	K_{Ih}	0.5	$n_{BCextleak0}$	2.5
$V_{Offset1}$[V]	0.55	n_F	1.036		
V_{therm1}[V]	0.20	n_R	1.000		

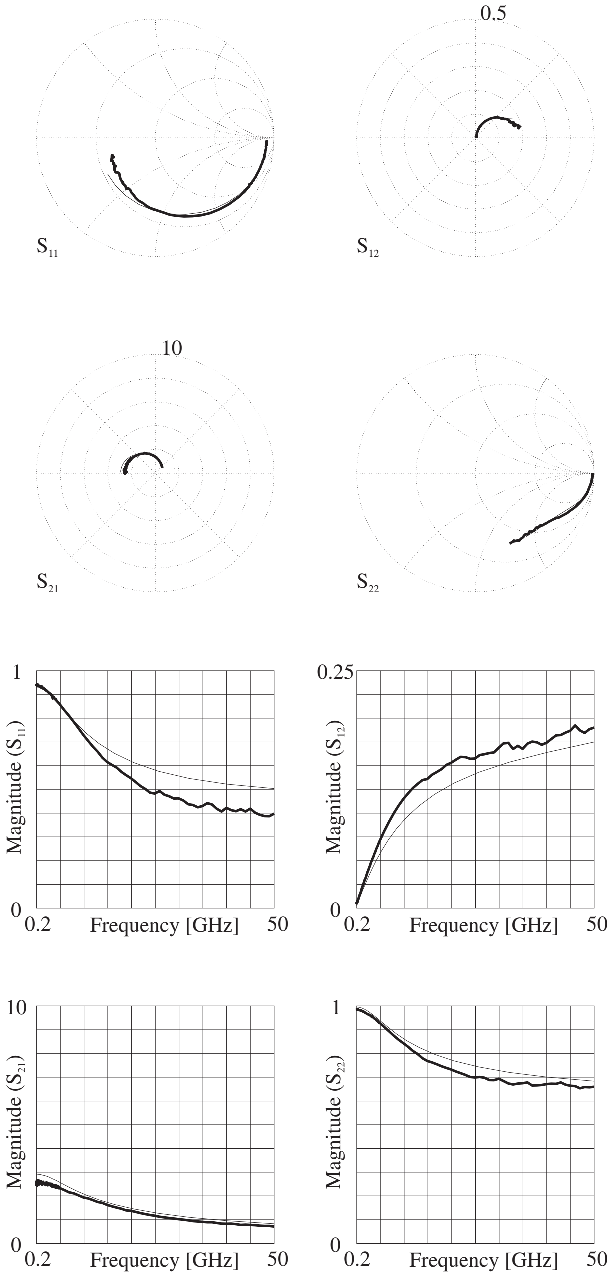

Figure 3.15: Measured and calculated S-parameters at I_C *=1 mA,* V_{CE} *=2V. Frequency is from 200 MHz to 50 GHz, all curves in polar plots move clockwise with increasing frequency. Thin lines denote calculated data and thick lines denote measured data.*

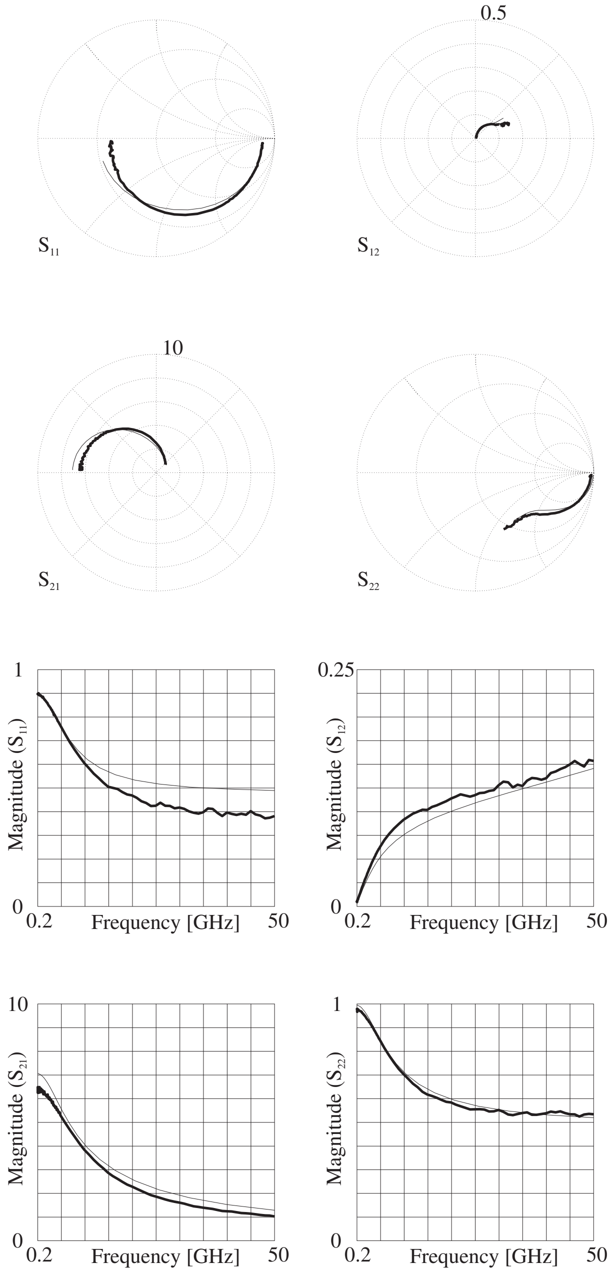

Figure 3.16: Measured and calculated S-parameters at $\mathrm{I_C}$ *=4 mA,* $\mathrm{V_{CE}}$ *=2V. Frequency is from 200 MHz to 50 GHz, all curves in polar plots move clockwise with increasing frequency. Thin lines denote calculated data and thick lines denote measured data.*

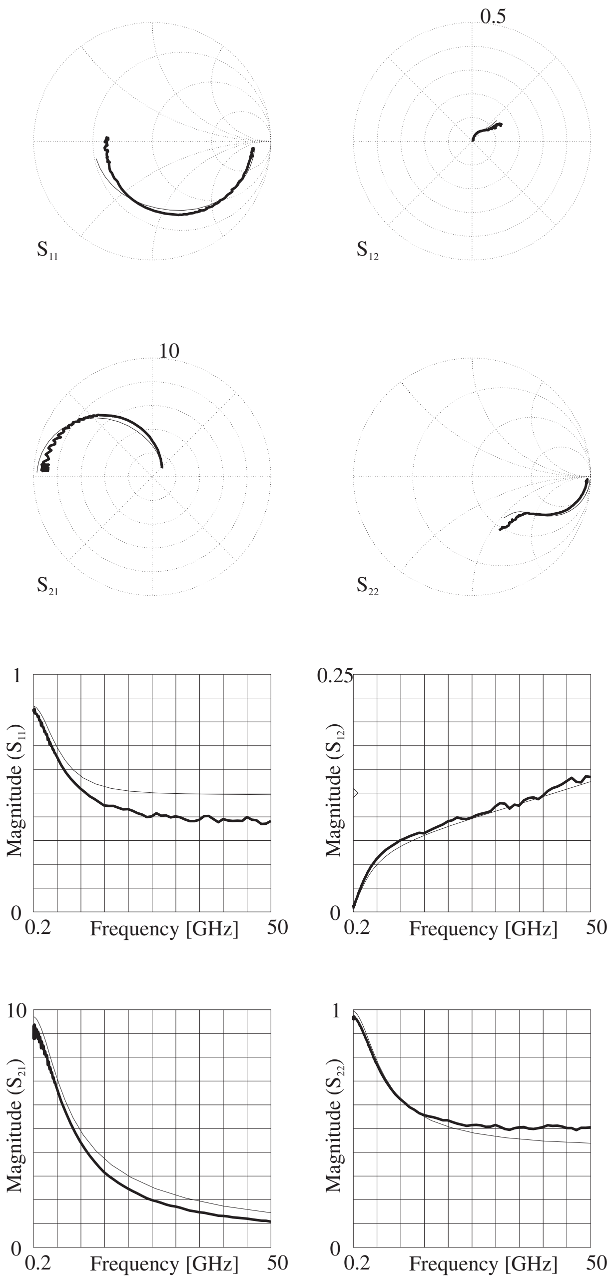

Figure 3.17: Measured and calculated S-parameters at I_C*=10 mA,* V_{CE}*=2V. Frequency is from 200 MHz to 50 GHz, all curves in polar plots move clockwise with increasing frequency. Thin lines denote calculated data and thick lines denote measured data.*

Chapter 4

Variation in S-parameters from a variation in model parameters

This section will show the impact on S-parameter from a variation in different circuit parameters as seen in Fig. 2.5 and Fig. 2.6. Only the parameters that show a distinguishable difference in the S-parameters when varying the circuit parameter have been included. The values of the circuit parameters have been varied one at a time around its nominal value with a factor of 10, i.e., curves corresponding to 0.1, 1 and 10 times the nominal value are shown for each S-parameter. Other circuit parameters have then been kept at their nominal values. The reason for varying the circuit parameters rather than physical parameters is to facilitate the identification of the impact each circuit parameter has which in turn can lead to understanding of how the underlying physical or technological parameters should be altered in the case of, e.g., a fitting procedure. The S-parameters relate to small signal circuits and the interpretation is thus easiest done using the circuit parameters of the model. The S-parameters have been calculated with the transistor in a common emitter configuration, connecting port 1 to the base and port 2 to the collector. Port impedance is set to 50 Ω. All S-parameters have been calculated in a frequency range from 200 MHz to 50 GHz. Common for all graphs is that frequency increases clockwise in the curves. To facilitate the interpretation of the S-parameters, simplified equivalent circuits are shown in Fig. 4.1 for the case when measurements are done from port 1 and port 2, corresponding to Fig. 4.1a and b, respectively. The nominal values of the different lumped elements can be seen in Table 4.1.

The impact on the S-parameters from a variation in R_{Bcont} can be seen in Fig. 4.2. At high values of R_{Bcont}, the magnitude of the forward coupling (S_{21}) exhibit a different behavior from the two other curves. An explanation to this can be that at the very low frequencies, no capacitances shunt any part of the transistor

Table 4.1: Nominal values for components in Fig. 4.1. Bias for the component is: V_{CE}*=2 V,* I_C*=4.0 mA.*

R_{Bcont}[Ω]	17	C_{BC} [fF]	4.9
C_{shunt} [fF]	750	C_{BE}[a] [fF]	220
R_{Blead}[Ω]	12	r_{BE}[b] [Ω]	360
R_{BCext}[Ω]	4.0	$R_{Eundepl}$[Ω]	0.92
C_{BCext}[fF]	40	R_{Econt}[ω]	5.3
R_C[Ω]	5.0	β[c]	69
$R_{Cundepl}$[Ω]	12		

[a]Includes junction and diffusion capacitance. They are approximately equal.
[b]Dynamic resistance of base-emitter junction.
[c]Current amplification factor.

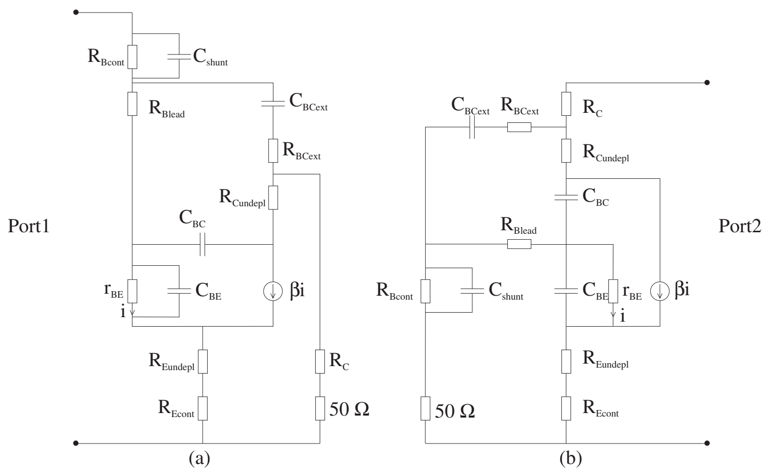

Figure 4.1: Simplified equivalent circuits identifying the relative positions of the different components in the transistor when performing measurements from (a) port1 or (b) port 2.

and the high value of R_{Bcont} in the base-lead is thus affecting the performance to a certain amount as can be seen in Fig. 4.2 S_{21}. At frequencies above the very low however, capacitances within the transistor begin to load and thus cause a voltage drop over R_{Bcont} which lowers the forward coupling. With increasing frequency C_{Bshunt} starts shunting R_{Bcont} and the impact from R_{Bcont} is decreased, thus the curve more resembles the one of R_{Bcont} at lower values. The impact on S_{11} from a variation of C_{Bshunt} indicates the validity of modeling the base contact with a shunting capacitance. At low values of C_{Bshunt} the resistance R_{Bcont} is included in the base-lead resistance which leads to a higher resistance at higher frequencies (see Fig. 4.3) compared to the case of a nominal or high value of C_{Bshunt}. At a high value of C_{Bshunt}, the resistance R_{Bcont} is instead shunted at all frequencies, see Fig. 4.3. Using the nominal value of C_{Bshunt}, R_{Bcont} is at low frequencies part of the base-lead resistance and thus following the curve corresponding to a low value of C_{Bshunt}. With increasing frequency, the reactance of the capacitance decreases and R_{Bcont} becomes increasingly shunted, thus the curve of the nominal C_{Bshunt} migrates at higher frequencies towards the curve of the higher value of C_{Bshunt}, see Fig. 4.3.

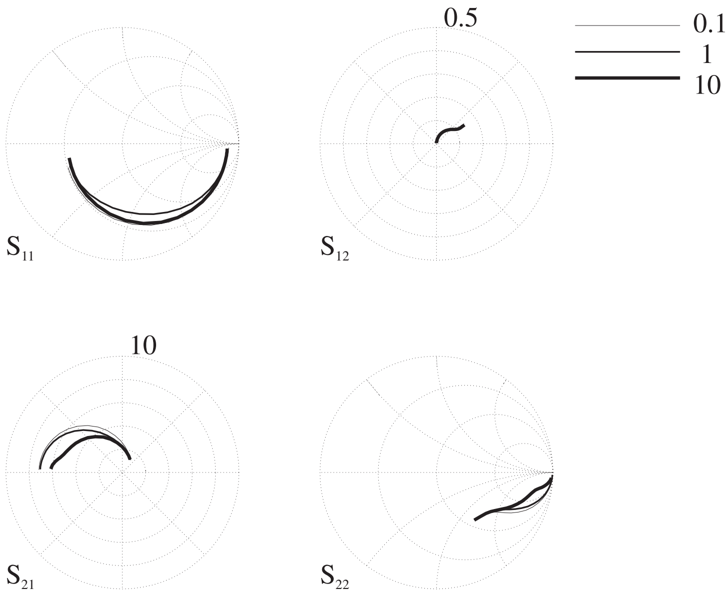

Figure 4.2: Calculated S-parameters for three different values of R_{Bcont}

The parameter C_{BCext} has a greater impact on S_{22} than it has on S_{11}. It can however be observed that at high values of C_{BCext}, the input impedance at port 1 is shunted to port 2 which is terminated in 50 Ω thus causing the kink in S_{11} at higher frequencies, see Fig. 4.4 S_{11}. The shunting effect can be verified in S_{12} where the feedback coupling varies strongly with the different values of C_{BCext}. Due to the coupling in S_{12}, S_{22} is also strongly affected. At low C_{BCext}, the intrinsic transistor is not shunted which can be seen as a high impedance, see Fig. 4.4 S_{22}. At high values of C_{BCext} the intrinsic transistor is fully shunted and S_{22} corresponds instead to a parallel circuit consisting of the port 1 impedance (50 Ω) and the base-emitter impedance, thus giving a total impedance at port 2 which is slightly less than 50 Ω, see Fig. 4.4 S_{22}.

Input impedance from port 1 is clearly affected by R_{Blead}. At a high value the shunting via C_{BCext} will come into effect at high frequencies, see Fig. 4.5 S_{11},

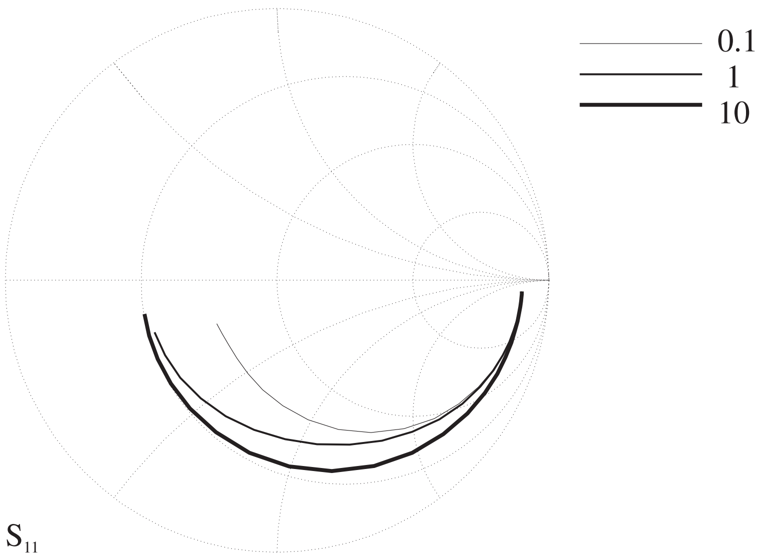

Figure 4.3: Calculated S_{11} *for three different values of* C_{Bshunt}*. Legend is the same as in Fig. 4.2.*

where the impedance is that of the lead consisting of C_{BCext}, R_{BCext}, R_C and the impedance of port 2 (50 Ω). This shunting can also be seen in Fig. 4.5 S_{12} where the feedback coupling increases at high values of R_{Blead}. The forward coupling (S_{21}) goes also down at high values of R_{Blead} which intuitively can be explained with that less signal becomes available to the intrinsic transistor, see Fig. 4.5 S_{21}. The interpretation of the impedance at port 2, see Fig. 4.5 S_{22}, gives that at high values of R_{Blead}, feedback coupling through the intrinsic part of the transistor via C_{BC} is blocked, thus giving a high impedance. At higher frequency the intrinsic transistor in series with R_{Blead} is is shunted by C_{BCext}. It should be pointed out that the effective impedance seen from port 2 is at all frequencies higher for the high value of R_{Blead} than for the other values of R_{Blead}. The crossing of the different curves in the Smith chart for S_{22}, see Fig. 4.5 S_{22}, can thus not be used for immediate conclusions of the impedance. The collector-lead resistance, $R_{Cundepl}$, has mainly an impact on the impedance at port 2 which increases with increasing $R_{Cundepl}$, see Fig. 4.6 S_{22}. Similar variation as the one caused by a variation of $R_{Cundepl}$ in S_{22} is seen from a variation of R_C. The impact on S_{11} is however then negligible.

An increase in $R_{Cundepl}$ appear to increase the impedance at port 1, see Fig. 4.6 S_{11}, but the magnitude of the impedance is instead decreasing with an increasing $R_{Cundepl}$ except for very high frequencies (above 40 GHz). This can not be clearly distinguished from the Smith chart as it does not contain any direct frequency information. An explanation for the decrease in impedance with an increasing $R_{Cundepl}$ can be found in how the current i, see Fig. 4.1a, is shunted from r_{BE} via $R_{Cundepl}$.

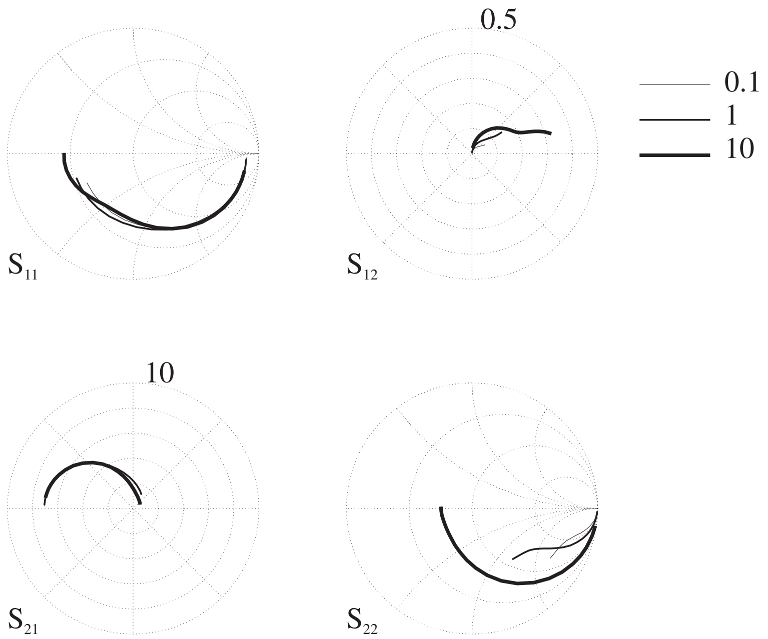

Figure 4.4: Calculated S-parameters for three different values of $\mathrm{C}_{\mathrm{BCext}}$. *Legend is the same as in Fig. 4.2.*

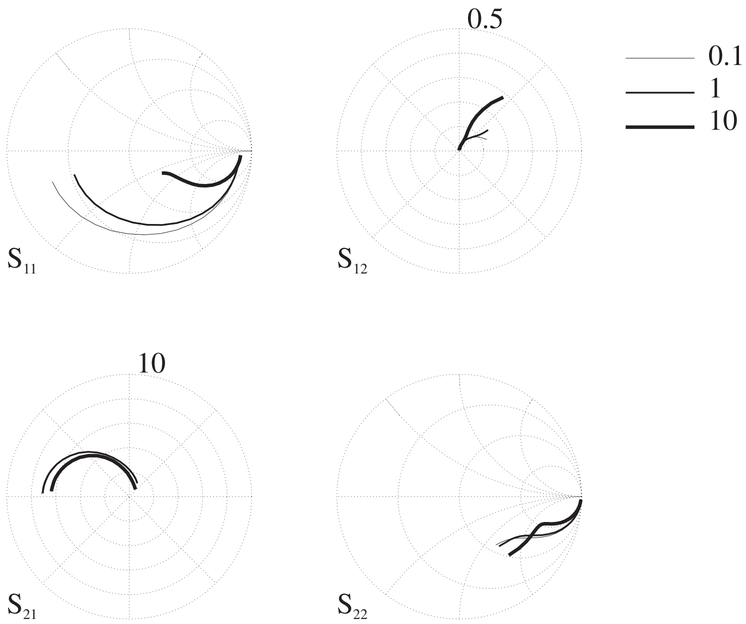

Figure 4.5: Calculated S-parameters for three different values of R_{Blead}. *Legend is the same as in Fig. 4.2.*

With a lower shunt of i, the current generator (βi) also conducts more current which is interpreted as a lower impedance. The fact that a variation of R_C does not affect S_{11} supports this explanation.

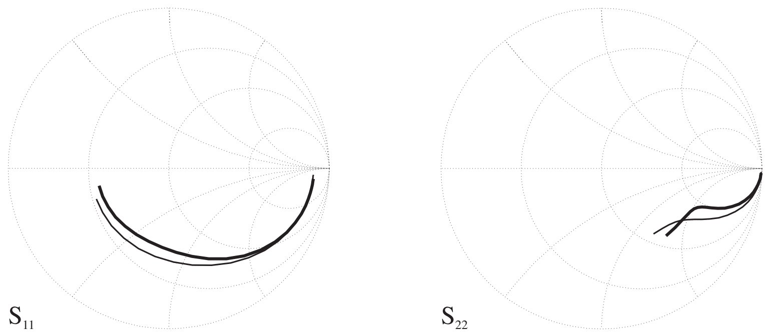

Figure 4.6: Calculated S_{22} *for three different values of* $R_{Cundepl}$. *Legend is the same as in Fig. 4.2.*

The emitter-contact resistance, R_{Econt}, has a great impact on several parameters, also parameters related to DC, e.g., collector current and thus the bias point, which makes it very difficult to make any simple interpretation of the result of a variation of this parameter. The curves in Fig. 4.7 are included to point out directions of the different S-parameters for a variation of R_{Econt}. Similar variation can be noticed for a variation of $R_{Eundepl}$ and the resulting S-parameters for a variation of $R_{Eundepl}$ has thus not been included.

The intrinsic base-collector capacitance (C_{BC}) has an impact on the input impedance of port 1. Indeed, the input impedance calculated from S_{11} in Fig. 4.8 shows a decrease with increasing capacitance for all but the highest frequencies (i.e., frequencies below 45 GHz) as would be expected. At the highest frequencies, the delays in the transistor seems to act as inductances which may cause resonance phenomenons together with the capacitances thus increasing the impedance. This was verified by setting the delays in the transistor to zero which yielded the same behavior at higher frequencies as the one described for lower ones. Due to the absence of immediate frequency information in the Smith chart, the impact of a capacitance variation is not obvious in Fig. 4.8 S_{11}. The shunting can clearly be seen in Fig. 4.8 S_{22} which indicates a lowering in impedance seen from port 2. At higher frequencies the base-emitter impedance becomes dominant which leads to a further decrease of the impedance, seen as a kink for all three curves in Fig. 4.8 S_{22}.

In a similar way as the input impedance on port1 is affected by a variation of C_{BC}, it is also affected by a variation of C_{BE}, see Fig. 4.9 S_{11}. The magnitude of the impedance is however continuously decreasing with increasing C_{BE} for all frequencies. The input impedance of port 2 is also strongly affected, see Fig. 4.9 S_{22}. It is slightly counterintuitive that a higher capacitance should result in a higher impedance, which however is the case, see Fig. 4.9 S_{22}. The capacitance is shunting

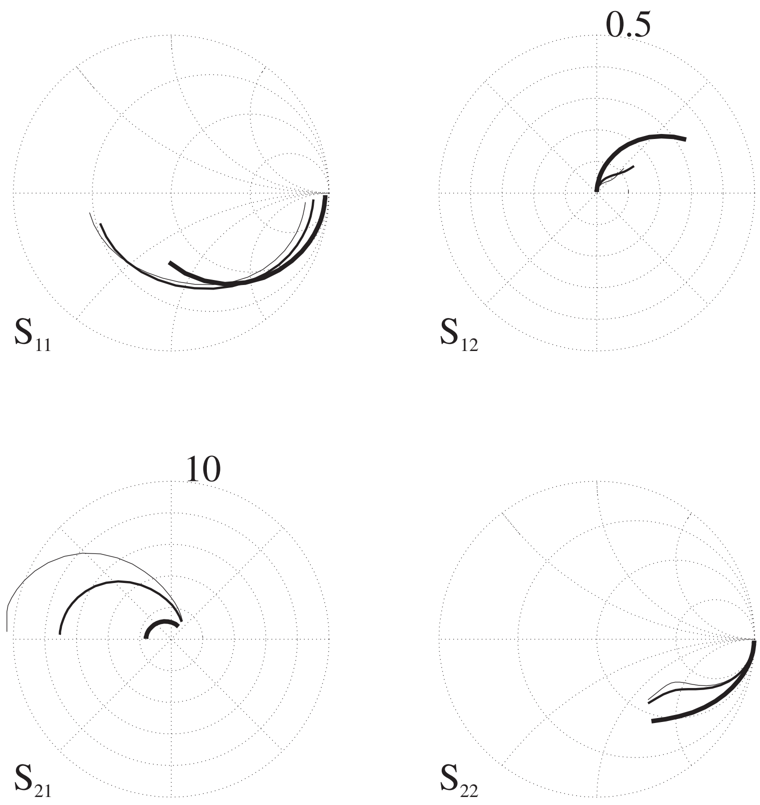

Figure 4.7: Calculated S-parameters for three different values of $\mathrm{R_{Econt}}$*. Legend is the same as in Fig. 4.2.*

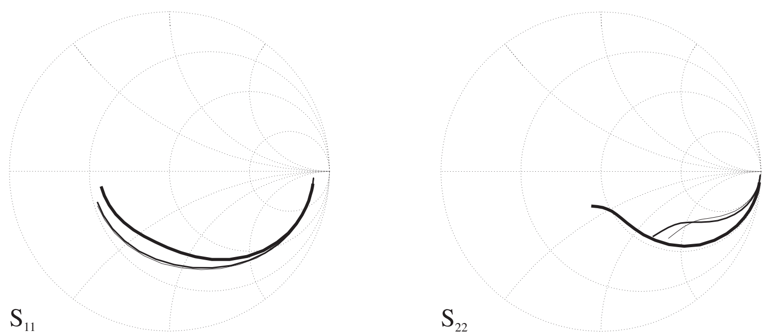

Figure 4.8: Calculated S-parameters for three different values of $\mathrm{C_{BC}}$*. Legend is the same as in Fig. 4.2.*

the base-emitter junction and is thus also affecting the injection of carriers into the base. This causes a decrease of current in the collector lead for a given voltage variation which is interpreted as an increase in impedance.

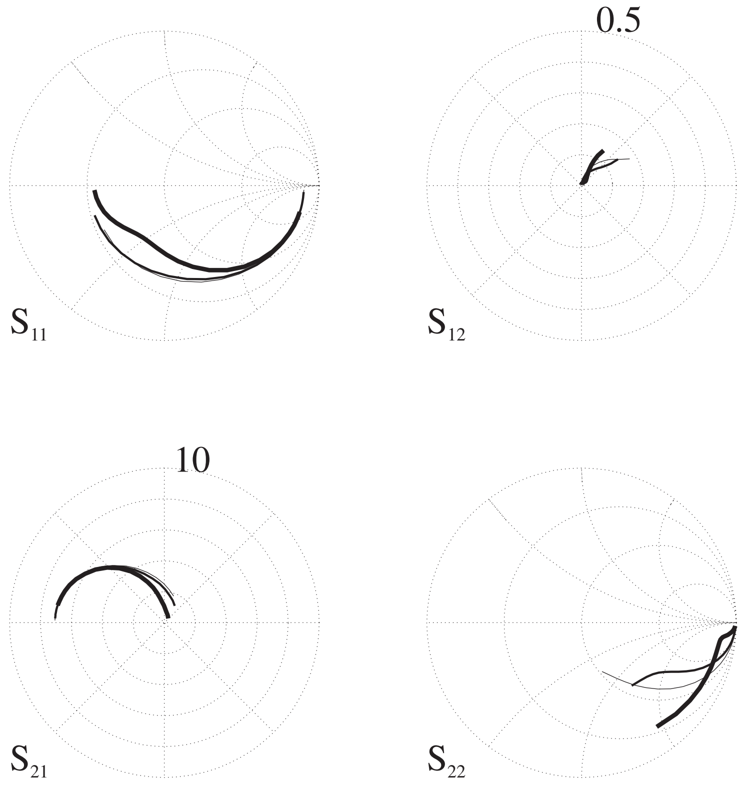

Figure 4.9: Calculated S-parameters for three different values of C_{BE}. *Legend is the same as in Fig. 4.2.*

The impact from a variation of the total delay through the transistor, τ, has similarities to those of variations of C_{BE} and C_{BC}. Conclusions are however difficult to draw from the S-parameters and the curves are thus here included to indicate the effects of variations in τ.

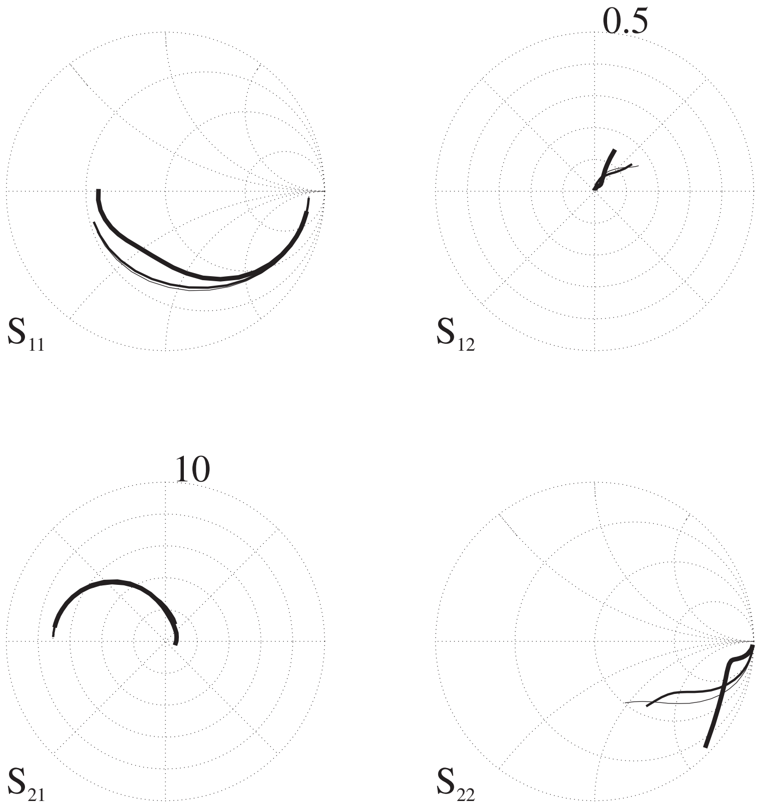

Figure 4.10: Calculated S-parameters for three different values of τ. Legend is the same as in Fig. 4.2.

Chapter 5

Low-frequency noise in semiconductors

5.1 Background

Excess noise, flicker noise, 1/f-noise and burst noise are some of the names used for the noise often found in the low-frequency region of noise measurements. Depending on the type of noise, the physical origin of the noise is differently well understood. For some types of noise, there exists essentially only empirical relations defining the possible levels of the noise. The characteristic appearance of the noise is differing, but in general the noise power spectral density decreases with increasing frequency and drops below the white noise level occurring in all kinds of systems, thus the meaning of low-frequency noise.

In the measurement part of this work, no specific distinction between the different kinds of noise occurring will be made. From a measurement point of view they can be treated equally and it is mainly in the physical interpretation of the individual noise sources that the individual characteristics are of importance.

5.2 Mathematical representation of noise

In the following text, noise will be presented with its *power spectral density* (PSD), denoted with an S. The word *power* indicates only a square dependence on the noisy signal and does not necessarily have anything to do with energy. The PSD is here defined as [36]:

$$S_{xy}(f) = \lim_{T\to\infty} \left\{ \frac{\overline{\mathcal{F}(x(t))(f) \cdot \mathcal{F}(y(t))^{*}(f)}}{T} \right\} \tag{5.1}$$

where $x(t)$ and $y(t)$ are signals in the time domain, $\mathcal{F}$ denotes the Fourier transform into the frequency domain and T is the length of the truncated time samples. The bar indicates an ensemble average, i.e., an averaging of several "parallel" signals.

A PSD is by definition a product where the components are indicated by the indices. The PSD is however often a product of only one signal and the indices would thus be identical. In this text these PSDs will be presented with only one index.

For measurements of two different noise signals, a coherence (γ) between them which indicates signals from a common source can be calculated as [36]:

$$\gamma^2 = \frac{S_{xy}^2}{S_x S_y} \tag{5.2}$$

where the notation described above has been used in the denominator (single indices). The coherence is a complex number, but usually the magnitude is of major concern. This is a number in the range from 0 to 1 where unity indicates identical *behavior* of the signals, however the amplitude may differ. A low coherence is not sufficient to assure that the different measured signals do not have the same physical origin [37].

5.3 Appearance of different types of noise

Different kinds of noise are shown in Fig. 5.1-5.4 and described below. They should mainly serve as suggestion to how different types of noise may appear in the time domain and how their respective PSD will appear as an instant and averaged sample. An approximation of the PSD calculated from an instant sample is however an extreme simplification of eq. 5.1 and is not describing the type of noise very well. An averaging of several PSDs is thus also performed and shown. The reason for still including the approximation of the PSD from a single instant sample is because this is the view of the signal found when performing measurements using a signal analyzer [38] which is a commonly used instrument for noise characterization.

The different noise types will only be discussed very briefly, the scales in the different plots are arbitrary.

The first three types of noise are included for their shape of the PSDs whereas the fourth shows a very particular kind of noise in the time domain and how it may create a very special PSD which may be confused with $1/f$ noise over a limited bandwidth.

5.3.1 White noise

Noise, given by fundamental physical laws and thus impossible to extinct completely, often has a flat PSD as seen in Fig. 5.1. This type of noise is often called white noise. Comparing the measured level of such noise with calculated minimum levels due to the intrinsic noise sources of the device under test can give an indication on whether there exists excess noise in the given frequency range or not.

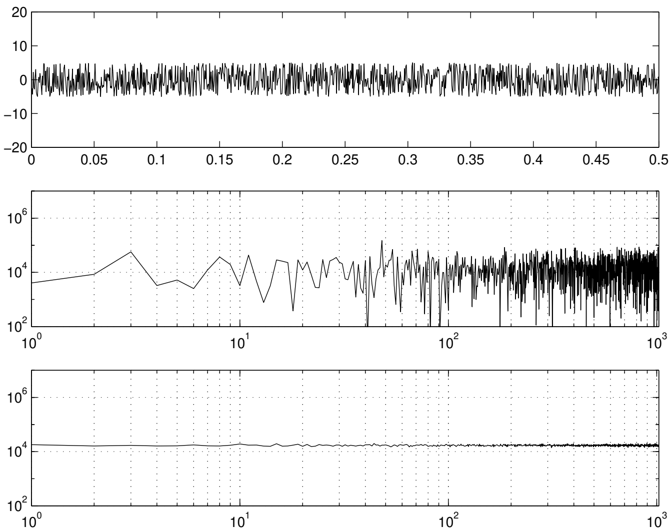

Figure 5.1: Plots of white noise. top: time domain, middle: the corresponding PSD based on a single time sequence, bottom: an average of 300 sequences. The units of the graphs are arbitrary.

5.3.2 Lorentzian type

The frequency dependence of the noise which has a so-called Lorentzian PSD is flat for low frequencies and falls with a $1/f^2$-dependence for high frequencies. A typical noise source for this type of PSD is trapping and de-trapping processes, e.g., generation-recombination (GR) noise [39]. Due to its frequency dependence, superimposed GR-noise on $1/f$-noise will appear as a bump on the $1/f$-spectrum.

5.3.3 $1/f$ noise

The true $1/f$ noise is shown in Fig. 5.3. It has a $1/f$-dependence in the PSD. In practice, the slope may have a dependence as $1/f^\delta$ where $0.8 \leq \delta \leq 1.2$. As of now, there exists no complete physical understanding of the $1/f$ noise in semiconductors. A mobility fluctuation of the charge carriers in the semiconductor due to lattice scattering has been suggested which very well models the electrical behavior of the $1/f$ noise as a bulk effect [40]. An empirical parameter, the Hooge parameter (α), is necessary. The following empirical relation for $1/f$ noise is found:

$$\frac{S_X}{X^2} = \frac{\alpha}{fN} \tag{5.3}$$

where X is the steady state value of the signal $x(t)$ having the specific $1/f$ dependence in the PSD and N is the numbers of free carriers (homogeneously distributed)

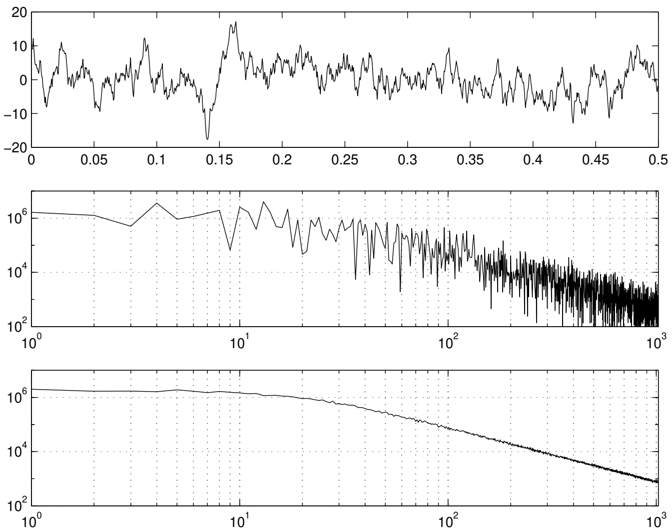

Figure 5.2: Plots of noise with a Lorentzian roll off. top: time domain, middle: the corresponding PSD based on a single time sequence, bottom: an average of 300 sequences. The units of the graphs are arbitrary.

in the measured sample. The Hooge parameter (α) is dimensionless and substantial work has been performed [41][42] in characterizing different materials for its value. It is for semiconductors found in the range $10^{-6} \leq \alpha \leq 10^{-3}$.

In addition to the lattice scattering model for the 1/f noise in semiconductors, also a fluctuation in the number of free carriers has been proposed [43] as an origin of the 1/f noise. The fluctuation in numbers would then be caused by trapping and de-trapping processes with a distribution of time constants. A weighted superposition of the different spectra would then give a 1/f spectrum.

5.3.4 Random Telegraph Signal

The Random Telegraph Signal (RTS) noise is a special case of trapping-de-trapping process which involves one or more carriers in a set of very few carriers. The trapping-de-trapping of a single carrier will thus have great impact on, e.g., the current. Depending on the likelihoods of the trapping center being either occupied or vacant, the two major levels of the signal will be occupied for different amounts of time, see Fig. 5.4(a) where the probabilities for the trapping and the de-trapping are very different.

The existence of more than one trapping center is possible which will give more than two major levels in the signal (not shown here).

Due to the trapping-de-trapping process, the PSD will have a Lorentzian behav-

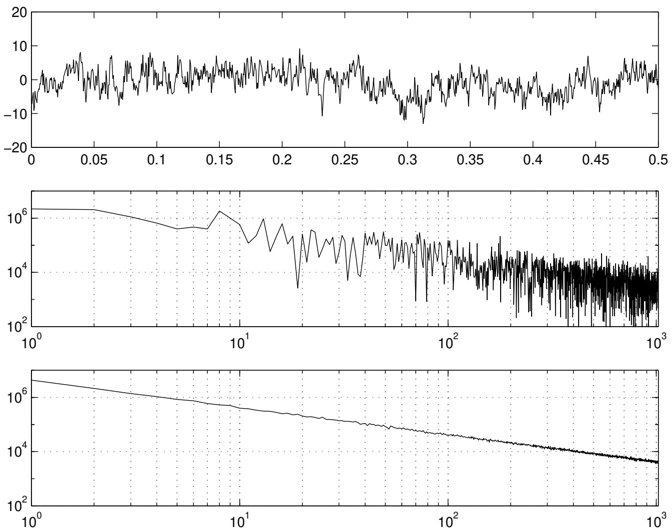

Figure 5.3: Plots of noise with a $1/f$ PSD. top: time domain, middle: the corresponding PSD based on a single time sequence, bottom: an average of 300 sequences. The units of the graphs are arbitrary.

ior which will roll off at higher frequencies into the background noise. Because of the roll-off, the slope of the PSD will never quite reach the $1/f^2$ and is thus likely to be mistaken for a $1/f^\delta$ behavior.

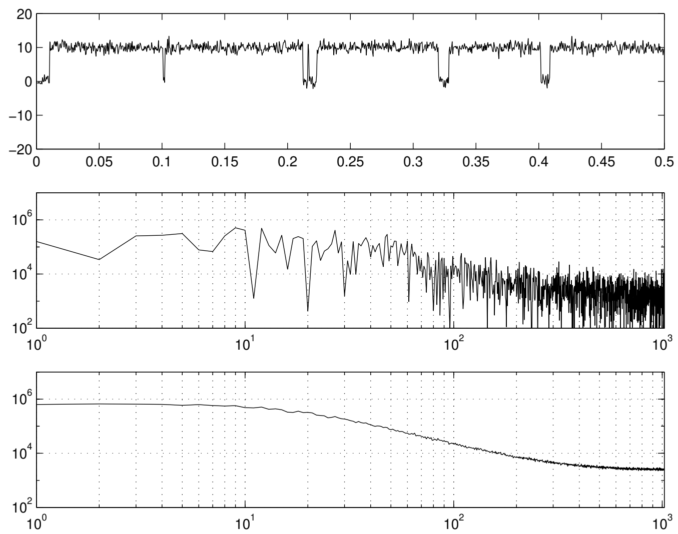

Figure 5.4: Plots of RTS noise. top: time domain, middle: the corresponding PSD based on a single time sequence, bottom: an average of 300 sequences. The units of the graphs are arbitrary.

5.4 Representation of low-frequency noise sources in SPICE

As the more or less industry standard general modeling tool for circuit analysis, including bipolar transistors, SPICE and its derivatives are widely used and thus deserves a brief presentation. A deeper investigation of the available tools for noise analysis is neither the intent, nor within the scope of this work. It suffices here to observe that the treatment of low-frequency noise in SPICE is not complete. As an example, the inclusion of both a noise source having a $1/f$ PSD and a noise source having a Lorentzian PSD would not be possible.

The noise modeling in SPICE consists of thermal noise for all real resistances and of shot noise, having a white noise appearance, for the two junctions of the transistor [17]. These sources all have a flat frequency spectrum. The modeling of low-frequency noise is accounted for by two parameters: a_f and k_f, in SPICE2 (an enhancement of the original SPICE) called Af and KF respectively. These are implemented as (defining it as PSD):

$$S_{i_B} = 2qI_B + k_f \frac{I_B^{a_f}}{f} \tag{5.4}$$

where the source is situated in parallel with the base-emitter junction. In PSPICE an additional source is added for the noise in the base-collector junction. The expression is identical to eq. 5.4 with the exception that the index B is exchanged with C to reflect the different junction.

The low-frequency noise sources in the SPICE-based simulator may be sufficient for certain modeling purposes and the dominant noise source in BJTs can indeed be found in the base-emitter junction [44]. For transistors with a polysilicon/monosilicon interface in the emitter however, the dominant noise source may very well be in the emitter [37] and the modeling using extracted data for the SPICE parameters may thus only be valid for circuit configurations and bias reflecting the one used at the time of parameter extraction. Care must be taken not to use the model in circuit configurations where the used noise parameters will not yield a correct noise output. A different set of noise parameters acquired from an extraction similar to the circuit configuration in use may resolve the modeling problem, but the result would be two or more parameter sets for the same transistor. If the noise modeling is of importance, a more refined model employing noise sources in new locations within the device should be considered. One modeling approach is to use noise sources with physical relevance. The benefit with such a modeling is that when it is correctly done, it will show improved scalability and circuit compatibility in comparison with a model employing solely empirically derived noise sources.

Chapter 6

Measurement of low-frequency noise

6.1 Background

The following text will describe measurement issues for both general cases and more specific ones regarding the measurement of noise in typical BJTs. Several topics will not have immediate scientific value, but are included for completeness. They are there to point out what, in the view of the author, deviates from generally applied measurement techniques for low-frequency noise.

To measure the mathematically defined PSD, a waveform in the time domain is sampled (for example with an A/D-card, digital oscilloscope or a signal analyzer) and converted to a complex-valued spectrum using the fast Fourier transform (FFT). Using eq. 5.1 it is then possible to calculate the PSD.

Two instrumental issues need to be addressed in order to have correct measurements. The first is the *dynamic range* of the measurement equipment. As the PSD spectrum contains a wide range of signal levels it is important that the measurement equipment can resolve the lowest level in presence of the highest level input to the equipment. In the time domain this can be seen as resolving the weakest signal which is superimposed on the strongest signal. Power line signals and harmonics of this frequency interfering with the measurements can create strong peaks in the frequency domain which can't be fully eliminated.

A rough estimate for A/D-converters is that the dynamic range is below or equal to $6dB/bit$ and thus an 8 bit A/D converter maximally has a $48dB$ dynamic range whereas a 16 bit A/D-converter maximally has a $96dB$ dynamic range.

The second issue of importance is the *analog bandwidth* of the measurement equipment. In order not to loose dynamic range in an offset of the input signal, the sampler should be put in an AC-mode and thus an analog circuit is necessary. Digital signal analyzers claiming mHz measurement capabilities are thus referring to a DC-mode where the sampling clock is set sufficiently slow. Active devices could possibly be employed for subtracting the input offset and thus being able to perform extremely low-frequency measurements. Such options have however not been investigated and it necessitates DC-mode throughout the whole measurement system which may pose big difficulties in the amplifiers.

6.2 Measurement setup

A schematic setup for performing common-emitter current noise measurements on a BJT is shown in Fig. 6.1. The amplifiers are in series with the base and collector current lead respectively and thus measures the fluctuation in the different currents. Using a signal analyzer, the signals are sampled simultaneously and PSDs are calculated. The true double channel sampling is important in order to be able to calculate the coherence between the signals.

Not shown in Fig. 6.1 is a computer controlling the data acquisition from the signal analyzer. The big amounts of data and the long time necessary for the averaging of the PSDs makes a computer very useful. A single measurement in an averaged PSD spanning from $2Hz$ to $100kHz$ may take up to 10 minutes in time. For characterization purposes, more than ten sets of such measurements may be necessary, e.g. when sweeping a bias current or an external device termination such as the base resistance. Ideally, all parameters of the measurement setup (bias, circuit termination etc.) should be computer controlled in order to run measurements overnight when external disturbances can be expected to be the lowest and more measurement points can be allowed.

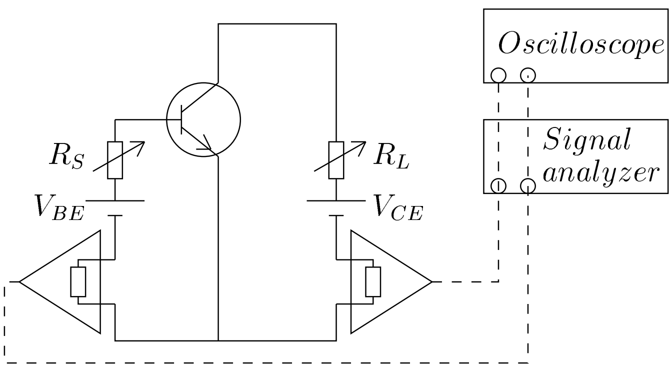

Figure 6.1: Measurement setup for a transistor in common-emitter configuration.

From Fig. 6.1 it is seen that an oscilloscope is included in the measurement setup. For the acquisition of data this is not necessary, but it is very useful for monitoring the actual signal which is to be sampled by the signal analyzer. During probing and setting of correct bias point, the oscilloscope will give valuable information as to whether the measured signal indicates noise that possibly originates within the device or is only caused by external effects like power line interference or bad contacts. The oscilloscope is also very useful to monitor the signal throughout the measurement to see if the amplifier may saturate or the behavior of the signal changes. The former may result in a faulty spectrum and the latter indicates, e.g., a degrading contact between the device and the probe tips.

Using the instant display of the measured signals, different types of noise can also be identified. The identification depends a lot on experience since different kinds of noise and undesired disturbances often interfere. The graphs in 5.3 showing the time domain signal may serve as a suggestion as to what can be seen on the oscilloscope screen.

The setting of the sweep time of the oscilloscope is of great importance when studying the measured signal. As there is no distinct frequency of the signal to observe, it is necessary to step through several sweep time settings in order to see if there are disturbances of, e.g., power line, seen at long sweep times. Possible oscillations within the device under test (DUT) or the amplifiers may appear as noise if the sweep time is not set short enough for the oscilloscope to resolve the oscillating signal. Furthermore the triggering of the sweep should be switched between the channels of the oscilloscope if any particular disturbance is suspected.

6.2.1 Verifying integrity of measurement setup

An important issue when performing sensitive measurements as noise measurements is to assure the integrity of the measurement setup. Although obvious, it is an important point to stress. Without good understanding of what kind of noise to expect and the noise floor of the equipment setup, the risk of simply measuring noise from the measurement equipment is apparent. After an initial measurement of a DUT, the acquired noise levels should be compared with the ones that can be expected from the measurement equipment when measuring a noiseless device. Especially, induced noise as discussed in 6.4.1 tends to be difficult to detect immediately as its impact depends on parameters within the DUT.

6.2.2 Bias control

Biasing of the DUT has been realized using passive elements with low intrinsic noise. Separate batteries are used for the base and collector in order to reduce possible conductor loops. Biasing of the collector is fairly simple since there is very low feedback to the base and thus induced noise has very low impact on the measurement. A $1.5V$ battery in series with a variable resistor has been sufficient for common-emitter measurements.

The output load resistor (R_L in Fig. 6.1) is mainly important during voltage noise measurements, but can also serve as a current limiter when the initial biasing of the circuit is performed. During voltage noise measurements, the voltage fluctuation is measured at the collector node using a voltage amplifier.

For the biasing of the base, a more complex setup is necessary. The base current must be precisely controlled. Low levels are easiest controlled using the base-emitter voltage and high current levels are easiest controlled using a current limiting resistance. While maintaining a well defined DC base current, the AC termination of the base is very important to control independently. A circuit which meets these demands is shown in Fig. 6.2. The positioning of a transimpedance amplifier when measuring both AC and DC parts of the current is also shown.

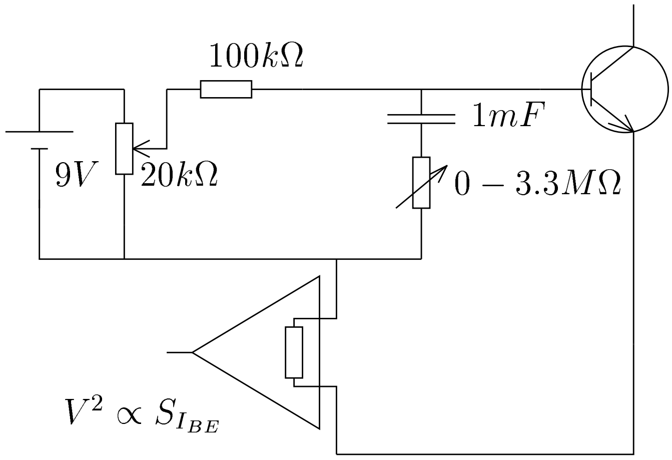

Figure 6.2: Schematic of how the base biasing is performed.

For low currents, the base-emitter voltage is controlled using the wire wound $20k\Omega$ 10-turn potentiometer, see Fig. 6.2. For higher base currents, the limiting $100k\Omega$ metal-film resistor will prevent a current rush due to the increased voltage from the potentiometer. Shunting the bias part is an electrolytic capacitor in series with a variable resistance realized using metal-film resistors and a switch with gold plated contacts.

Electrolytic capacitors are infamous for their bad noise characteristics, but measurements of the biasing setup indicate a voltage noise level below $3.2 \cdot 10^{-19} V^2/Hz$ at a frequency of $235Hz$ and an output voltage of $0.7V$ which is the equivalent of Nyquist noise from a 20Ω resistor. The frequency of $235Hz$ was chosen in order not to have any substantial power-line interference. The actual noise level may be lower, but this has not been possible to verify with available measurement equipment. The used capacitor was selected for its comparably low leakage current, approximately $0.05\mu A$ for a voltage drop of $1V$ and a one minute settling time.

Verifying measurements have been made on three electrolytic capacitors with $1000\mu F$, $50V$, $3300\mu F$, $50V$, $3300\mu F$ and $16V$ as nominal capacitance and highest voltage respectively. In order to measure the voltage and current noise, they were biased with a $1.5V$ battery through a $10k\Omega$ metal film resistor and the voltage noise was measured. An average noise level at 235Hz was found to be below $3.3 \cdot 10^{-19} V^2/Hz$, again limited by the accuracy of the measurement equipment. The current noise level should thus be below $3.3 \cdot 10^{-27} A^2/Hz$, calculated using eq. 6.1 in 6.3. In conclusion, the electrolytic capacitors seem not to be causing any noticeable noise in this configuration.

It is however very important to let the charge in the capacitors settle. In the first minute, the leakage current is higher, but slowly settles to its lower value. Beginning the measurement before the leakage current in the capacitor has settled is not advisable since both base and collector current will vary accordingly.

Due to the charging time and existing leakage in the dielectric capacitors, the practical setting of the bias current is best done using a two-step process: in the first step, the correct bias of the base current is set for a virtually disconnected shunting capacitor. This is done by setting the variable resistance (the $0 - 3.3M\Omega$ variable resistor) in Fig. 6.2 to its highest value and adjusting the potentiometer $(0 - 20k\Omega)$ so the desired base or collector current can be measured. In the second step the capacitor is reconnected by setting the variable resistance to the desired value of base termination for the AC signal. The voltage over the base-emitter junction will then drop due to the charge of the capacitor through the $100k\Omega$ resistance and it is necessary to wait until the base current has reached within 5% of desired value. It is possible to shunt the $100k\Omega$ resistance and also actively charge the capacitor to the right voltage. A working circuit is shown in Fig 6.3. By pressing the switch, the capacitor is completely disconnected and quickly charged using the op-amp to a voltage which is very much the same as over the base-emitter junction. When the switch is returned to the original setting, the op-amp is disconnected and the bias is close to the desired one. It has been noticed that the the bias drops slightly, i.e., the voltage over the base-emitter junction drops slightly when the capacitor is connected. This can be explained with leakage currents in the capacitor. Adjusting the base-emitter voltage slightly might thus be necessary in order to maintain the desired bias. For measurements where an extremely precise bias is requested, it would be necessary to wait for the charge within the electrolytic capacitor to settle. The delay (approximately 30 seconds) caused by feeding information about the used bias settings into the controlling program is however usually sufficient when performing measurements.

6.2.3 Thermal control

The device temperature is controlled using a Peltier element which is actively regulated by a PID regulator. The Peltier element is heating a 2 mm thick brass plate in which a temperature transducer (AD590) is mounted 0.5 mm under the surface, thus giving correct temperature feedback. The measured chip is fastened to the brass plate through vacuum which ensures good thermal coupling. The PID-regulator manages to maintain the temperature within $\pm 0.5^\circ$ K from set value in the active range. Such a small variation seems not to have a noticeable impact on the measured noise. The Peltier element is also electrically insulated from the measured device in order to minimize electrical disturbance from the necessary controller current flowing through the Peltier element.

The probe tip pressure on the device pads needs to be continuously monitored

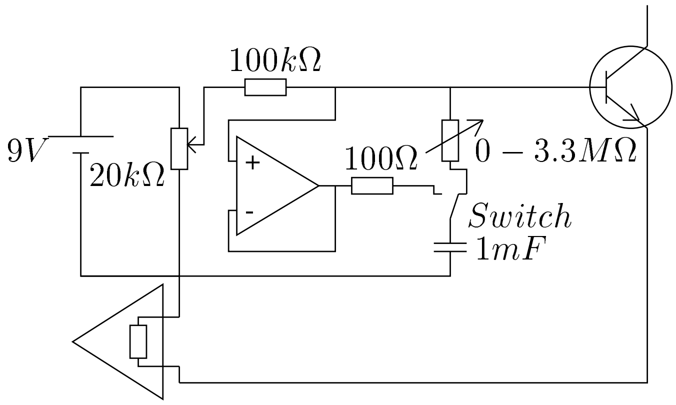

Figure 6.3: Circuit for fast setting of base bias current. The low power op-amp is powered from the 9V battery.

since it will vary due to thermal expansion and contraction of the chuck as the temperature changes. From practical observations a temperature variation of $20°C$ of the sample can be accepted without adjusting the probe tip pressure. An increased pressure leads to probe-tip travel which may destroy the device.

6.3 Measurements using voltage amplifiers

For the measurements of electrical noise there are two kinds of amplifiers that have been found to be very useful: the voltage amplifier and the transimpedance amplifier. They will be discussed briefly here.

Voltage noise can be directly measured using regular voltage amplifiers. When measuring signals from a high impedance output port, the input impedance of the amplifier must be taken into account. With an FET input stage of the amplifier, its impact on the DUT is minimal.

To measure current noise using a voltage amplifier, the noise current needs to be converted to an equivalent voltage. Running the current through a resistor facilitates this. Since there is a linear relation between the voltage and the current, there will be a quadratic relation between the PSDs as:

$$S_V = R^2 \cdot S_I \tag{6.1}$$

The quadratic relation can be used in case the voltage amplification is not sufficient. Increasing the value of the resistance will increase the PSD in a square dependence of the resistance. There are however two drawbacks with this technique. The first is that the DC voltage drop over the resistor may pose biasing problems. It is nearly impossible to shunt the DC current through an inductor since the size of the coil would become very big for the low frequencies and the coil would also pick up undesired power line noise. There are also situations, as will be described later, when high resistance values are disturbing the measurement and are thus unacceptable. The second drawback is that the noise of the resistor itself used for the conversion must be accounted for. Since this noise is linearly dependent on the resistance whereas the conversion in eq. 6.1 shows a quadratic dependence, an increase in resistance may reduce the problem.

6.4 Measurements using transimpedance amplifiers

The transimpedance amplifier is connected directly into the signal lead where the current noise will be measured, see Fig. 6.1. Through its active input, the input impedance can be very low while still maintaining a very high conversion factor from measured current to output voltage. Typical data for an ultra-low noise amplifier are shown in Table 6.1. The low input impedance is very important for measurement situations where the circuit resistance cannot be allowed to vary arbitrarily.

Table 6.1: Input impedance, conversion ratio and equivalent gain for the Brookdeal 5002 transimpedance amplifier.

Input impedance	Conversion ratio	Equivalent gain
1 Ω	1 $V/\mu A$	10^6
100 Ω	10 $V/\mu A$	10^7
10 $k\Omega$	0.1 V/nA	10^8

6.4.1 Issues with using transimpedance amplifiers

The transimpedance amplifier enables a very convenient way of measuring very weak current noise in a direct way. There are however some limitations, who will be pointed out here, that are necessary to be aware of in order to make proper use of the instrument.

Due to an internal feedback resistance within the transimpedance amplifier (R in Fig. 6.6) being several orders of magnitude greater than the effective input impedance of the amplifier, it is necessary that the DC impedance of the measured circuit (R_{circ} in Fig. 6.6) well exceeds the input impedance of the transimpedance amplifier. Otherwise the amplifier may latch up internally and the output signal will be disturbed. A practical circuit DC resistance being a decade higher than the input impedance (compare Table 6.1) of the amplifier has been found to be sufficient.

The active input of the transimpedance amplifier will induce noise into the measured circuit. The level of this noise can be directly measured as in Fig. 6.4 and was for a Brookdeal 5002 found to be $S_{V_{Tamp}} \approx 1.3 \cdot 10^{-16} V^2/Hz$ at a frequency of 235 Hz, for all range settings.

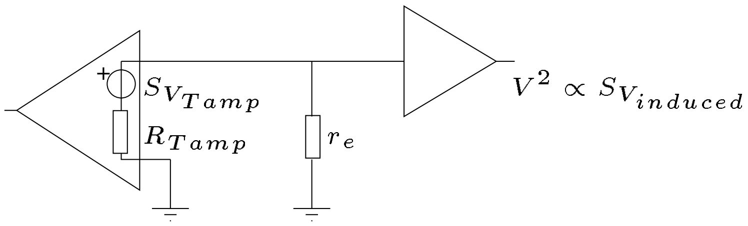

Figure 6.4: Schematic setup for measuring the output voltage noise from the active input of the transimpedance amplifier.

For measurements employing only one amplifier this noise seldom causes any problems since it is not affecting the output signal of the own amplifier more than possibly defining a slightly high noise floor. In measurement setups employing more than one amplifier, e.g., when measuring both base and collector current noise in a BJT, the induced noise can indeed be detrimental to the results. The induced noise will be further discussed in 6.5. A method of partly circumventing the problem is discussed in *Paper VII.*

6.5 Externally induced noise related to the measurement setup

The setup for performing on wafer low-frequency noise measurements on BJTs is technically not very complex. Due to the very low signal levels however, there are several issues regarding externally induced noise that needs to be addressed. The main causes for additional noise are:

- Large currents in conductors
- Wire loops causing electromagnetic coupling of, e.g., power line signal
- Mechanical vibrations
- Noise induced from the measurement equipment

The different effects manifest themselves in different ways in the measured noise.

6.5.1 Noise from current in conductors

Currents through lines with non-negligible resistance will create a voltage noise which may be induced into the DUT or sensitive points within the measurement equipment and thus create additional noise in the output. By carefully designing the setup in a way that large currents, e.g., supply currents for the amplifiers etc., do not flow through wires aimed for the measurement circuit, the noise can be reduced.

6.5.2 Noise from external coupling

Due to wire loops, magnetic fields can induce currents which will cause disturbances. Power line interferences are easily detected as peaks in the PSD at given frequencies. With a high resolution in the frequency spectrum, the fundamental frequency and some of its harmonics can thus easily be discarded. For higher harmonics, the resolution in the frequency spectrum may be limited and the spectrum is cluttered which appears as a bump in the low kHz range. Other sources of low-frequency electromagnetic radiation are CRTs. Specifically, interference originating in the necessary measurement equipment has been identified. The way of reducing the interference has been to move the equipment away from the DUT.

A way of practically reducing the pick-up of interfering signals is to have the cables leading the weak signal enclosing an as small area as possible since the magnetically induced currents are area dependent [45]. The conventional setup with the signal cables leading to the probes via the micro manipulators should thus be avoided. Both signal cables leading in parallel away from the probes and mounting the amplifiers and bias supplies as closely together as possible has provided a satisfactory measurement setup.

External shielding of the setup probably lowers interference, but the disadvantages of not being able to access the setup for changing settings etc. makes this option less attractive. If a shielding is desired, the shielding material should have high permeability in order to suppress interference from the low-frequency magnetic fields caused by power-line currents etc. Iron or Mumetal should be chosen as one layer of shielding material. All electrical connections through the shielding box should be made at one point for grounding purposes. As a rule of thumb, the shielding should be tight enough not to admit any light passing through, in order to prevent any high-frequency coupling through the shield [46]. As an example, during unshielded measurements, the typical time slots of the GSM standard have been identified. This indicates that mobile phones and base stations interfere with the measurements. Depending on the DUT, the disturbances are differently pronounced.

A three layer shielding box of dimensions $500 \times 500 \times 300mm^3$ has been used for shielded measurements performed at the Technical University of Eindhoven, The Netherlands. The box walls were composed of $3mm$ Arco transformer steel, $0.5mm$ Mumetal foil and a $1mm$ Aluminum outer shield. Interfering signals, e.g., power-line disturbances, were detectable, but strongly suppressed.

6.5.3 Noise from mechanical vibrations

Mechanical vibrations of the measurement setup cause the electrical contact between the probe tips and the contacting pads of the DUT to vary. Depending on the contacting surface of the DUT pads and the noise level of the DUT, the impact on the measurement is differently pronounced. Transistors without metallization, having only silicide contacting pads were found to be unmeasurable as the signal clearly deteriorated a very short while after contacting with the probe tips. Using an approximately $1\mu m$ thick metallization layer for the pads resolves most of the contacting problems and the impact of vibrations on the measurement is reduced to an acceptable level.

From practical experience, a varying vacuum caused by the intermittent running of the vacuum pump and vibrations in the building are major sources of undesired noise which is easily distinguishable on the instant display of the measured signal on the oscilloscope screen.

Mounting the probe station on a heavy concrete table and upgrading the vacuum pump has lowered disturbance of undesired noise. Placing the measurement equipment on a stable floor (e.g. in the basement of a building) should further improve the rejection of vibrations.

6.5.4 Noise from the measurement equipment

For certain circuit configurations, noise of the active input of one of the transimpedance amplifiers may be induced into the DUT and dominate the output noise which is measured by the other transimpedance amplifier. A typical situation where the above described situation may occur is shown in Fig. 6.5. The schematic representation of the amplifier is added with a voltage noise source which will output a noise into the measured device (shown as a BJT small-signal circuit within the rectangle with dashed lines). The amplifier on the collector side is omitted in Fig. 6.5 as its impact on measurements is negligible due to the low feedback from collector to base. Counterintuitively for the base transimpedance amplifier, the voltage noise source within the amplifier will usually not affect the output of the own amplifier.

Consequently, a coherence in the two signals that ideally should be measured is obscured by a disturbing signal. What is important to notice is thus that the amplifier *inducing* the erroneous signal may still output a correct signal. At low-impedance termination of the base, the intrinsic output noise in the collector lead may be strongly decreased [44] and thus go below the level of the transferred part of the induced noise. The output current PSD in the collector lead due to the induced voltage noise ($S_{V_{Tamp}}$) from the amplifier can be approximately calculated as:

$$S_{I_{transferred}} = S_{V_{Tamp}} \left(\frac{h_{fe}}{R_{Tamp} + R_S + r_b + r_\pi + (1 + h_{fe}) r_e} \right)^2 \qquad (6.2)$$

where R_{Tamp}, r_b and r_e have been included for completeness. They can often be considered negligible in comparison with r_π and thus omitted.

An explanation to the seemingly strange behavior of the transimpedance amplifier, inducing noise into the circuit, but not being affected at the own output, is shown in Fig. 6.6. The transimpedance amplifier is composed of a low noise differential voltage amplifier having a gain, G, with a feedback resistance (R in Fig. 6.6) which gives the conversion magnitude between current and voltage. The input impedance of the transimpedance amplifier, as seen in, e.g., Fig. 6.5, can be estimated as $R_{Tamp} \approx R/G$. Due to the non-ideal grounding of the positive input of the amplifier, the noise at this input node (shown as v^+ in Fig. 6.6) will be transferred to the negative input node (shown as v^- in Fig. 6.6) and thus output to the measurement circuit. The same noise will occur at the output of the amplifier, but compared with the converted current noise of the measured circuit, it is usually

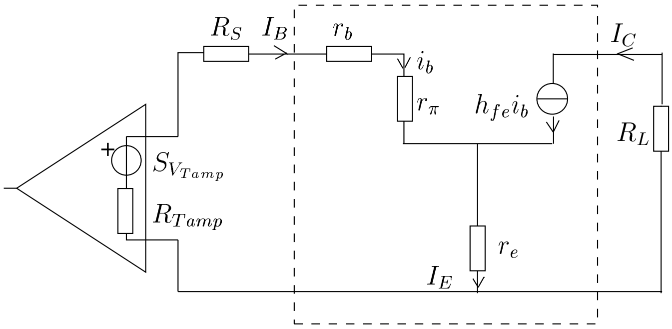

Figure 6.5: Schematic model of measurement situation where the active input of the transimpedance amplifier measuring the base current may induce noise which is transferred into the collector lead. The circuit within the dashed lines shows the small-signal equivalent of a transistor in common-emitter configuration.

considered negligible. The output voltage PSD caused by $S_{V_{Tamp}}$ can be estimated as (see Fig. 6.6):

$$S_{V_{out}} = S_{V_{Tamp}} \left(\frac{G}{1 + \frac{GR_{circ}}{R_{circ}+R}} \right)^2 \tag{6.3}$$

where R_{circ} is the resistance to ground seen from the input of the transimpedance amplifier. Noticing that $R \gg R_{circ}$, eq. 6.3 can be simplified to:

$$S_{V_{out}} = S_{V_{Tamp}} \left(\frac{G}{1 + \frac{R_{circ}}{R_{Tamp}}} \right)^2 \tag{6.4}$$

In a typical measurement situation with $G \approx 10^5$, $R_{Tamp} = 100\Omega$, $S_{V_{Tamp}} \approx 1.3 \cdot 10^{-16} V^2/Hz$ at a frequency of $235Hz$ and $R_{circ} = r_\pi \approx 26k\Omega$ at a bias of $I_B = 1\mu A$, the output voltage noise corresponds to an input current noise of approximately $2 \cdot 10^{-25} A^2/Hz$ which is lower than the shot noise of a diode at this bias current.

By removing the transimpedance amplifier, the induced noise is reduced to the noise originating in the biasing supply as discussed in 6.2.2.

A way of lowering the induced noise from the transimpedance amplifier while still being able to measure the base current noise is shown in Fig. 6.7.

By properly choosing the values of the partitioning factor η and R_{shunt} in Fig. 6.7, a trade-off between sensitivity and induced noise may be found. The reduction factor for both amplification of current noise from the DUT and the output voltage noise level from the transimpedance amplifier into the DUT is (provided $R_{shunt} \gg R_{T_{amp}}$ in Fig. 6.7):

$$\kappa = \left(\frac{\eta}{1+\eta} \right)^2 \tag{6.5}$$

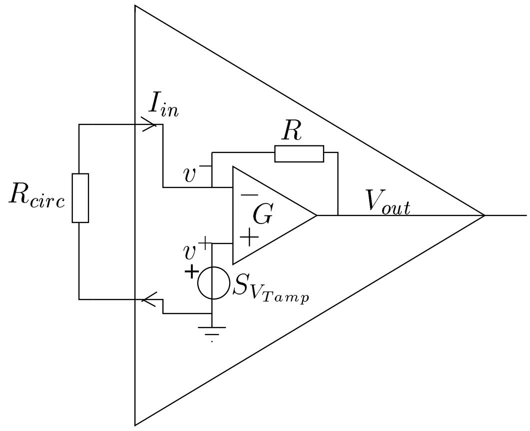

Figure 6.6: Schematic model of the transimpedance amplifier including the source of the voltage noise at the input.

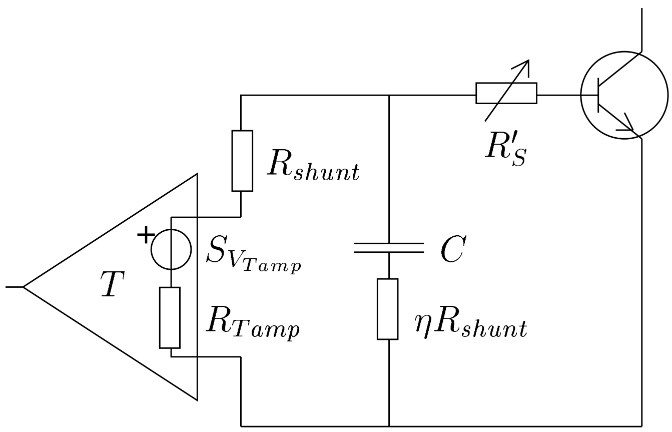

Figure 6.7: Schematic of how the induced noise from the transimpedance amplifier can be reduced through a shunting configuration.

Thus, the output voltage signal from the transimpedance amplifier corresponds to $\kappa T^2 S_{I_{BE}}$ and the induced noise is reduced to $\kappa S_{V_{Tamp}}$. The factor T is the conversion factor from current to voltage of the transimpedance amplifier. The current noise $S_{I_{BE}}$ is the noise measured from the base node of the DUT in a common-emitter configuration. The value of κ should be chosen so $\kappa T^2 S_{I_{BE}}$ still dominates in the output from the transimpedance amplifier. From a practical point of view, a value of $\eta \geq 0.46$, i.e., $\kappa \geq 0.1$ is necessary in order not to loose too much conversion gain and thus sensitivity in the transimpedance amplifier.

The effective base series resistance termination (see Fig. 6.1 and 6.7) is calculated as:

$$R_S = R'_S + \frac{\eta}{1+\eta} R_{shunt} \tag{6.6}$$

where the internal resistance of the transimpedance amplifier is assumed to be small in comparison with R_{shunt}. The capacitance in the shunting circuit of Fig. 6.7 is important for two reasons: it enables correct measurement of the base current for biasing and it prevents latch-up of the transimpedance amplifier which otherwise may occur when the circuit resistance seen by the amplifier (R_{circ} in Fig. 6.6) is too low.

6.6 Importance of averaging

6.6.1 Impact on the PSD

As can be seen in the middle and bottom graphs of Fig. 5.1-5.4, a PSD calculated from a single measurement differs quite strongly from a PSD based on a larger set of measurements. Due to the random nature of noise, a PSD based on a single measured time sequence will never give the expected spectral behavior. It is important to point out that the averaging is made of several subsequent sampled time sequences of the same signal, i.e., not averaging of different signals as suggested in eq. 5.1. The averaging which is made assumes that the signal is stationary and that the spectrum from non-overlapping time sequencies can be averaged as being independent and thus being considered as measured in parallel [36]. The averaging process should not be confused with sampling a longer time sequence which only would give information about lower frequencies and consequently higher frequency resolution.

6.6.2 Choosing number of averages

The number of instantaneous time sequences that need to be averaged for finding the level of a PSD varies with application and the need of accuracy. The accuracy of the level of the PSD itself is however not necessarily the most important parameter when choosing the number of averages. If measurements are performed on more than one signal, the coherence between the two signals, as defined in eq. 5.2, may be of importance as it indicates existence of an identical signal in both signal leads. The magnitude of the coherence function will, by definition, be equal to unity for a single time sequence. Averaging the complex valued function will however give a decreasing function, i.e., the trend during an averaging is that it will decrease to a stable value. As discussed in [47] the minimum amount of averages necessary for a certain coherence level is:

$$\gamma_{floor} \approx \frac{1}{\sqrt{N_{avg}}} \tag{6.7}$$

which means that the correct detection of a low coherence level needs a very high amount of averages whereas full coherence can be detected using very few time sequences.

6.6.3 Choosing number of samples within a time sequence

Although the averaging will improve the appearance of the PSD spectrum, caution is necessary when interpreting data at the lowest frequencies. Since the FFT is performed on a finite set of sampled data which has been assumed to repeat infinitely in time, PSD values at the lowest frequencies will correspond to very few samples within the sampled data. Averaging does somewhat help, but the amount of samples in each time sequence should be chosen so that the lowest two or three frequency points (sometimes called lines) can be discarded.

6.7 Wide-band measurements

To be able to distinguish slopes etc. in a PSD, measurements over several decades of frequencies is often necessary. The measurements should then be performed over several frequency bands, e.g., a single decade of frequencies are measured at a time. The total PSD spectrum is then constructed from the PSDs of the different frequency bands as shown in Fig. 6.8.

When measuring over several sub-bands, it is possible to maintain a somewhat constant relative frequency resolution, i.e., the frequency resolution on a log-scale will remain fairly constant. If only one frequency band is chosen for the whole measurement, the majority of frequency points (90%) will be found in the top decade of the band. Thus also the loss when concatenating subsequent bands at higher frequencies is very small; only 10% of the frequency points are lost when keeping information only from the highest frequency decade of the band.

An additional benefit when dividing the measurement into sub-bands is that an efficient analog filtering of the signal is possible before feeding it into the signal analyzer. As the low-frequency noise level has a tendency to decrease with increasing frequency, the highest power density will be found in the lowest frequency region. If the frequency band that is measured is too wide, the dynamic range of the A/D-converter in the signal analyzer may limit the ability to detect the levels of the PSD at the higher frequencies, i.e., the signal part with the lowest intensity. By passing the measured signal through a band-pass filter, the dynamic range of the A/D-converter only needs to handle the different levels existing within the pass-band of the filter.

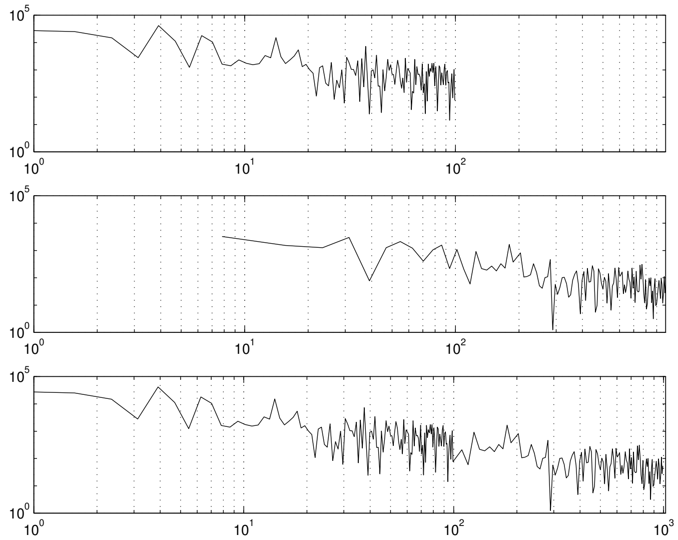

Figure 6.8: Example of how a wide-band spectrum is built by combining different sub-bands. Arbitrary units on the scales, no averaging. top: PSD of low-frequency band, middle: PSD of high-frequency band, bottom: concatenated PSD for whole band.

Chapter 7

Characterization

7.1 Background

This chapter will deal with different aspects of characterization of bipolar transistors using low-frequency noise measurements. Some parts are specifically related to the investigation of low-frequency noise in SiGe HBTs, whereas other parts are of more general nature.

7.2 Measurement of low-frequency base and collector current noise and coherence in SiGe heterojunction bipolar transistors using transimpedance amplifiers

A method of measuring noise of a SiGe HBT is presented where transimpedance amplifiers is used. Through the interpretation of data it has been established that the dominant noise source is located in the base-emitter junction of the device. Circuit parameters for the device under test has also been extracted and been found to compare well with values extracted using DC characterization. The complete text can be found in *Paper V*.

7.3 Temperature dependence and electrical properties of dominant low-frequency noise source in SiGe HBT.

A continued investigation on the dominant noise source of HBTs has been performed. The temperature dependence and electrical properties of the dominant low-frequency noise source in a SiGe HBT has been investigated. By employing a temperature variation of the device to get a variation of the base or collector current independently of each other, it is shown that the dominant noise source is strongly dependent on the collector current, but only weakly dependent on the base current. A modified Ebers-Moll model is presented that accounts for the collector current dependence of the dominant noise source and simultaneously accounts for the temperature dependence of the current amplification factor (β). Using the modified Ebers-Moll model, the physical positioning of the noise source is discussed. The complete text can be found in *Paper VI.*

7.4 Improved coherence measurements using voltage and transimpedance amplifiers in noise characterization of bipolar transistors

A method is presented to improve accuracy in noise characterization of bipolar transistors by using both a voltage amplifier and transimpedance amplifiers. When performing measurements using only voltage amplifiers, the range of base resistance termination is limited. When performing base current noise measurement measurements using voltage amplifiers, the accuracy drops drastically with low base resistance termination. The same problem is not existing when using a transimpedance amplifier. However, measurement accuracy of the whole setup is decreased at low base resistance terminations. Noise from the active input of the transimpedance amplifier is induced into the system and the accuracy of the measurements deteriorates. We show that by combining the use of both voltage and transimpedance amplifiers, the value of the base resistance termination can be decreased by almost an order of magnitude with remaining accuracy. The complete text can be found in *Paper VII.*

7.5 On the possibility to discriminate between noise sources in HBTs using a junction temperature variation

7.5.1 Introduction

Already performed work [44] has pinpointed the dominant noise source in a SiGe HBT to be in the base-emitter junction (S_{I_B} in Fig. 7.1). The source is thus not in the base lead or in the emitter lead, beyond the base-emitter junction. To find the physical origin of the dominant source is beyond the scope of this work and it is not clear whether it can be suppressed or not, i.e., whether SiGe HBT devices not having the dominant noise source in the base-emitter junction exists or not. In the case of a different device where the previously found source (called S_{I_B} in [44]) is not dominant, the already described method of discriminating the source can only exclude S_{I_B} and a more elaborate technique is necessary for a more precise location of the dominant noise source. With the common-emitter configuration, noise sources in the base lead and in the emitter lead, according to Fig. 7.1, are difficult to distinguish between. Using a different circuit setup could possibly make the discrimination easier. In a practical situation however, such configuration may be difficult to realize due to limitations in the pad configuration of the available devices. Extraction of parameters should also as long as possible be performed in the configuration where the device ultimately will be used in, e.g, in the common-emitter configuration.

7.5.2 Theory

The low-frequency noise sources in an HBT can schematically be presented as in Fig. 7.1.

The noise in the base and collector lead can thus be written as:

$$S_{I_{BE}} = \frac{1}{Z^2}\left[I_B^2 S_{r_b} + r_\pi^2 S_{I_B} + (I_B + I_C)^2 S_{r_e} + {r_e}^2 S_{I_C}\right] \tag{7.1}$$

$$S_{I_{CE}} = \frac{h_{fe}^2}{Z^2}\left[I_B^2 S_{r_b} + {Z_S'}^2 S_{I_B} + (I_B + I_C)^2 S_{r_e} + \frac{(R_S + r_b + r_\pi + r_e)^2}{h_{fe}^2} S_{I_C}\right] \tag{7.2}$$

The correlated spectrum between the two signals is expressed as:

$$\begin{aligned} S_{I_{BE}I_{CE}} = \frac{h_{fe}}{Z^2}&\left[I_B^2 S_{r_b} - r_\pi Z_S' S_{I_B} + (I_B + I_C)^2 S_{r_e}\right. \\ &\left. - \frac{(R_S + r_b + r_\pi + r_e) r_e}{h_{fe}} S_{I_C}\right] \end{aligned} \tag{7.3}$$

where

$$Z = (R_S + r_b + r_\pi + (1 + h_{fe}) r_e) \tag{7.4}$$

$$Z_S' = (R_S + r_b + r_e) = Z - r_\pi - h_{fe} r_e \tag{7.5}$$

$$I_C = \beta I_B \tag{7.6}$$

Since previous work [44] already has dealt with the discrimination of the source S_{I_B}, this part will concentrate on the first, third and fourth term within square brackets in eq. 7.1 ($I_B^2 S_{r_b}$, $(I_B + I_C)^2 S_{r_e}$ and $r_e^2 S_{I_C}$).

Due to the current dependence of the noise sources to be distinguished between, a procedure of controlling the base or collector current independently of the other one is desirable. By varying only one current, the variation in output noise from

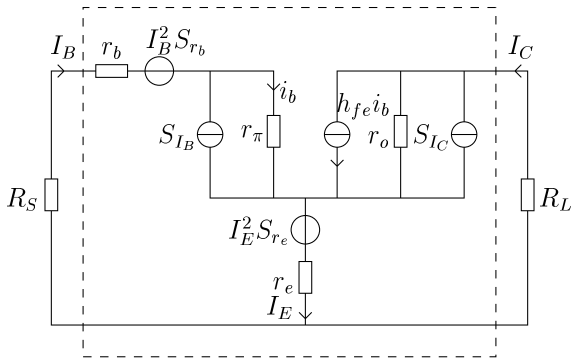

Figure 7.1: Small signal equivalent circuit of a typical BJT. The area within the dotted rectangle is the transistor. Currents with capital indices denote steady state currents

the base-emitter and collector-emitter leads will give indications on which source is the dominant one. From eq. 7.6 however it is seen that for a fixed β both currents will vary equally much and thus also the relation between current dependent noise sources will remain constant.

Through a big variation in current levels, a variation in β can be achieved and thus also the relation between I_B and I_C will vary. This is however not a very useful approach since both noise sources show a strong current dependence and the exponent of the current dependence need not remain constant. A different approach is necessary.

In a true HBT the electrical junction between the base and emitter exhibits a band-gap difference which ideally translates to a temperature dependence of β as:

$$\beta = K e^{\frac{L}{T}} \tag{7.7}$$

where K and L are constants depending on the material combination of the device. Second order effects on the temperature dependence exist (e.g. band-spikes in an AlGaAs/GaAs HBT), but of main importance is that the relation between base and collector current vary with temperature in a distinct way. This implies a possibility to vary the base and collector current independently of each-other.

Given the temperature dependence of β, it is thus possible to vary the relation between I_B and I_C while indeed keeping one of them constant. For a typical $Si_{1-x}Ge_x$ base device having $x \approx 0.2$, β can vary almost a factor of 2 for a temperature variation from 20° C to 80° C. In doing so, either I_B or I_C can be held constant while varying the other current.

From measurements of $S_{I_{BE}}$ and $S_{I_{CE}}$ it is then possible to distinguish which part of the sources (either S_{r_b}, S_{r_e} or S_{I_C}) is the main contributor, depending on the different current dependencies of $S_{I_{BE}}$ and $S_{I_{CE}}$.

A clear base current dependence on both $S_{I_{BE}}$ and $S_{I_{CE}}$ indicates that S_{r_b} is the dominant part, see eq. 7.1 and 7.2. In the term $(I_B + I_C)^2$, also found in both eq. 7.1 and 7.2, the collector current is dominant and thus S_{r_e} is only very weakly dependent on base current. A clear collector current dependence on both $S_{I_{BE}}$ and $S_{I_{CE}}$ may speak for either S_{r_e} or S_{I_C} being dominant. In order to distinguish between the two latter sources, the correlated spectrum between the two measured signals needs to be studied. From eq. 7.3 it is seen that there is a 180° phase difference between the signal of S_{r_e} and the signal of S_{I_C} in the measured $S_{I_{BE}I_{CE}}$. Thus, it should be possible to distinguish between these two sources by studying the phase of $S_{I_{BE}I_{CE}}$.

7.5.3 Conclusion

A theoretical technique for distinguishing which of the three sources S_{r_b}, S_{r_e} and S_{I_C} as seen in Fig. 7.1 is dominating in the the measured signals has been shown. Using the phase of the correlated signal, $S_{I_{BE}I_{CE}}$, found from the two measured signals, it is possible to distinguish between three different sources.

7.6 Simulation of noise in SPICE-like simulators using AC voltage and current sources only

A method for simulating noise sources in an arbitrary circuit where coherence and power spectral densities can be accurately calculated using regular voltage and current AC sources, is presented. This is useful when low-frequency noise measurement results are studied. By employing the simulation technique on a BJT model, the impact of different noise sources can be investigated and an understanding of the impact of external circuit parameters is simplified. The simulation method is based on a set of calculations where the different noise signals are made orthogonal by shifting the phase offset by different fractions of 2π between the calculations. The averaged resulting signals then correspond to the noise levels. Coherence between the different sources can also be calculated which is of great importance when studying results from two channel low-frequency noise measurements. The complete text can be found in *Paper VIII*.

Chapter 8

On the definition of the noise corner frequency in a BJT

8.1 Background

The definition of the noise corner frequency (f_c) which commonly is used[1] defines f_c as the interpolated frequency where the low-frequency noise PSD (having a negative frequency dependence) reaches the white-noise floor of the measured device. As f_c often is used as a figure of merit, it is important that it reflects – in an objective way – key features of a device. This is however not always the case as f_c:

- Does not give any information of absolute noise levels.
- Only indicates a single frequency where the excess noise reaches the noise floor of the device and does not give any information about noise at other frequencies.
- May be dependent on external circuitry or biasing conditions.
- Does not give any information on where the excess noise source is situated and may thus, for the same corner frequency, indicate quite different noise properties for two different devices.

In conclusion, f_c in its current definition can not be said to be an objective figure of merit for comparison between devices. To find an expression which gives sufficient information for comparing devices with different properties like different β etc., a more complex term is necessary. It is also important to more clearly define the circumstances under which the corner frequencies have been measured so different devices more easily can be compared and so that the measured corner frequency is relevant for the application in which the device will be used. In this chapter a common-emitter configuration of the devices has been assumed unless

[1] A strict definition for the low-frequency noise corner frequency of a BJT has not been found by the author.

otherwise stated. The common-emitter configuration is commonly used and serves as a good basis for developing an understanding of the finding of the corner frequency. Possibly – in order to make the corner frequency a more standardized property – the common-emitter should be made the default configuration for the corner frequency measurements; not necessarily because it is the best, but as it will work as a given configuration.

8.2 Definition of noise floor in a BJT

The noise floor, which shows as the flat level at frequencies high enough where the low-frequency noise diminishes, can be dominated by different sources depending on circuit setup and device properties. The sources for this type of noise are ideal in the sense that the levels of the PSDs should be defined by fundamental, and well understood, physical laws. The level of the PSDs will thus be predictable and will not change unless device parameters change. In the BJT, the noise in the base-emitter and base-collector junctions (see Fig. 7.1) are often the dominating sources. Resistances within the device also contribute to the noise. Of major interest for a common-emitter configuration is the noise floor in the collector lead since this lead often is where the output signal is measured. In the following text the different circuit elements in a simplified device model will be studied to find their contribution to the output noise level.

8.2.1 Contribution by base-emitter junction

The current PSD caused by the current flow through the base-emitter junction in a forward bias state is calculated as [36]:

$$S_{I_{B_0}} = 2qI_B \tag{8.1}$$

According to [36], this noise is not originating in so-called shot-noise, but is to be explained with other physical mechanisms. The derived equation is however the same as found in [39] which is verified experimentally. In Fig. 7.1 it is seen that the contribution to the collector will be:

$$S'_{I_{C_0}} = \left(\frac{R_S + r_b + r_e}{R_s + r_b + r_\pi + (1 + h_{fe})r_e}\right)^2 h_{fe}^2 S_{I_{B_0}} \tag{8.2}$$

As can be seen clearly, this output noise level is directly dependent on circuit parameters external to the device itself. In eq. 8.2 it has been assumed that $h_{fe} \approx \beta$ which is valid as long as the ideality factors of the base and collector currents are equal, i.e., the current curves in a Gummel plot are in parallel. A derivation of the expressions for the different terms will show that $h_{fe} = \beta \frac{n_B}{n_C}$ where n_B and n_C are the ideality factors (≥ 1) of the base and collector current respectively in a Gummel plot. For a well designed and fabricated BJT these ideality factors will not exceed 1.1 and thus the equivalence between h_{fe} and β is assured. As the equivalence is of importance in this work a short derivation follows. By definition:

$$\beta = \frac{I_C}{I_B} \tag{8.3}$$

and

$$\begin{aligned} h_{fe} &= \frac{\delta I_C}{\delta I_B} \\ &= \frac{\delta I_C}{\delta V_{BE}} \frac{\delta V_{BE}}{\delta I_B} \\ &= \frac{I_C}{n_C v_T} \frac{n_B v_T}{I_B} \\ &= \frac{I_C n_B}{I_B n_C} \\ &= \beta \frac{n_B}{n_C} \end{aligned} \tag{8.4}$$

which gives that

$$h_{fe} = \beta \frac{n_B}{n_C} \approx \beta \tag{8.5}$$

Thus the equivalence is established assuming that $\frac{n_B}{n_C}$ is close to unity.

8.2.2 Contribution by base-collector junction

In the reverse biased base-collector junction, carriers are swept through. This creates a true shot-noise which is calculated as (compare with eq. 8.1) [36]:

$$S''_{I_{C_0}} = 2qI_C \tag{8.6}$$

$$\approx 2qh_{fe}I_B \tag{8.7}$$

where it has been assumed that $h_{fe} \approx \beta$.

For the output noise at the collector, $S''_{I_{C_0}}$ is not dependent on external circuit parameters and can thus be considered an intrinsic noise level.

Since $S'_{I_{C_0}}$ is dependent on the circuit resistance R_S it is important to know at what value of this resistance that $S'_{I_{C_0}}$ dominates over $S''_{I_{C_0}}$. Neglecting r_b and $(1+h_{fe})r_e$ in comparison with R_S (regions of parameter values where this assumption is justified will be discussed) gives that $S'_{I_{C_0}}$ is dominant over $S''_{I_{C_0}}$ for values of R_S where:

$$R_S > \frac{v_T}{I_B(\sqrt{h_{fe}} - 1)} \tag{8.8}$$

Alternatively, the right hand side of eq. 8.8 can be written as $\frac{r_\pi}{\sqrt{h_{fe}}-1}$. A short derivation of eq. 8.8 is made by comparing eq. 8.2 and 8.7:

$$\frac{R_S^2}{(R_S + r_\pi)^2} h_{fe}^2 2qI_B > 2qh_{fe}I_B \tag{8.9}$$

$$
\begin{aligned}
& \Leftrightarrow \\
h_{fe}R_S^2 &> (R_S + r_\pi)^2 \\
& \Leftrightarrow \\
R_S^2(h_{fe}-1) &- 2R_S r_\pi - r_\pi^2 > 0 \\
& \Leftrightarrow \\
R_S^2 - 2R_S\frac{r_\pi}{h_{fe}-1} - \frac{r_\pi^2}{h_{fe}-1} &> 0
\end{aligned}
$$

By finding the values of R_S where eq. 8.9 becomes an equality and observing that eq. 8.9 is valid for high values of R_S, the minimal value of R_S can be found where eq. 8.9 holds:

$$
\begin{aligned}
R_S &> \frac{r_\pi}{h_{fe}-1} \pm \sqrt{\frac{r_\pi^2 + (h_{fe}-1)r_\pi^2}{(h_{fe}-1)^2}} \\
&> \frac{r_\pi \pm \sqrt{h_{fe}}r_\pi}{h_{fe}-1}
\end{aligned} \tag{8.10}
$$

It can be assumed that $h_{fe} \gg 1$ for a working transistor and that the value of R_S is non-negative, thus:

$$
\begin{aligned}
R_S &> \frac{r_\pi(\sqrt{h_{fe}}+1)}{h_{fe}-1} \\
&> \frac{r_\pi}{\sqrt{h_{fe}}-1} \\
& //r_\pi = \frac{v_T}{I_B}// \\
&> \frac{v_T}{I_B(\sqrt{h_{fe}}-1)}
\end{aligned} \tag{8.11}
$$

In Table 8.1, the base series resistance termination, R_S where $S'_{I_{C0}}$ and $S''_{I_{C0}}$ are equal is calculated for different values of h_{fe} and I_B. It is seen that for base currents of $I_B = 1mA$, the break-even point for R_S is found to be very small. This is a simplification and indeed r_b and r_e cannot immediately be considered negligible. The first-order conclusion is thus that $S''_{I_{C_0}}$ will not become dominant over $S'_{I_{C_0}}$ at the output for these base currents as r_b and r_e are in series with R_S. However, base currents of $1mA$ indicate a very big device and both r_b and r_e may thus very well be very small, possibly still making eq. 8.8 retaining its validity.

8.2.3 Contribution by series resistances

The two last parameters that may induce noise (as seen in Fig. 7.1) are r_b and r_e. Their induced voltage noise is caused by thermal motion of the carriers and can generally be expressed (for low frequencies) as [36]:

Table 8.1: Lowest values of R_S where S'_{C_0} is dominant in comparison with S''_{C_0} in the collector output noise floor. The parameterization on I_B rather than on r_π is due to the comparison of two current dependent entities.

h_{fe}	I_B	R_S
10	100nA	120kΩ
	10μA	1.2kΩ
	1mA	12Ω
50	100nA	43kΩ
	10μA	430Ω
	1mA	4.3Ω
100	100nA	29kΩ
	10μA	290Ω
	1mA	2.9Ω
200	100nA	20kΩ
	10μA	200Ω
	1mA	2.0Ω

$$S_{V_R} = 4k_BTR \tag{8.12}$$

and their contribution in total to the collector output noise is (converted to current noise):

$$S'''_{I_{C_0}} = \frac{h_{fe}^2}{(R_s + r_b + r_\pi + (1 + h_{fe})r_e)^2} 4k_BT(R_S + r_b + r_e) \tag{8.13}$$

where R_S has to be included as it is a physical resistor and thus contributes noise. From a comparison between eq. 8.2 and eq. 8.13 it can be seen that the value of $(R_S + r_b + r_e)$, where the Nyquist noise of the resistors dominate over the noise of the base-emitter junction in the output noise, can be calculated as:

$$(R_S + r_b + r_e) < \frac{4k_BT}{2qI_B} \tag{8.14}$$

which can be simplified to:

$$(R_S + r_b + r_e) < 2r_\pi \tag{8.15}$$

by observing that

$$r_\pi = \frac{k_BT/q}{I_B} \tag{8.16}$$

The result in eq. 8.15 is quite interesting since it shows that the noise floor in the collector current of a measured BJT quite easily can be dominated by a resistor noise rather than the, commonly expected, noise of the base-emitter junction.

The relation between $S''_{I_{C0}}$ and $S'''_{I_{C0}}$ is a bit more complicated. Comparing eq. 8.6, 8.7 and 8.13 gives that the Nyquist noise of the resistors dominate over the shot noise of the collector-base junction in the output noise when:

$$\frac{(R_S + r_b + r_e)}{(R_s + r_b + r_\pi + (1 + h_{fe})r_e)^2} > \frac{1}{2h_{fe}r_\pi} \tag{8.17}$$

The relation in eq. 8.17 is only interesting to investigate for values of $R_S < \frac{r_\pi}{\sqrt{h_{fe}-1}}$ since for higher values of R_S, $S'_{I_{C0}}$ becomes dominant over $S''_{I_{C0}}$ in the collector current noise. Thus, for $R_S \ll r_\pi$ and $(1 + h_{fe})r_e \ll r_\pi$, eq. 8.17 simplifies to:

$$(R_S + r_b + r_e) > \frac{r_\pi}{2h_{fe}} \tag{8.18}$$

In conclusion, there are three regimes possible. For $\frac{r_\pi}{2h_{fe}} < (R_S + r_b + r_e) < 2r_\pi$, the Nyquist noise of the resistors are dominant. For lower values of $(R_S + r_b + r_e)$, the shot noise of the base-collector junction is dominant and for higher values of $(R_S + r_b + r_e)$, the noise of the base-emitter junction is dominant in the collector current. It has been assumed that the device has a moderate current gain (so $(1 + h_{fe})r_e \ll r_\pi$ is valid).

In conclusion it is important to point out that the noise floor of the collector current in a common-emitter configuration is not solely defined by the noise in the base-emitter junction and that the level of the noise floor indeed is varying.

8.3 Comments on finding the corner frequency

It has been shown that the fundamental noise floor of a BJT in a common-emitter configuration is affected by several different parameter. Thus also the corner frequency will be depending on how the noise measurement has been performed. This is especially important when values of the corner frequency are extrapolated from measurements where the actual noise floor is not found. It is also important to verify that the noise floor which may be measured indeed is the fundamental one and not caused by excess noise of some kind.

The true noise floor should be defined as the theoretical floor given by well understood physical processes, e.g., the ones described in 8.2.1-8.2.3. The corner frequency may thus reflect the level of the excess noise only. If the measured noise floor were to be used, the intersection of two different, unknown, noise signals could give a considerably lower corner frequency caused by a too high measured noise floor. The origin of this noise can be caused by, e.g., the measurement equipment itself.

From the calculation of the noise floor level caused by the different fundamental noise sources it is also shown that with different positioning of the sources inside the device, the noise will be transferred to the collector lead in different ways. The same effect is occurring for the excess noise due to how they are positioned within the BJT. Thus, a comparison between different devices should preferably be made between devices having dominant sources in the same position within the device.

8.4 Conclusion

The definition of a corner frequency for a bipolar transistor is very difficult as this frequency is dependent of many parameters inside and outside the device. As a figure of merit when comparing different transistors with drastically different properties, the corner frequency is questionable. When comparing devices that are closely related to each-other, e.g., comparing different devices in the evolution of a fabrication process, the corner frequency may work as a very good indicator of quality difference between the different devices. The measurements should then be performed under similar conditions, e.g., collector current density can be maintained constant and base-resistance termination is chosen as function of r_π as described.

Chapter 9

Suggestions for future work

As the work presented in this thesis follows the two major paths of modeling and aspects of low-frequency noise, also the suggestions for continued work can be divided into two directions.

The modeling of the SiGe HBT can be improved in several ways depending on what application one has in mind.

For the completeness of the model, the impact of several physical parameters like alloy grading of the base, dopant grading of the collector and emitter etc., should be further studied. Also different physical effects like base push-out and extreme forward biasing of the base-emitter junction need to be investigated. Each parameter or physical process which will be included in the model will require a thorough investigation and it is thus important to initially try to estimate the importance and benefit of such work.

As a large-signal model with an emphasis on accounting for the physical processes within the transistor, the complexity of the model when simulating more complex structures may need to be decreased. It is then important to investigate what parameters have key importance for a certain work.

From the work on the low-frequency noise sources of the SiGe HBT, the model should be added with ability to handle noise at different locations within the device. As a large-signal model it is also interesting to investigate modeling of the up-conversion of low-frequency noise into, e.g., phase-noise of an oscillator.

Using the method of simulating low-frequency noise in a SPICE like simulator using only AC voltage and current sources, a model of the noise sources within a BJT should be realized and studied. Calculations of the input and output current noise and coherence between the signals should be calculated for a set of different signal levels of the individual noise sources. The BJT need not be in a common-emitter configuration. Also different circuit configurations and a variation of parameters for external circuit elements, e.g., the base resistance termination in a common-emitter configuration should be studied. By creating such a dataset, an increased understanding of the effects of the different noise sources and circuit configurations can be achieved which should simplify the study of new devices.

In the work on extracting the noise sources within the SiGe HBT it has been found that only one noise source is dominating in the device; regardless of device manufacturer. The noise source seems thus to be related to the Si/SiGe interface rather than related to a specific fabrication process. The origin of this source has not been completely investigated and a continued work should emphasize on finding the physical origin and position of the source. With such information it can be established whether the noise source can be removed or at least its impact lowered through fabricational improvements. A suggestion for the study is to use different alloying combinations of the SiGe base and investigate its impact on the noise level.

For continued research of specific noise sources, a higher automation of the measurement procedure is mandatory. Due to the time consuming parameter-sweep measurements, a sufficient set of measured devices for proper statistical studies of the noise is currently impossible. By being able to control all circuit parameters (i.e., biasing conditions, device temperature and circuit terminations) through a computer program, devices can be measured on a daily basis without continuous supervision which otherwise is necessary.

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Appendix A

Nomenclature for the large-signal model

BJT	Bipolar Junction Transistor
DHBT	Double Heterojunction Bipolar Transistor
FEM	Finite Element Method
HBT	Heterojunction Bipolar Transistor
MDS	Microwave Design System
SCR	Space Charge Region
SDD	Symbolically Defined Device
SEM	Scanning Electron Microscopy
SHBT	Single Heterojunction Bipolar Transistor
SIMS	Secondary Ion Mass Spectroscopy

Variables:

_In	node variables related to the SDD
_Vn	node variables related to the SDD
A_{B}	base contact area [cm^2]
A_{C}	total area of base-collector junction [cm^2]
A_{E}	area of base-emitter junction [cm^2]
A_{Econt}	area of emitter contact [cm^2]
α_{F}	forward base transport factor
α_{R}	reverse base transport factor
β	DC current gain
β_{HBT}	DC current gain for HBT
C_{j0}	junction capacitance at zero bias [F]
C_{BC}	capacitance in intrinsic base-collector junction [F]
C_{BCext}	junction capacitance in extrinsic base-collector junction [F]
C_{BCext00}	junction capacitance in extrinsic base-collector junction at zero bias and ambient temperature [F]
C_{BCpad}	capacitance between base and collector pad [F]

$C_{BCtottotal}$	base-collector capacitance [F]
C_{BE}	capacitance in intrinsic base-emitter junction [F]
C_{BEpad}	capacitance between base and emitter pad [F]
C_{Bshunt}	capacitance shunting the base contact resistance [F]
C_{CEpad}	capacitance between collector and emitter pad [F]
$C_{DCblock}$	capacitance for blocking of DC [F]
C_j	junction capacitance [F]
$C_{RFshunt}$	capacitance for shunting RF-signals [F]
C_B	electron affinity in base [V]
C_C	electron affinity in collector [V]
C_E	electron affinity in emitter [V]
D_{eB}	diffusion constant for electrons in base [cm^2s^{-1}]
D_{hC}	diffusion constant for holes in collector [cm^2s^{-1}]
D_{hE}	diffusion constant for holes in emitter [cm^2s^{-1}]
ΔV_B	potential difference between Fermi level and valence band in base [V]
ΔV_C	potential difference between Fermi level and conduction band in collector [V]
ΔV_E	potential difference between Fermi level and conduction band in emitter [V]
ε	dielectric constant [As/Vcm]
ε_0	dielectric constant in free space $8.854 * 10^{-14}$ [As/Vcm]
ε_B	dielectric constant in base [As/Vcm]
ε_C	dielectric constant in collector [As/Vcm]
ε_E	dielectric constant in emitter [As/Vcm]
E_1	constant for calculating doping induced band-gap contraction [eV]
E_{Cbreak}	electric breakdown field in collector [V/cm]
ΔE_g	difference in band-gap between two different materials [eV]
ΔE_{gX}	band-gap contraction due to doping [eV]
E_g	band-gap energy difference [eV]
E_{gB}	band-gap in base [eV]
E_{gB0}	band-gap in base at fixed temperature [eV]
E_{gC}	band-gap in collector [eV]
E_{gC0}	band-gap in collector at fixed temperature [eV]
E_{gE}	band-gap in emitter [eV]
E_{gE0}	band-gap in emitter at fixed temperature [eV]
f_t	frequency where current gain reaches unity [Hz]
f_{max}	maximum frequency of oscillation [Hz]
Φ_B	potential difference from Fermi level to vacuum level in base [V]
Φ_C	potential difference from Fermi level to vacuum level in collector [V]
Φ_E	potential difference from Fermi level to vacuum level in emitter [V]
γ	constant for calculating doping and temperature dependent electron mobility in Silicon
g_{BC}	DC transconductance

η	B constant for calculating base diffusion delay
i_{B}	total base current [A]
I_{B}	DC base current [A]
i_{BCext}	diode current in extrinsic base-collector junction [A]
$I_{BCext00}$	saturation current for current in external base-collector junction diode [A]
$i_{BCextleak}$	leakage current occurring between base and collector [A]
$I_{BCextleak}$	Saturation current for external leakage current between base and collector [A]
i_{C}	total collector current [A]
I_{C}	DC collector current [A]
i_{Ce}	electron injection current into base from collector [A]
I_{Ce0}	electron saturation current in base-collector diode [A]
i_{Ch}	hole injection current into collector from base [A]
I_{Ch0}	hole saturation current in base-collector diode [A]
I_{E}	DC emitter current [A]
i_{Ee}	electron injection current into base from emitter [A]
I_{Ee0}	electron saturation current in base-emitter diode [A]
i_{Eh}	hole injection current into emitter from base [A]
I_{Eh0}	hole saturation current in base-emitter diode [A]
I_{LBC}	leakage currents occurring in the intrinsic base-collector junction [A]
I_{LBE}	leakage currents occurring in the intrinsic base-emitter junction [A]
I_{m}	current components for the non-ideal current in the intrinsic transistor [A]
φ	factor introduced in the frequency domain to account for delays [rad]
j	imaginary constant
J_{0e}	electron saturation current density [A/cm^2]
J_{Em}	emitter leakage saturation current density[A/cm^2]
K_{IEe}	constant to account for a reduction of electron injection current into the base from the emitter
K_{IEh}	constant to account for a reduction of hole injection current into the emitter from the base
K_{ICe}	constant to account for a reduction of electron injection current into the base from the collector
K_{ICh}	constant to account for a reduction of hole injection current into the collector from the base
k_{B}	Boltzmanns constant $= 1.381 * 10^{-23}$ [Js/K]
L_{B}	effective length between base contact metallization and intrinsic base [cm]
L_{Bpad}	inductance in base pad [H]
L_{Cpad}	inductance in collector pad [H]
L_{Epad}	inductance in emitter pad [H]
$L_{DCshunt}$	inductance for shunting of DC [H]
L_{F}	emitter length in the direction of the base current flow [cm]

M_C	multiplication factor for collector avalanche breakdown
μ_{eC}	electron mobility in collector [$cm^2V^{-1}s^{-1}$]
μ_{eC0}	electron mobility in collector at fixed ambient temperature [$cm^2V^{-1}s^{-1}$]
μ_{eE}	electron mobility in emitter [$cm^2V^{-1}s^{-1}$]
μ_{hB}	hole mobility in base [$cm^2V^{-1}s^{-1}$]
$\mu_{hBtrans}$	transverse (parallel to the surface) hole mobility in strained base [$cm^2V^{-1}s^{-1}$]
μ_{n0}	constant for calculating doping and temperature dependent electron mobility in Silicon [$cm^2V^{-1}s^{-1}$]
μ_{n1}	constant for calculating doping and temperature dependent electron mobility in Silicon [$cm^2V^{-1}s^{-1}$]
$m_{hhSiGestrain}$	mass of heavy holes in strained SiGe [kg]
$m_{lhSiGestrain}$	mass of light holes in strained SiGe [kg]
N_0	constant for calculation of doping induced band-gap contraction [cm^{-3}]
N_B	doping concentration in base [cm^{-3}]
N_C	doping concentration in collector [cm^{-3}]
N_E	doping concentration in emitter [cm^{-3}]
$n_{BCextleak}$	ideality constant for the leakage current occurring between base and collector
N_{cond}	density of states in the conduction band [cm^{-3}]
$N_{cSiGeLStrain}$	density of states in the L-valley of the conduction band of strained SiGe [cm^{-3}]
$N_{cSiGeStrain}$	total density of states in the conduction band of strained SiGe [cm^{-3}]
$N_{cSiGeXStrain}$	density of states in the X-valley of the conduction band of strained SiGe [cm^{-3}]
n_F	ideality constant for the diodes in the base-emitter junction modeling electron and hole injection
n_R	ideality constant for the diodes in the base-collector junction modeling electron and hole injection
n_i	intrinsic carrier concentration [cm^{-3}]
n_{iB}	intrinsic carrier concentration in base [cm^{-3}]
n_{iC}	intrinsic carrier concentration in collector [cm^{-3}]
n_{iE}	intrinsic carrier concentration in emitter [cm^{-3}]
n_m	ideality constant for the different current components of the non-ideal current in the intrinsic transistor
N_{ref}	constant for calculating doping and temperature dependent electron mobility in Silicon [cm^{-3}]
N_{val}	density of states in the valence band [cm^{-3}]
$N_{vSiGehhStrain}$	density of states for heavy holes in the valence band of strained SiGe [cm^{-3}]
$N_{vSiGelhStrain}$	density of states for light holes in the valence band of strained SiGe [cm^{-3}]
$N_{vSiGeStrain}$	total density of states in the valence band of strained SiGe [cm^{-3}]
π	constant $\approx 3.141...$

P	internally dissipated power [W]
Q	charge [As]
q	unity charge = $1.602 * 10^{-18}$ [As]
QE_g	temperature dependent multiplication factor for energy band-gap
Q_f	charge build-up in non-reverse biased junction capacitance [As]
Q_G	total base charge [As]
Q_r	charge build-up in reverse biased junction capacitance [As]
ρ_B	base contact resistivity [Ωcm^2]
R_B	total base-lead resistance [Ω]
R_{BCext}	series resistance in extrinsic base-collector junction [Ω]
R_{Bcont}	base contact resistance [Ω]
R_{BCpad}	resistance between base and collector pad [Ω]
R_{BEloss}	resistance for modeling shunting loss between base and emitter in the extrinsic part of the transistor [Ω]
R_{BEpad}	resistance between base and emitter pad [Ω]
R_{Blead}	resistance of base sheet leading in to intrinsic transistor [Ω]
R_{Bpad}	resistance in base pad [Ω]
R_{Bprobe}	resistance in probe connecting to the base pad [Ω]
R_C	collector contact and sub-collector resistance [Ω]
R_{CEloss}	resistance for modeling shunting loss between collector and emitter in the extrinsic part of the transistor [Ω]
R_{CEpad}	resistance between collector and emitter pad [Ω]
R_{Closs}	resistance for modeling loss in the collector lead of the extrinsic part of the transistor [Ω]
R_{Cpad}	resistance in collector pad [Ω]
R_{Cprobe}	resistance in probe connecting to the collector pad [Ω]
$R_{Cundepl}$	resistance of undepleted part of collector [Ω]
r_E	emitter contact resistivity [Ωcm^2]
R_{Econt}	emitter contact resistance [Ω]
R_{Eloss}	resistance for modeling loss in the emitter-lead of the extrinsic part of the transistor [Ω]
R_{Epad}	resistance in emitter pad [Ω]
R_{Eprobe}	resistance in probe connecting to the emitter pad [Ω]
$R_{Eundepl}$	resistance of undepleted part of emitter [Ω]
S_{11}	scattering parameter
S_{12}	scattering parameter
S_{21}	scattering parameter
S_{22}	scattering parameter
T	junction temperature [K]
t	total delay [s]
T_0	ambient temperature [K]
τ_B	base diffusion delay [s]
τ_C	collector transit time delay [s]
τ_F	adjustment parameter for delay [s]
v	applied voltage [V]

v_{BC}	total base-collector voltage [V]
v_{BE}	total base-emitter voltage [V]
v_{CE}	total collector-emitter voltage [V]
V_{BC}	DC-part of base-collector voltage [V]
V_{BE}	DC part of base-emitter voltage [V]
V_{Cbreak}	collector breakdown voltage [V]
V_j	built-in voltage [V]
V_{jC0}	built-in voltage in base-collector junction [V]
V_{jC00}	built-in voltage in base-collector junction at fixed ambient temperature [V]
V_{jE0}	built-in voltage in base-emitter junction [V]
V_{Offset_m}	offset voltages used to simplify extraction of non-ideal current components in the intrinsic transistor [V]
v_S	electron saturation velocity in silicon [cm/s]
V_T	thermal voltage [V]
V_{T0}	thermal voltage at ambient temperature [V]
V_{thermm}	model parameters for thermal dependence of non-ideal current components in the intrinsic transistor [V]
ω	angular frequency [rad/s]
W_B	total base width [cm]
W_{Beff}	effective base width [cm]
W_C	total collector width [cm]
W_E	total emitter width [cm]
W_F	width of emitter in direction perpendicular to the base current [cm]
x_{GE}	fraction of Germanium content in the base
X_j	depletion width [cm]
X_{j0}	depletion width at zero bias [cm]
X_{jBC}	depletion width in base on collector side [cm]
X_{jC}	depletion width in collector SCR [cm]
X_{jC00}	depletion width in collector SCR at zero bias and ambient temperature [cm]
X_{jE}	depletion width in emitter SCR [cm]

Appendix B

Implementation of device model in MDS

This appendix shows an implementation of the large-signal model in MDS from Hewlett Packard. The different figures (B.1-B.6) correspond to different pages within a *circuit element* of MDS. The *circuit element* can be inserted as a unique circuit with input and output terminals (called `Tin`, `ref`, `Pout`, `Base`, `Collector` and `Emitter` in Fig. B.1) into a design. Different kinds of simulations can be made and different parameters of the model can be varied by either editing the equations or allowing the simulator to vary parameters according to an optimization scheme.

The implementation of the model into the simulation package has been an ongoing process during a long time. Thus, parameter names have varied and there is a difference between some variable names in the implementation and the variable names used in the definition of the model. The variable names in the implementation have been retained in order to maintain a more bug free version than would be the case if all variable names were to be rewritten with names used in the definition of the model. Using the presented implementation, all simulations included in this work have been performed.

In the first page (see Fig. B.1) the embedding shell is implemented. Most circuit elements are self explanatory. The elements called `CPWTL` model coplanar transmission lines and the element `CPWSUBSTRATE` defines the physical parameters for the substrate and conductors composing the transmission lines.

The three connectors used for thermal feedback (called `Tin`, `ref` and `Pout`, slightly above the center of Fig. B.1) are inserted for connection with the intrinsic part. Nodes with identical names as the connector names connect to the SDD, see Fig. B.3.

The extrinsic part of the transistor is implemented in Fig. B.2. The two diodes are defined using different parameter sets, thus two different model forms (called `DIODEMODELFORM` in Fig. B.2). All parameters for the extrinsic part are evaluated at the beginning of the simulation.

The intrinsic part of the transistor is implemented through the SDD which has already been discussed. The major part of the equations for calculating the port currents are found in Fig. B.4. The physical parameters defining the device are found in Fig. B.5. Some equations concerning the physical properties of the device (e.g., band-gap contraction of the different layers of the device) are also included. In Fig. B.6 are the completing equations and constants.

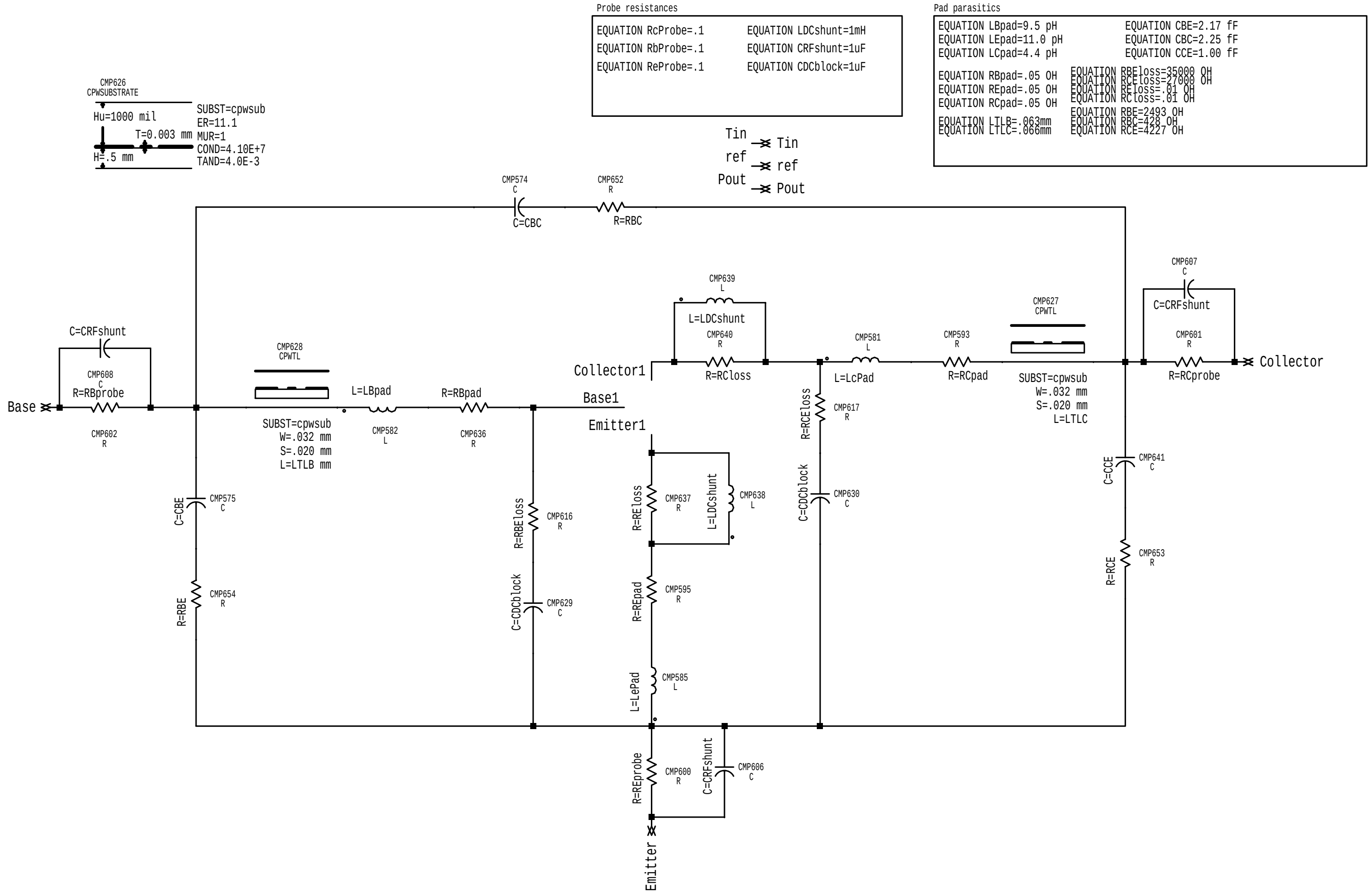
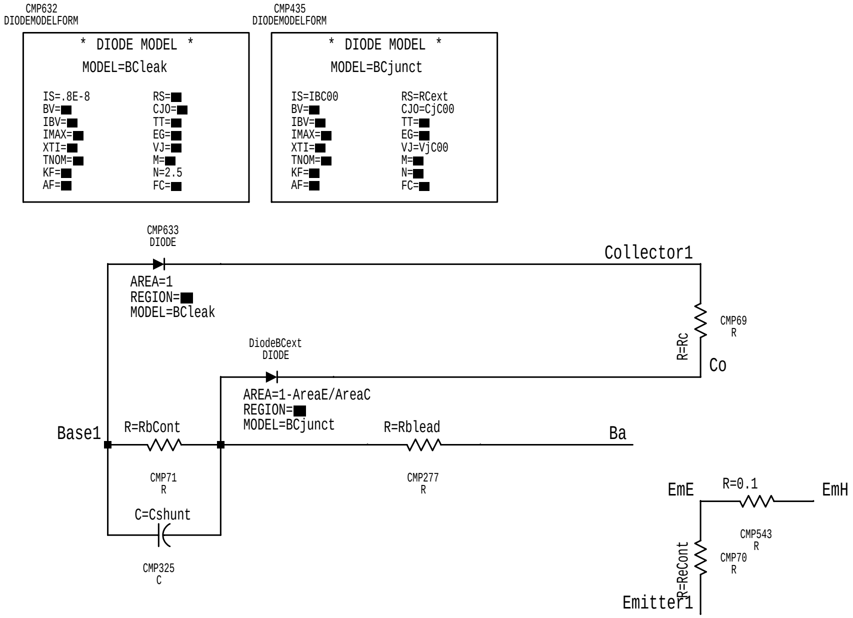


Figure B.1: The embedding shell.



Non-linear part

```
EQUATION IBC00=ICe00+ICh00
EQUATION ICe00=q*(areaC-AreaECont)*DBase*niB^2/(WB*NB)
EQUATION ICh00=q*(areaC-AreaECont)*DC*niC^2/((WC-XjC00)*NC)
EQUATION VjC00=XIB-XIC-dVC+EgB0   EQUATION VBC00=-1
EQUATION CjC00=epsC*areaC/XjC00
EQUATION XjC00=sqrt(2*NB*epsC*epsB*VjC00/(q*NC*(epsB*NB+epsC*NC)))
EQUATION RCext=(WC-XjC00*sqrt(abs(1-VBC00/VjC00)))/(q*unC0*NC*AreaC)
```

Contact resistances

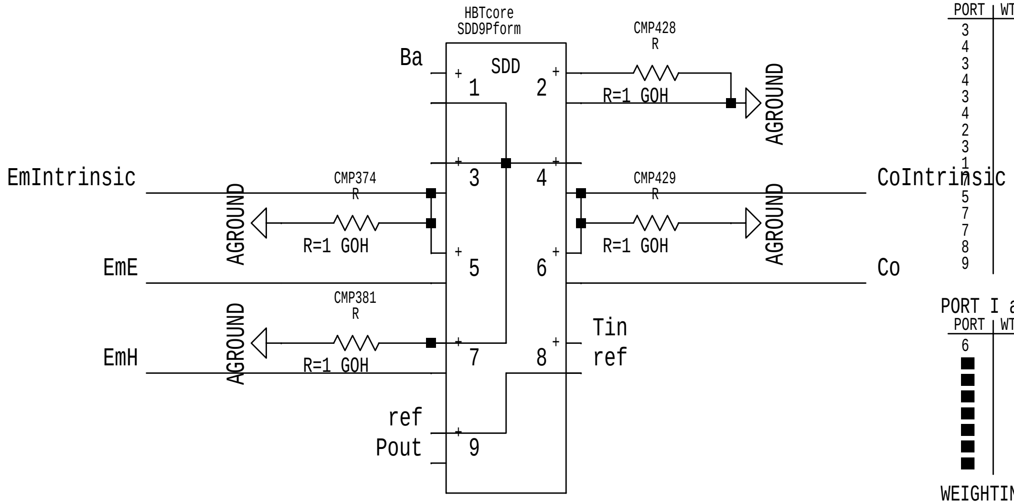
```
EQUATION RbCont=RhoBa/(AreaC-AreaECont)
EQUATION RhoBa=5E-7<5.00E-6<5E-5
EQUATION Cshunt=sqrt((q*epsB*NB)/(2*VjBM))*(AreaC-AreaECont)
EQUATION ReCont=RhoEm/AreaECont
EQUATION RhoEm=5E-7<5.31E-07<5E-5
EQUATION VjBM=1  Intrins. voltage Base-Metal
```

Lead resistances

```
EQUATION Rblead=LB/(Wfinger*WB*uhBtrans*q*NB)
EQUATION Wfinger=20E-4
EQUATION LB=2E-4
EQUATION uhBtrans=250

EQUATION Rc=5 oh
```

Figure B.2: The extrinsic part of the transistor.



PORT CURRENTS

PORT	WT.FCN.	EXPRESSION = I
3	0	IFor+IEhole
4	0	IRev*M+IChole-AreaE*JCGR+ICleak
3	1	Qbe+Qbediff
4	1	Qbc
3	3	-IRev*alphaR
4	2	-IFor*alpha0F*M
2	0	0
3	0	0
1	0	Ib
4	0	0
5	0	Ie
7	0	0
7	0	1*(Ieleak+Iehigh1+ILeakE0)
8	0	_v8/1E6
9	0	P

PORT I and V

PORT	WT.FCN.	EXPRESSION = 0
6	0	_V6+Ic*RCundepl

WEIGHTING FUNCTIONS:

WT.FCN.	EXPRESSION
2	delayF
3	1

Constants:

EQUATION Mje=0.5
EQUATION Mjc=0.5
EQUATION nF=1.000<1.036<1.040
EQUATION nR=1.0
EQUATION Vbemax=.87+1
EQUATION Vbemin=-1E10
EQUATION Vbcmax=.90+1
EQUATION Vbcmin=-1E10
EQUATION Tmax=523

Thermal:

EQUATION Ttemp=if (_v8<273) then 273 else _v8 endif
EQUATION T=if (Ttemp>Tmax) then Tmax else Ttemp endif
EQUATION P=mag(Vce*Ic)+mag(Vbe*Ib)+mag(Ic*Ic*ReCont)

EQUATION VT=kB*T/q

Miscellaneous:

EQUATION w=omega
EQUATION Tau=TauF+TauC+0.22*TauB
EQUATION Vce=Vbe-Vbc

.22 from Laser, "Reconciliation...,"Trans. Elec. Dev. 1991 pp1685-1692

Figure B.3: The intrinsic part of the transistor. The SDD implementing circuits as nonlinear functions. For the equations, see Fig. B.4, B.5 and B.6.

```
EQUATION expon(_val)=if (_val>k) then exp(k)*(_val-k+1) else exp(_val) endif
EQUATION k=69
EQUATION limit(_in,_max)=_max*(1-.02*ln(exp(50*(1-_in/_max))+1))
```

Collector junction

```
Junction voltage:
EQUATION VbcTemp=If (_v4>Vbcmax) then Vbcmax else _v4 endif
EQUATION Vbc=If (VbcTemp<Vbcmin) then Vbcmin else VbcTemp endif

Ideal diode currents:
EQUATION IRev=ICe*(expon((Vbc)/(VT*nR))-1)
EQUATION IChole=ICh*(expon((Vbc)/(VT*nR))-1)

EQUATION JCGR=2.16E-01 */ 1000
EQUATION IC10=.8E-18 */ 1000
EQUATION nC1=1<2.50<10
EQUATION ICleak=IC10*(expon(Vbc/(VT*nC1))-1)

Junction capacitance, different
models:
EQUATION Qbctemp=if (Vbc>(aBCcap*VjC0)) then Qbcf else Qbcr(Vbc) endif
EQUATION Qbc=Qbctemp*AreaE/AreaC
EQUATION Qbcdiff=0*tauB*IFor
EQUATION Qbcr(_v)=-VjC0*CjC0*((1-(_v)/VjC0)^(1-Mjc))/(1-Mjc)
EQUATION Qbcf=CjC0*(Vbc-aBCcap*VjC0+(Vbc-aBCcap*VjC0)^2/(4*VjC0*(1-aBCcap)))/sqrt(1-aBCcap)+Qbcr(aBCcap*VjC0)
EQUATION aBCcap=.5

Junction delay and breakdown
multiplier:
See Teeter Thesis, p.115
EQUATION delayF = if (w<1) then 1 else sin(w*(tauC))*exp(-j*w*(tau))/(w*(tauC)) endif
EQUATION M=if Vbc<0 then 1/(1-(abs(Vbc/Vbreak))^4) else 1 endif
```

Emitter junction

```
Junction voltage:
EQUATION Vbetemp=If (_v3>Vbemax) then Vbemax else _v3 endif
EQUATION Vbe=If (VbeTemp<Vbemin) then Vbemin else VbeTemp endif

Ideal diode currents:
EQUATION IFor=correctIFor*IEe*(expon((Vbe)/(VT*nF))-1)
EQUATION IEhole=correctIEhole*IEh*(expon((Vbe)/(VT*nF))-1)

EQUATION correctIFor=0.2   EQUATION correctIEhole=.5
Too high calculated bandgap narrowing
overestimates the saturation current.
Decr. by 1/2 - 1/3 suggested by F. Beisswanger

Junction capacitance, different
models:
EQUATION Qbe=if (Vbe>(aBEcap*Vje0)) then Qbef else Qber(Vbe) endif
EQUATION Qbediff=tauB*IFor
EQUATION Qber(_v)=-Vje0*Cje0*((1-(_v)/Vje0)^(1-Mje))/(1-Mje)
Cap model from paper on SDD (p.17)
EQUATION Qbef=CjE0*(Vbe-aBEcap*VjE0+(Vbe-aBEcap*VjE0)^2/(4*VjE0*(1-aBEcap)))/sqrt(1-aBEcap)+Qber(aBEcap*VjE0)
EQUATION aBEcap=.5
EQUATION Qbef1=Vbe*CjE0

Leakage currents, empirical for
base:
EQUATION Ielowtemp=JE10*AreaE*expon((Vbe-voffs1)/(VT*n1)-(VT1/VT-VT1/VT0))
EQUATION Ielow=if (mag(Ielowtemp)>1) then 1 else Ielowtemp endif

EQUATION Iehightemp=JE20*AreaE*expon((Vleak-voffs2)/(VT*n2))
EQUATION Iehigh=if (Iehightemp>1) then 1 else Iehightemp endif
EQUATION Ieleak=if (mag(Iehigh+Ielow)<1E-10) then 1E-10 else (Iehigh*Ielow)/(Iehigh+Ielow)+Iehigh1 endif

EQUATION Vleak=_v7
EQUATION voffs1=0.55
EQUATION voffs2=0.65
EQUATION VT1=.1<0.2<.2
EQUATION JE10=2.914 */ 1000
EQUATION JE20=5.E+08 */ 10
EQUATION n1=1<1.8449<10
EQUATION n2=5<20.000<200

EQUATION Iehightemp1=JE30*AreaE*expon((Vleak-voffs3)/(VT*n3)-(VT3/VT-VT3/VT0))
EQUATION Iehigh1=if (Iehightemp1>1) then 1 else Iehightemp1 endif
EQUATION voffs3=.85    EQUATION VT3=.10
EQUATION JE30=1E-16 */ 100
EQUATION n3=1<1.000<2
EQUATION IleakE0=JeGR*AreaE  EQUATION JeGR=1E-6 */ 100

EQUATION ME=if Vbe<-0.9999*VbreakE then abs(1/IRev) else MEtmp endif
EQUATION MEtmp=if Vbe<0 then 1/(1-(abs(Vbe/VbreakE))^4) else 1 endif
```

Terminal currents:

```
EQUATION Ic=-_i6
EQUATION Ib=_v1/.1
EQUATION Ie=_v5/REundepl

RCundepl must use fixed values since it is used
for finding Ic and thus power dissipation.
Alternative way of solving this is to use a
separate node for finding Ic.

EQUATION RCtemp=(WC-XjC)/(q*unC*NC*AreaE)
EQUATION RCundepl=If (RCtemp<.1) then .1 else RCtemp endif
EQUATION REtemp=(WE-XjE)/(q*unE*NE*AreaE)
EQUATION REundepl=If (REtemp<.1) then .1 else REtemp endif
```

Figure B.4: Equations defining the intrinsic shell.

Device data:

Emitter

```
EQUATION WE=0.070E-4
EQUATION NE=1.00E18<2.00E+18<4.00E18
EQUATION EgE=QEg(T)*(1.12-deltaEgE)

EQUATION deltaEgE=E1*(ln(NE/N0)+sqrt(ln(NE/N0)^2+.5))
EQUATION meE=0.3283*m0
EQUATION niE=3.59E19*(T/300)^1.5*exp(-EgE/(2*VT))
EQUATION XIE=4.05
EQUATION dVE=EgE/2-VT*ln(NE/niE)
EQUATION epsE=11.8*epsilon
EQUATION DE=1.14E5*NE^-.25

EQUATION AreaE=DAE*20E-8*Scale
EQUATION AreaECont=DAE*20E-8*Scale
EQUATION DAE=.500<0.500<1.00
```

Base

```
EQUATION WB=.010E-4<3.000E-06<.030E-4
EQUATION NB=NB0*WB0/WB
EQUATION EgB=QEg(T)*(EgSiGestr-deltaEgB)
EQUATION EgB0=QEg(T0)*(EgSiGestr-deltaEgB)
EQUATION deltaEgB=E1*(ln(NB/N0)+sqrt(ln(NB/N0)^2+.5))
EQUATION mhB=(mhhSiGestr^1.5+mlhSiGestr^1.5)^.66666667
EQUATION niB=sqrt(NvSiGestr*NcSiGestr*exp(-EgB/VT))
EQUATION XIB=4.05
EQUATION dVB=if (dVBtmp>0.1*VT) then dVBtmp else 0.1*VT endif
EQUATION epsB=(11.8+4.2*x)*epsilon
EQUATION DBase=unB*VT
EQUATION dVBtmp=EgB/2-VT*ln(NB/niB)

EQUATION WB0=.010E-4
EQUATION NB0=5.00E19<2.00E+20<2.00E20

EQUATION x=0.30
EQUATION T0=293

EQUATION areaC=40E-8*Scale
```

Collector

```
EQUATION WC=0.300E-4
EQUATION NC=5.00E16 */ 2
EQUATION EgC=QEg(T)*(1.12-deltaEgC)

EQUATION deltaEgC=E1*(ln(NC/N0)+sqrt(ln(NC/N0)^2+.5))

EQUATION niC=3.59E19*(T/300)^1.5*exp(-EgC/(2*VT))
EQUATION XIC=4.05
EQUATION dVC=EgC/2-VT*ln(NC/niC)
EQUATION epsC=11.8*epsilon
EQUATION DC=1.14E5*NC^-.25
```

Figure B.5: Definition of device data.

Built-in potentials

```
EQUATION VjE0=XIB-XIE-dVE+EgB
EQUATION VjC0=XIB-XIC-dVC+EgB
```

Breakdown voltage

```
EQUATION Ebreak=2.5E5*(1+(log(NC)-14)^3/14)
EQUATION Vbreak=.5*epsC*Ebreak^2/(2*q*NC)

EQUATION EbreakE=2.5E5*(1+(log(NE)-14)^3/14)
EQUATION VbreakE=epsE*EbreakE^2/(2*q*NE)
```

Depletion capacitance, change in basewidth not accounted for.

```
EQUATION CjC0=epsC*areaC/XjC0
EQUATION CjE0=epsE*areaE/XjE0
```

Delays, change in basewidth not accounted for.

```
EQUATION TauC=XjC0/(2*vs)
EQUATION TauB=WB^2/(2.43*DBase)
```

Saturation currents

```
EQUATION IEe=q*areaE*DBase*niB^2/(WB*NB)
EQUATION IEh=q*areaE*DE*niE^2/(WE*NE)
EQUATION ICe=q*areaC*DBase*niB^2/(WB*NB)
EQUATION ICh=q*areaC*DC*niC^2/((WC-XjC)*NC)
```

Depletion widths

```
EQUATION XjC0=sqrt(2*NB*epsC*epsB*VjC0/(q*NC*(epsB*NB+epsC*NC)))
EQUATION XjE0=sqrt(2*NB*epsE*epsB*VjE0/(q*NE*(epsB*NB+epsE*NE)))

EQUATION XjCtmp=If (Vbc>(0.99*VjC0)) then XjC0*.1 else XjC0*sqrt(abs(1-(Vbc/VjC0))) endif
EQUATION XjC=if (XjCtmp<(0.99*WC)) then XjCtmp else 0.99*WC endif

EQUATION XjEtmp=If (Vbe>(0.99*VjE0)) then XjE0*.1 else XjE0*sqrt(abs(1-(Vbe/VjE0))) endif
EQUATION XjE=if (XjEtmp<(0.99*WE)) then XjEtmp else 0.99*WE endif
```

Mobility,velocity and diffusion

```
EQUATION unBSiGe=200   According to Dr. Erben   EQUATION unBSi=un1+(un2-un1)/(1+(NB/Nref)^gamma)
EQUATION un1=80*(T/300)^-.45                    EQUATION un10=80*(T0/300)^-.45
EQUATION un2=1430*(T/300)^-2.25                 EQUATION un20=1430*(T0/300)^-2.25
EQUATION Nref=1.12E17*(T/300)^3.2               EQUATION Nref0=1.12E17*(T0/300)^3.2
EQUATION gamma=.72*(T/300)^.065                 EQUATION gamma0=.72*(T0/300)^.065
EQUATION vs=1.32E7/(1+1.33E-3*T)
EQUATION unB=if (x<.10) then unBSi else unBSiGe endif
EQUATION unC=un1+(un2-un1)/(1+(NC/Nref)^gamma)  EQUATION unC0=un10+(un20-un10)/(1+(NC/Nref0)^gamma0)
EQUATION unE=un1+(un2-un1)/(1+(NE/Nref)^gamma)
EQUATION uhB=1.14E5*NB^(-.25)/VT
```

Bandgap and intrinsic carrier conc.

```
EQUATION QEg(_T)=(1.1785-9.025E-5*_T-3.05E-7*_T*_T)/1.124
EQUATION EgSiGestr=.9646*(1.165-.75*x)
EQUATION NcSiGeXstr=2*(2*pi*.3272*m0*kB*T/h^2)^1.5*(4+2*exp(-.6*x/VT))*1E-6
EQUATION NcSiGeLstr=2*(2*pi*.2217*m0*kB*T/h^2)^1.5*4*exp((-1.0709+1.366*x-.1615*x*x)/VT)*1E-6
EQUATION NcSiGestr=NcSiGeXstr+NcSiGeLstr
EQUATION NvSiGehstr=2*(2*pi*mhhSiGestr*kB*T/h^2)^1.5*1E-6
EQUATION NvSiGelstr=2*(2*pi*mlhSiGestr*kB*T/h^2)^1.5*exp(-.155*x/VT)*1E-6
EQUATION NvSiGestr=NvSiGehstr+NvSiGelstr
EQUATION mhhSiGestr=m0/((1-x)/.49+x/.28)
EQUATION mlhSiGestr=m0/((1-x)/.16+x/.044)
```

Constants

```
EQUATION E1=0.009
EQUATION N0=1E17
EQUATION VT0=kB*T0/q
EQUATION epsilon=8.854E-14
EQUATION q=1.602E-19
EQUATION kB=1.38E-23
EQUATION m0=9.1095E-31
EQUATION h=6.626E-34
```

Figure B.6: Equations used for defining the intrinsic shell.