Radio Frequency Integrated Circuits for 24 GHz Radar Applications

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To Victoria

Abstract

This thesis presents radio frequency integrated circuits and subsystems, together with packaging solutions, for fully integrated compact and low cost Silicon-Germanium (SiGe) 24 GHz transceivers developed during the European Commission funded project ARTEMIS.

The circuits have been manufactured using a commercially available SiGe HBT semiconductor process at ATMEL (Heilbronn, Germany) featuring transistors with 0.8 μm emitter structures, f_{max}=90 GHz and f_T=80 GHz. For all circuits, standard 20 Ωcm substrate has been used.

Sub-circuits that have been designed and manufactured are 12 GHz VCO:s, polyphase filters, LO pump amplifiers, LNA:s, down- and up-conversion subharmonic mixers, complete receivers and complete transmitters. Measured results of individual circuit blocks, subsystems (e.g. VCO together with polyphase filter) and system performances is presented.

A low loss 24 GHz chip-to-PCB transition using Low Temperature Co-fired Ceramic (LTCC) packaging has been manufactured and evaluated, including a balun structure to interface the differential RFIC with a high gain single ended off-chip patch antenna array.

Finally, measurement techniques for on-chip differential circuits is presented.

Acknowledgements

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Fourthly, I would like to thank former ARTEMIS project members Dr. Ertugrul Sönmez, Dr. Peter Abele and Prof. Hermann Schumacher for their great companionship and for their pioneering work in SiGe RFIC design. In particular, Dr Ertugrul Sönmez has given me countless advice on the more advanced topics in circuit design as well as providing me with circuits for use in the receiver and transmitter presented in this thesis.

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Contents

Chapter 1

Introduction

1.1 Background and applications

The license-free 24 GHz industrial, scientific and medical (ISM) band has been identified as a potential host for future Bluetooth-like short-range wireless systems, but has so far been restrained from widespread consumer deployment by the lack of low cost millimeter-wave circuitry with sufficient performance. While drastically increasing the operating frequency (x10 compared to Bluetooth) represents obvious advantages in the form of higher absolute bandwidths, reduced interference problems (from e.g. microwave ovens, Bluetooth and WLAN), reduced size of antennas and lower health hazard from EM radiation (due to the smaller penetration depth in human tissue), it also puts higher demands on packaging and semiconductor technology.

This thesis presents the development of RFIC:s and packaging solutions for a fully monolithic SiGe based receiver and transmitter front end within the European Commission funded project ARTEMIS ('Advanced RF Frontend Technology using Micromachined SiGe'), aiming to demonstrate the feasibility of inexpensive, compact short-range radio frequency subsystems for the 24 GHz ISM band. Two main applications for the radio systems were targeted

- Short range Bluetooth-like communication devices featuring low gain on-chip antennas to remove all chip to chip-carrier high frequency interconnects and therefore greatly simplify packaging issues. To increase antenna efficiency, the antenna metallization was deposited on thick organic dielectrics (BCB) on top of the silicon wafer, in combi-

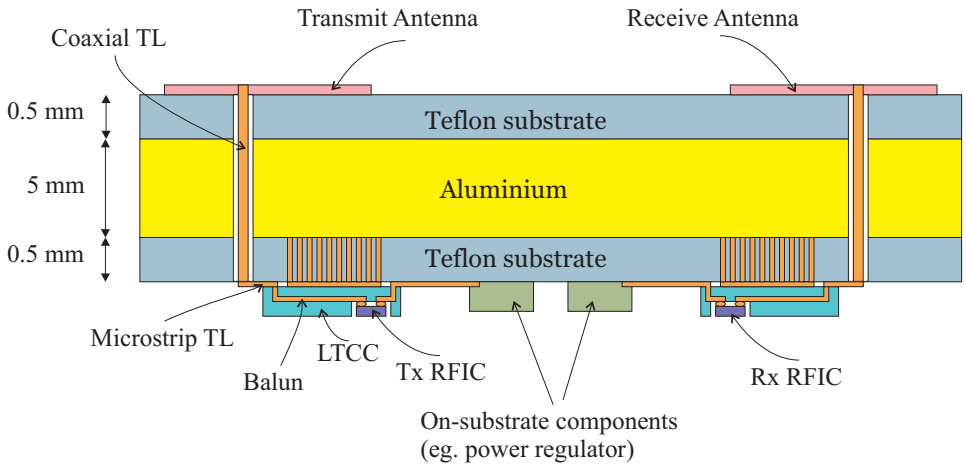


Figure 1.1: Radar sensor module consisting of separate Tx and Rx RFICs on LTCC carriers with off-chip high gain patch antennas

nation with selective removal of the (lossy) silicon substrate (so called micromachining) in regions of high field densities [1]. A possible packaging solution is standard wire bonding, or flip-chip mounting, directly to a cheap circuit board (e.g. FR-4), with glob-top coating [2] of the RFIC for mechanical protection.

- Radar (*RAdio Detection And Ranging*) sensors for traffic surveillance or pre-crash sensing, featuring high gain off-chip patch array antennas. LTCC packaging was used to provide the chip-to-PCB signal transition, including a balun structure to convert the differential input of the receiver (or differential output of the transmitter) to the single ended PCB microstrip line connecting to the antenna array, see Figure 1.1.

The work presented in this thesis has mainly been focused on subsystems for the radar sensor, although some design choices have been made, such as pad placement and selection of Vcc, to ensure compatibility with short range communication device requirements as well.

The requirements of low cost and compactness have been met by using fully integrated receivers and transmitters in a silicon germanium (SiGe) semiconductor process. This is feasible for three reasons. Firstly, at 24 GHz all passive components become very small, especially if transmission lines are used only as short interconnects and not as resonators, stubs, transformers etc. This small size directly translates into a low price of the RF

front-end, especially when compared to the more traditional designs using discrete III-V devices. Secondly, the effective radiated power (EIRP) in the 24 GHz ISM (Industrial, Scientific and Medical) band is restricted by European Telecommunications Standards Institute (ETSI) regulations [3] to 100 mW, meaning that if a 20 dBi gain antenna is used (as in the targeted radar application) the power amplifier need only to deliver about 0 dBm (slightly more to compensate for losses in the balun and interconnects). Thus, since the on-chip power levels are low, the thermal effects can be handled even with the PA integrated on the same die. Thirdly, both the receiver and the transmitter have been designed using a direct conversion architecture. For the receiver, this means that the high-Q off-chip IF filters and IF downconversion stages used in a superheterodyne architecture are replaced by low-pass filters and baseband amplifiers that are easily integrated monolithically. Also, no (typically off-chip) image filter is required between the LNA and the mixer.

Earlier work on monolithic transceivers for the 24 GHz band is represented by the phased-array receiver in [4], featuring a 4.8 GHz IF superheterodyne architecture implemented in a $f_T = 120$ GHz BiCMOS process consuming 11.55 mm^2 chip area. The targeted applications are ultrahigh-speed wireless communication and long distance radar, making the receiver less suitable for low-cost short-range applications. No work on a 24 GHz transmitter counterpart has been reported so far.

In [5] the first fully monolithic SiGe receiver for the 24 GHz band was presented. The system features a single-ended superheterodyne receiver implemented in a $f_T = 50$ GHz HBT process. Later, this work has been extended into a fully differential design [6] using the same process as in this thesis. A transmitter has also been developed, reusing most of the components from the receiver. By utilizing an image-rejection architecture no off-chip filters were needed. Fundamental mode mixing (i.e. the VCO operates at 24 GHz) has been used, implicating a higher susceptibility to DC offsets compared to the subharmonic approach adopted in this thesis.

In [7] a 24 GHz transceiver chip is reported using a $f_{max} = 84$ GHz SiGe(C)-HBT:s BiCMOS technology. This work is an extension of a transmitter reported in [8]. The transceiver does not include an on-chip LNA, has (only) one single-balanced mixer, is based on a single-ended design using microstrip transmission lines (strip on top layer metal, signal ground on bottom layer metal, silicon dioxide as substrate) both as interconnects and as resonators, and so differs from the work in this thesis in many respects.

1.2 Outline of the thesis

The focus of this thesis is primarily on RFIC design for high microwave frequency (like 24 GHz) applications, and most of the chapters are thus related to this subject. Schematics of all implemented circuits are given with explanations of the design choices made and the purpose of each component included. For the more complex circuits, like the VCO and the mixers, explanations of their functionality are provided and the most important derivations have been included for completeness sake. Furthermore, some details has been provided on items such as SiGe HBT vs Si BJT specifics, EM modelling of passive components in IC:s etc.

The second part of this thesis concerns packaging of the RFIC:s, mainly focusing on the design of a differential chip to single ended PCB transition for 24 GHz signals using LTCC carrier. Finally, some information on how the measurements were conducted has been provided.

1.3 Contributions

Parts of the material in this thesis have been presented at the following conferences:

- P. Lindberg, E. Öjefors and A. Rydberg, "A SiGe 24 GHz zero-IF downconverter," presented at GigaHertz Conference, Linköping, Sweden, 2003.
- P. Lindberg, E. Öjefors and A. Rydberg, "A SiGe HBT 24 GHz Sub-Harmonic Direct-Conversion IQ-Demodulator" in Proc. SiRF'04, September, 2004
- A. Rydberg, P. Lindberg and E. Öjefors, "Towards MEMS-based mm-Wave Radar," presented at RVK Conference, Linköping, Sweden, 2005.
- H. Schumacher, P. Abele, J. Berntgen, K. Grenier, J. Lenkkeri, P. Lindberg, E. Öjefors, R. Plana, W.-J. Rabe, A. Rydberg, E. Sönmez, and K. Wallin "Compact, low-cost 24 GHz modules using micromachined Si/SiGe HBT technology," presented at IST Mobile and Wireless Communications Summit, Lyon, France, 2004
- P. Lindberg, E. Öjefors and A. Rydberg, "A 24 GHz on-chip differential Wilkinson coupler using lumped components," Presented at GigaHertz Conference, Uppsala, Sweden, 2005.

- P. Lindberg, E. Öjefors and A. Rydberg, "A SiGe 24 GHz monolithically integrated direct conversion receiver," Presented at GigaHertz Conference, Uppsala, Sweden, 2005.
- P. Lindberg, E. Öjefors and A. Rydberg, "LTCC packaging for a 26 GHz SiGe receiver," Presented at GigaHertz Conference, Uppsala, Sweden, 2005.

Chapter 2

System architecture and process technology

2.1 Front End Architecture

The 24 GHz transceiver developed within the ARTEMIS project was divided into separate transmitter and receiver chips, see Figure 2.1, due to isolation constraints and to relax heat dissipating requirements of the chip carriers. For cost and packaging reasons, the circuits have been implemented monolithically, which was made possible by the choice of a direct conversion architecture. The receiver front-end is schematically shown in Figure 2.2. The transmitter shares almost all subcomponents with the receiver, with the exception of the LNA being replaced by a PA and a modified mixer core used for up-conversion. All circuits are designed for a unipolar supply voltage of 3V.

The main building blocks of the front end are shown in Figure 2.1. Looking at the transmitter (at the top) section of the transceiver, a VCO (Voltage Controlled Oscillator) produces a 12 GHz signal that is fed to two mixers 45° out of phase. In the more traditional case (called "fundamental mixing"), a 24 GHz LO signal would have been fed to the two mixers 90° out of phase for I/Q-modulation. In the architecture employed in this work, the mixers have been designed to operate at twice the LO frequency (so called "sub-harmonic mixing"), meaning that there is an intrinsic frequency (x2) multiplication inside the mixer that will also double the phase shift, hence the 45° instead

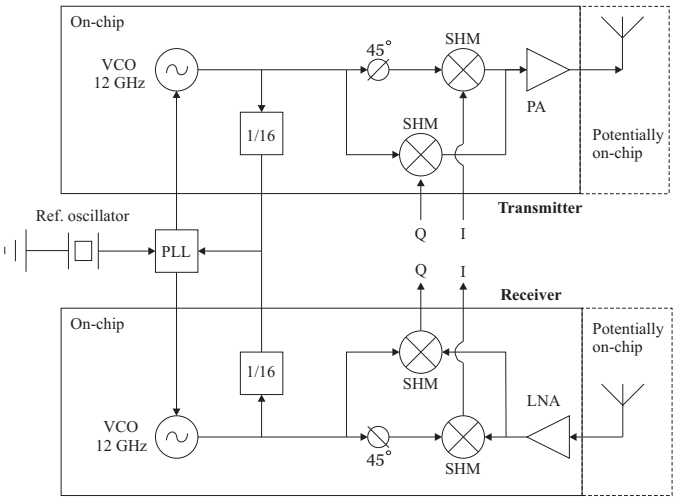


Figure 2.1: Simplified block schematic of targeted 24 GHz transceiver system, consisting of separate receiver and transmitter RFICs locked to a common off-chip PLL

of the normal 90°. The second port of the mixer is fed by baseband signals (either I or Q) and the two outputs of the mixers are combined at the input of the power amplifier (PA) that is connected to the antenna. Since the baseband signal is immediately shifted up to the carrier frequency, as opposed to using an intermediate frequency (IF) this architecture is called direct conversion. For transmission, direct conversion has been shown to be an attractive means of reducing hardware complexity and cost [9][10], with the most significant problem being the potential disturbance of the LO by the PA (so called 'injection pulling') [11]. For reception however, direct conversion implies some serious problems [12][13][14][15]:

DC-offsets: If the LO signal leaks (through substrate, inductive or capacitive coupling) to the RF input of the mixer, either directly or through the LNA, it will self-mix and create a DC voltage that will disturb the received signal and, even worse, may saturate the following stages of the receiver. The same effect happens if a large interfering signal at the LNA or mixer input leaks to the LO input. This effect can either be removed by AC-coupling (in which case a modulation method should be used at the transmitter side that minimizes the signal energy close to dc after down-conversion, so called 'dc-free coding') the baseband

signal, or, as in this work, by using sub-harmonic mixing (i.e. the LO and RF frequencies are separated).

I/Q mismatch: Since the 24 GHz signal is directly converted to baseband I and Q signals, it is more difficult to provide a perfect 90° phase separation and equal magnitudes compared to when down-converting from an IF frequency (as in superheterodyne receivers). This means that the received signal constellation will be altered, increasing the bit error rate. This problem is more pronounced in discrete designs and tends to be less severe with high levels of integration. No special method (such as using I/Q calibration look-up tables), except for highly symmetric layouts, have been attempted to reduce the I/Q mismatch.

Even-order distortion: If two strong, closely spaced (in frequency) interfering signals are present at the input of the LNA, any even order non-linearity in the amplifier will produce low-frequency beats at the difference frequency of the two signals. This term is fed to the RF-input of the mixer, where it would ideally be translated to a high frequency and removed by the output filter. However, as there is a finite direct feed-through from the RF to the baseband ports in all real mixers, some of it will appear at the output corrupting the received signal. By using a completely differential system, all even-order distortion is (ideally) removed.

1/f noise: As the received signal is directly converted to DC and is only amplified by the LNA and mixer prior to this, any 1/f (flicker) noise present at the output will greatly reduce the signal to noise ratio. This problem is more severe in CMOS technologies, with typical corner frequencies of a few MHz, than in bipolar technologies with typical corner frequencies of a few kHz. No special techniques, other than the usage of bipolar transistors, have been used to counter this effect.

To provide a clean LO signal without temperature and time drift and with low phase noise, the VCO should be phase-locked to an off-chip crystal oscillator (a so called phase locked loop, PLL). Since there are no commercially available PLL:s working at 12 GHz, the VCO is connected to a frequency divider (or prescaler) that divides the frequency by a factor of 16, providing for a simpler off-chip transition and cheaper PLL circuit.

By connecting the VCO:s of the receiver and the transmitter to the same PLL, the LO signals in the receiver and transmitter can be phase synchronized, which is required by the radar application. Furthermore, by using IQ

modulation and demodulation, the phase and amplitude of the carrier (24 GHz) signal is easily controlled, implying that any modulation method (like BPSK, QPSK, 16 QAM etc) can be used.

A more complete schematic, with buffer and pump amplifiers included, of the receiver (with the transmitter being identical except for the LNA being replaced by a PA) is shown in Figure 2.2. As all components are either designed to be narrow banded (e.g. to get as much gain as possible from the active devices in amplifiers) or are narrow-banded by nature (e.g. the polyphase filter), there is a distributed filter action taken place throughout the system in addition to the explicit low-pass filters following the mixers.

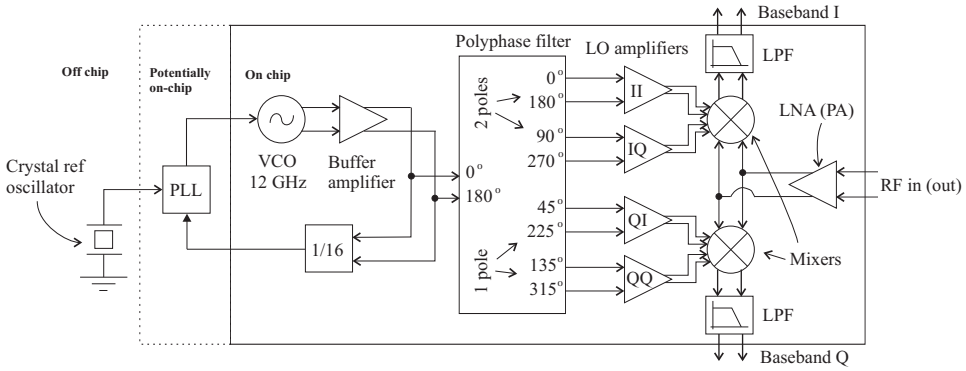


Figure 2.2: Block schematic of receiver and transmitter

By using sub-harmonic x2 mixing in the IQ-(de)modulator and a fully differential topology, several advantages are obtained:

- The VCO operates at half the RF frequency (i.e. 12 GHz) resulting in

    1. a larger unstable region of the active devices, making the oscillator less sensitive to terminating and load impedances. In contrast, oscillators working close to f_{max} may require many design iterations just to achieve oscillation start-up.
    2. higher resonator Q (on-chip LC tank), translating into lower phase noise and higher output power. The higher gain of the active devices at 12 GHz further increases the maximum available output power. These advantages are however counter-acted at the system level by the intrinsic frequency doubler in the mixer

adding 6 dB to the phase noise, and the LO input ports of the mixers consuming more (x2) power than an ordinary mixer

3. no disturbance of the transmit LO by the PA (s.c. "injection pulling" or "injection locking") since the output frequency is not close to the oscillating frequency
4. no LO power at 24 GHz (from second order non-linearities) because of the differential output
5. reduced LO to antenna coupling (from the inductor in the resonator tank) when using an on-chip antenna, since as the coupling has a maximum at the antenna resonance frequency, which is far from the LO frequency

- no DC offsets from LO self-mixing since there is (ideally) no LO signal at the RF frequency
- no base-band offsets from second order distortion of RF input signals because of the differential topology
- reduced cross-talk between circuit blocks from supply and ground signal disturbances because of (ideally) no high-frequency currents in Vcc lines or ground. This can be even more important in mixed signal environments, for example with PLL circuitry on-chip, where e.g. transients from digitial switching can severly degrade system performance
- higher output power is available from the active devices due to the differential design. The output power, which in terms of voltage is limited by the breakdown voltage of the transistors (somewhere between BV_{CEO} and BV_{CBO} - usually closer to BV_{CBO} in a real circuit [16]) is increased due to the effective "doubling" of the breakdown voltages of the transistors, i.e. only half the output voltage is over each transistor.

2.2 SiGe Semiconductor technology

The circuits have been realized in Atmels Silicon Germanium (SiGe) heterojunction bipolar transistor (HBT) semiconductor process *SiGe2RF* [17], featuring a 0.8 μm lithography, 3 metal layers (see Figure 2.3), MIM-capacitors, 4 resistor types, lateral PNP:s and pn/zener/varactor/schottky-diodes. Important advantages of SiGe HBTs over III-V devices (such as GaAs or InP)

more commonly used at high microwave frequencies, are that, as they are silicon based, they

- have lower price
- have higher yield
- are compatible with CMOS technology (s.c. BiCMOS)
- have better thermal properties
- are process compatible with etching techniques

thus enabling fully monolithic integrated transceivers, including digital circuit blocks (see e.g. [4]), using simple packaging. A pure CMOS process would also have the same advantages as listed above, but applications have so far been limited to low frequency (< 10 GHz) low power systems [18].

The main difference of SiGe HBTs (Heterojunction Bipolar Transistors) compared to standard silicon bipolar transistors (BJTs) is the slight addition of germanium ($\sim 5 - 30\%$, depending on doping profile) in the base layer, forming SiGe/Si junctions at the base-emitter and base-collector interfaces. This affects (bends) the conduction band structure, introducing a drift field through the base which in turn increases the current gain [19]

$$\beta_0 \sim \frac{N_E}{N_B} \exp\left(\frac{E_{gE} - E_{gB}}{kT}\right) = \frac{N_E}{N_B} \exp\left(\frac{\Delta E_g}{kT}\right) \tag{2.1}$$

where E_{gE} is the bandgap of Si in the emitter (1.12 eV at 300K), E_{gB} is the bandgap of SiGe in the base (0.66-1.12 eV at 300K depending on Ge fraction), N_B and N_E are doping concentrations in the base and emitter respectively, and $kT = 0.026eV$ at 300K. From (2.1) it can be seen that a high Ge fraction in the SiGe base layer results in a massive increase of current gain β. The bandgap of the SiGe is reduced from 1.12 eV by approximately 75 meV for each 10% of Ge introduced [20] (a factor of 17.9 times higher current gain for each 10%). However, since the Ge lattice constant (i.e. size of crystal cell) differs from that of Si by roughly 4.2% ($a_{Si} = 0.5431nm$ and $a_{Ge} = 0.5658nm$), the base layer is under compressive strain which could lead to breaks in the crystallinity, setting an upper limit to possible Ge fractions. The semiconductor process used in this work - SiGe2 from Atmel - uses a high and constant Ge mole fraction of about 20% [21].

The extra DC current gain is traded of for higher power gain, higher f_{max}, lower thermal noise and higher Early voltage [22] (due to less modulation of the space region into the neutral base) by increasing the base doping,

thus reducing r_b (see Figure 2.4). A high f_{max} is necessary when working at high microwave frequencies (as a rule of thumb, the working frequency should preferably be a factor a 8-10 below f_{max}), and advantageous at lower frequencies for low-power applications. The DC current gain is however not a very critical parameter for RF devices and going above a couple of hundred is usually not interesting. The reduced base resistance for current gain trade is on a one to one basis, i.e. the base doping can be increased by the exact same amount as the current gain is decreased.

The technology used features a 0.5 μm minimum electrical emitter size (corresponding to a 0.8 μm geometrical size) of NPN transistors with f_T=80 GHz ($f_{max}\approx$ 90 GHz) and BV_{CE0}=2.5 V using selective implanted collector (SIC), 3 Al metal layers, inductors, nitride capacitors and four different types of resistors. Non-SIC (power) transistors with f_T=50 GHz and BV_{CE0}=4V can be used together with SIC (RF) transistors on the same chip as the option is defined by a single mask. The active devices are modelled in the design kit from the manufacturer using HICUM (High Current Model) models verified well into the $\geq$ 24 GHz region targeted in this thesis.

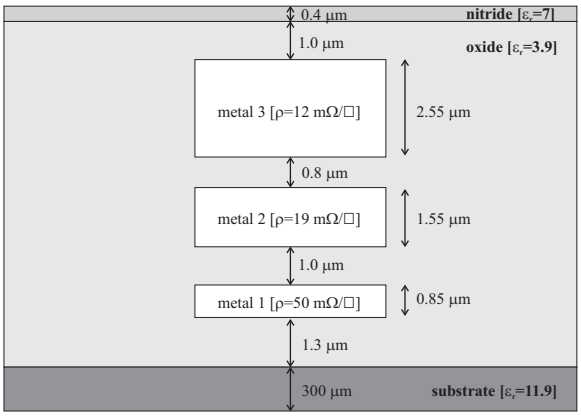


Figure 2.3: Schematic cross section of metal layers in Atmels SiGe2 process

The substrate is of p-type with options of using conventional 20 Ωcm or high-resistivity 1000 Ωcm. Close to the substrate surface (down to $\sim$1.5μm), the substrate is heavily p-doped ($\sim$150 $\Omega/\square$) forming a s.c. p^+ channel stopper region. This region is connected to ground potential using substrate vias (see Figure 2.5). Since the subcollector of HBT:s are always connected to a high potential ($>$ 1 V) the subcollector-substrate diode is reverse biased. The channel stopper is of course removed in the vicinity of the subcollectors.

Traditionally, there has been a substantial price difference between high and low ohmic substrates, but today that is no longer true. The main advantages of the 1000 Ωcm substrate are lower collector-substrate capacitance (due to the depletion layer extending further into the substrate) and higher Q-values of passive structures such as inductors, transmission lines and antennas. The main disadvantage is the increase of transistor spacing necessary to avoid the depletion layers of the sub-collectors to meet, making layouts more sparse which in turn leads to increased losses and impedance mismatches from interconnect lines. Also, high resistivity substrate is not compatible with CMOS circuitry. To summarize, the substrates have different merits and the selection will be dependent on the application.

2.2.1 Active components

Transistors are the only active components used in the circuits, however with two different applications: SIC HBT:s for amplification and non-SIC for realizing varactors. Although lateral PNP transistors are supported by the manufacturer, the high frequency (above a few MHz) performance is rather limited and the area consumption is somewhat excessive, and so have therefore not been used. The (small-signal) model for the transistor, including noise sources, that is used in the following discussions is shown in Figure 2.4.

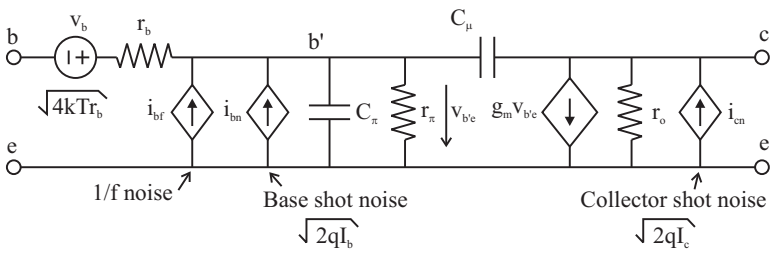


Figure 2.4: Small-signal model of transistor, including noise sources

Transistors

RF transistors (using SIC) with double base contacts (for reduced base resistance) and single collector and emitter contacts (s.c. CBEB configuration) with emitter lengths of 5-20 μm, see Figure 2.5, have been used for amplification in the circuit designs. Although transistors with two collector fingers

have marginally better performance[1], only one collector finger has been used for practical reasons - with two collector fingers and two base fingers, the emitter finger is completely confined, thus complicating the layout design. For optimum high frequency performance (i.e. maximum cutoff (or transition) frequency[2] f_T), J_C=1.5 mA/μm^2 with $V_{CEQ} = 1 - 1.8V$, see Figure 2.6.

This voltage range together with the supply voltage of 3V limits the number of stacked devices to 2, which has some implications for the circuit designs, most notably for the mixer cores (see Section 3.0.9 and 3.0.10).

The current consumption for a typical 10 μm device is relatively high – $I_{CQ} = 1.5mA/\mu m^2 \times (0.5 \times 10\mu m^2)$=7.5 mA, and for a differential device that current is doubled. As all input impedances are low-ohmic at high radio frequencies like 24 GHz (due to C_π and C_μ), usually the current limits the

[1] f_T=75 GHz and f_{max}=75 GHz for CBEBC compared to f_T=75 GHz and f_{max}=70 GHz for CBEB as reported in [6]. Note that these are somewhat more conservative numbers compared to those reported by the manufacturer

[2] The maximum transition frequency f_T, i.e. the frequency were the (extrapolated) AC current gain is reduced to 1, is a common figure of merit for a transistors high frequency performance. Referring to Figure 2.4, with the input driven by an AC current source and the output shorted (so that C_μ is in parallel with C_π), it can easily be shown [23] that the high frequency current gain β_{ac} is equal to

$$\beta_{ac}(j\omega) = \frac{I_c}{I_b} = \frac{\beta}{1 + j\omega(C_\pi + C_\mu)r_\pi} = \frac{g_m}{1 + j\omega(C_\pi + C_\mu)}$$

and reduces to 1 at

$$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$$

implying that f_T increases linearly with I_{CQ}, until high-injection effects (most importantly base push-out or Kirk effect [20]) starts to dominate, reducing f_T beyond a certain current density. Because the onset of the Kirk effect is delayed with increased collector doping, there is a fundamental trade off in BJTs between speed (increased f_T with increased collector doping) and output power (decreased BV_{CEO} with increased collector doping). For a RF designer, another measure of high frequency capabilities is often more useful: the maximum frequency of oscillation f_{max}. Defined as the frequency where the power gain is reduced to 1, with the input driven by a source impedance Z_s and the output conjugately matched, it mainly differs from f_T in that it includes the effect of the base resistance r_b. The base resistance reduces the power gain because of the voltage division between r_b and C_μ. Even more importantly, though not related to f_{max}, is that the base resistance produces thermal noise directly at the input terminal of the transistor (b' in Figure 2.4), obviously the worst location for a noise source! It can be shown [20] that the maximum operation power gain is inversely proportional to f^2 and that f_{max} is given by

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_\mu r_b}}$$

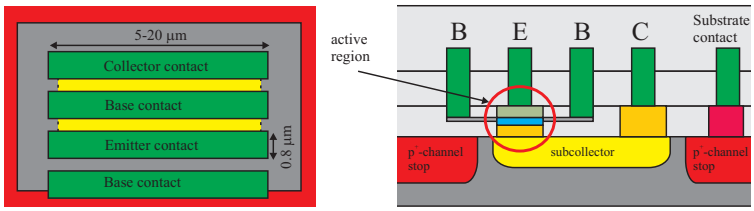


Figure 2.5: Layout of transistor, top (left) and side (right) view

maximum output power and linearity of the devices, so a high DC current is typically required anyway. For lower frequencies or lower gain, the current can be reduced.

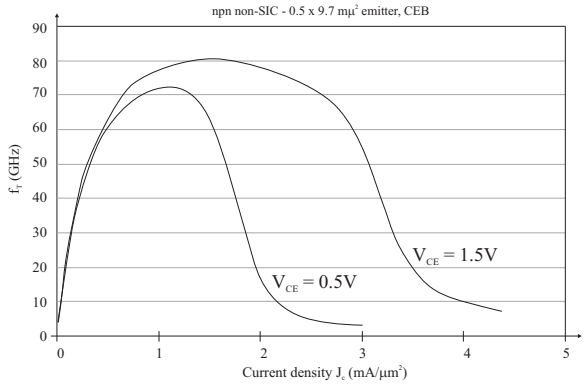
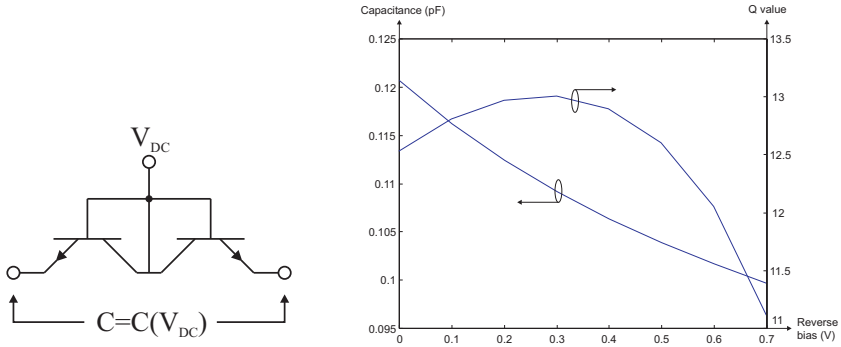


Figure 2.6: Cutoff frequency f_T of SiGe2 transistor as a function of current density

Varactor diodes

To tune the oscillating frequency of the VCO, a variable capacitor (s.c. varactor) has been included in the resonator tank. Varactor diodes are supported in the semiconductor process but they require one additional (optional) mask layer. Instead, the emitter-base junctions of NPN non-SIC transistors have been used to the same effect. Since the depletion region is a function of the reverse bias (it expands at higher reverse bias), two transistors can be connected to form a symmetrical (important in differential VCOs) three-terminal device where the third terminal sets the capacitance

value with a DC voltage, see Figure 2.7.



(a) Schematic of varactor (b) Simulated capacitance and Q of varactor

Figure 2.7: Variable capacitor (Varactor) using NPN transistors

As can be seen from the simulated values of the varactor (Figure 2.7) used in the 12 GHz VCO, with 2x4 NPN:s in parallel, the Q of such a capacitor is not very high (in the order of 10-15) and will therefore significantly impact the phase noise of the oscillator. A higher reverse bias will decrease the effect of the limited Q, partly because the Q increases with reverse bias (up to about 0.3 V) but mainly since the total impedance increases resulting in less current through the varactor (and therefore less losses). A maximum reverse bias of 0.5 V is allowed according to the design rules from the manufacturer, but in reality much higher voltages can be used to give a wider tuning range, as seen in the measurements of the VCO. Due to the limitations of the varactor, there is a compromise between a large tuning range (to compensate for process tolerances, temperature drift and for use in wide-band systems) and phase noise. The phase noise is also in practice increased for VCO:s with a large tuning range because the oscillating frequency is more sensitive to noise on the DC control voltage.

2.2.2 Passive components

The passive circuit elements is often the performance limiting factor in silicon based circuits, the reason being their rather limited Q values. This is especially true for inductors, where reactance to resistance ratios are typically in the modest 5-15 range, but even the capacitors have far from ideal characteristics at 24 GHz. There are three reasons for the limited Q-values of the passive components: substrate losses, metal losses and parasitic substrate capacitance. By the substrate capacitance loss it is meant the increase of an

already existing resistive part caused by the parallel capacitance to ground, i.e. not associated with any losses from this coupling.

The behavior of the passive devices (not including interconnect lines) as individual components are adequately predicted in schematic simulations by models provided in the manufacturers design kits. However, for more complex and distributed structures such as the polyphase filter, the Wilkinson combiner, long interconnects at impedance sensitive locations etc, EM simulations are necessary to predict the effects of metal losses and parasitics. The simplified layer configuration used for the EM simulations is shown in Figure 2.8.

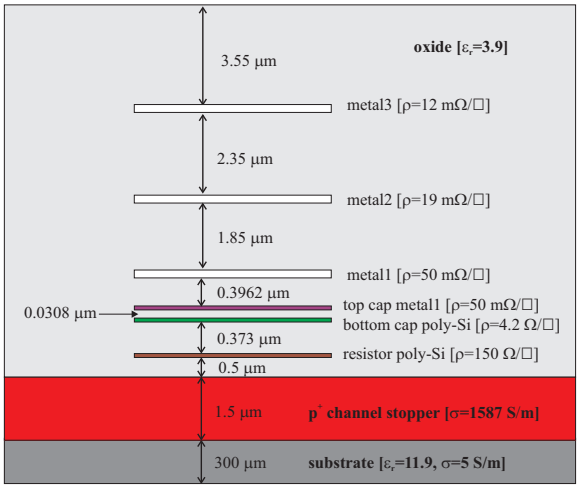


Figure 2.8: Schematic cross section of metal, capacitor and resistance layers used in IE3D simulations of polyphase filter

Resistors

The design kit supports four kinds of resistor values: 4 Ω/□ low ohmic, 150 Ω/□ medium ohmic, 430 Ω/□ and 1500 Ω/□ high ohmic resistors. Generally, since resistor values can differ slightly from different wafer runs and wafer locations, it is good design practice to use identical resistor values (and types) for e.g. resistive dividers for transistor biasing, since the changes will apply equally for closely space resistors. As an example, a 2 $k\Omega$ and 500 Ω divider (1:5) is preferably implemented as one 2 $k\Omega$ resistor and four 2 $k\Omega$ resistors in parallel, even though it will consume more space than building the 500 Ω resistor as a separate component.

Capacitors

Capacitors are today available in two types. The first is the nitride capacitor, shown in Figure 2.9, with poly-silicon as bottom electrode, a metal 1 (aluminum) top electrode and a 67 nm thin nitride layer deposited in between for a capacitance of 1.1 $fF/\mu m^2$. The terminals are connected by metal 1 and metal 2, where the top electrode have vias stacked up to metal 2 as shown in Figure 2.9. The second capacitor option is a high-Q MIM (Metal-Insulator-Metal) type embedded between metal 2 and 3 for a capacitance of 0.93 $fF/\mu m^2$. Since MIM capacitors is a recent addition to the process, only the nitride type has been used. The MIM type has, in addition to lower ohmic losses because of the metal bottom electrode, the additional advantage of a lower parasitic substrate capacitance (since the device is located further away from the lossy substrate compared to the nitride version) increasing the effective Q and reducing substrate noise from being coupled to the bottom electrode.

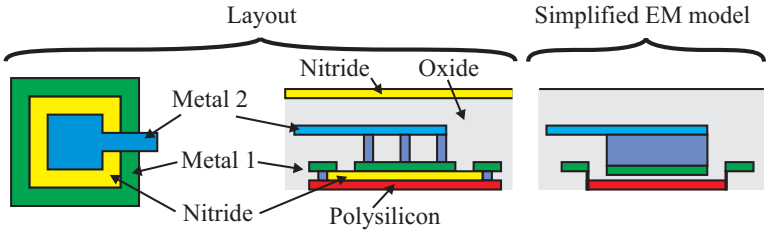


Figure 2.9: Layout of capacitor and simplified EM model

Because of the high aspect ratio in the structure and the multiple dielectric layers – a 0.067 μm nitride layer ($\varepsilon_r = 7$) sandwiched in a 9.68 μm oxide layer ($\varepsilon_r = 3.9$) with 0.4 μm nitride ($\varepsilon_r = 3.9$) on top, the simulation time is rather high and the numerics are somewhat unstable, rendering the component difficult to include in simulations of networks with several components (e.g. polyphase filter). Therefore, for the EM simulations the structure has been simplified: all vias has been replaced with vertical walls along the edges and the complicated dielectricas have been replaced by a homogenous oxide layer. To compensate for the decrease in capacitance due to the change of dielectrica, the distance between the electrodes were reduced to obtain the measured 1.1 $fF/\mu m^2$.

As the capacitor is not fully symmetric, with different parasitic substrate capacitance at each terminal being the most important effect, two identical

capacitors can be placed in a series back-to-back configuration to ensure full symmetry. This however reduces the total capacitance of the device to half the value of each capacitor

Inductors

Since all on-wafer impedances at 24 GHz are by nature capacitive, inductors are extensively used for impedance matching. Also, since the output impedances of the active devices are not very high in this frequency region, and since they consume 1 V for proper functionality, inductors are in some instances used as (high frequency) current sources for common mode rejection. Finally, inductors are used for noise-less emitter degeneration to increase linearity and input impedances of the amplifiers. Although spiral inductors are supported by the design kit, all inductors have been tailor made in IE3D to optimize the structures for the different applications and to include the effects of the surrounding layout and interconnect lines.

High-Q inductors, for instance when used as collector loading in amplifiers or the resonator tank in the VCO, have spiral inductors using metal 2 and metal 3 in parallel with multiple vias connecting the layers. For applications where the Q is not as critical, like in current sources, the inductors have been realized as circular spirals starting at metal 3 and spiraling down to metal 1. This way the area consumption is kept to a minimum.

Directly below the inductors, the p^+-channel stopper has been removed to increase the Q-value by avoiding eddy currents and reducing the capacitive coupling. Further techniques to reduce losses, although not used in this work, include a patterned ground shield to reduce the capacitive coupling to the substrate while blocking magnetically generated currents (which would reduce the inductance) [24]. A guard ring of metal 1 and 2, connected to the substrate by vias, surrounds all inductors to reduce coupling between the inductors [25] and to provide a co-planar ground plane.

Transmission lines (interconnects)

Transmission line structures for conventional silicon processes have received considerable attention during the last decade, mainly focusing on coplanar waveguide [26] and microstrip lines [27]. Because of the differential topology, the only transmission line structure of interest in this work is the coplanar stripline (CPS) consisting of two side-by-side metal strips, see Figure 2.11. Due to the high losses in the 20 Ωcm silicon substrate and the excessive area consumption, transmission lines have only been used as circuit interconnects

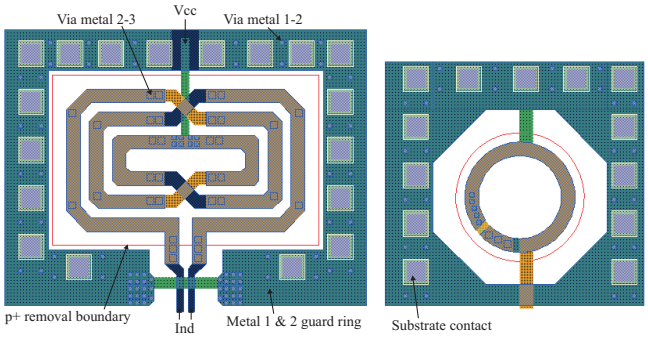


Figure 2.10: Layout of high (left) and low (right) Q inductors

and not as matching stubs or resonators.

Design techniques to reduce losses includes:

- Removing the p^+-channel stopper under the coplanar strips [28] (as is done with inductors and on-chip antennas)
- Using wide strips in the top-most metal layer (metal 3) (which is also the thickest metal layer) to reduce metal losses and parasitic substrate coupling
- Reducing the slot width between the CPS lines to confine the field lines away from the substrate. This is limited by design rules to 1 μm in metal1, 2 μm in metal2, and 3 μm in metal3

CPS lines with high Z_0 can be used to partly compensate for the (parasitic) capacitive nature of all input impedances in the high-GHz region. However, this approach would be very hard to implement in a practical design due to modelling problems and design complexity. Instead, the preferred choice in this work has been to minimize the length of all interconnect lines and use CPS structures with as low Z_0 as possible within the limits of the technology (i.e. metal spacing). This means using as small a distance between the lines as possible and keeping the ground layer close. The low Z_0 is necessary since all impedances are by nature low ohmic at these elevated frequencies, so a low characteristic impedance introduces minimum impedance transformations.

The minimum trace width is limited by current handling capabilities of the metal, with electron migration being the main mechanism for loss of

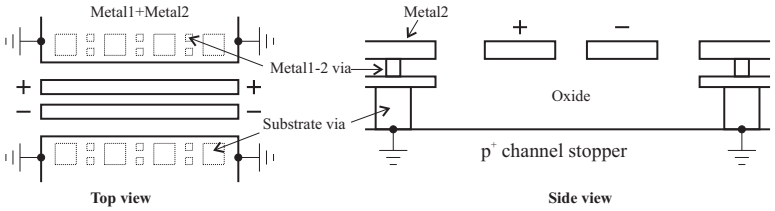


Figure 2.11: Layout of CPS transmission line

reliability. In the used process, metal 1-3 has 3, 5 och 8 $mA/\mu m$ maximum DC current/width respectively. The AC component of the currents can typically be much larger, with a factor 4 often used [16].

Chapter 3

RFIC Subcircuits Design

3.0.3 Interstage Matching (Tuning)

Conjugate matching between inputs and outputs of circuit blocks is well known to provide maximum power transfer from source to load. In most instances, such as at the amplifier-filter or antenna-transmission line interfaces, it is obvious why maximum power transfer is desired. However, in some cases the conjugate match also provides optimum circuit performance even though power transfer per se is not the objective. Such cases are for example the LO and RF inputs of the mixer cores. By conjugate matching these inputs, maximum voltage swing is obtained at the bases of the switching transistors and maximum RF currents are supplied at the emitters of same transistors, hence resulting in maximum conversion gain and minimum noise of the circuit (see Section 3.0.9). As a side-effect, there is also maximum current input at the bases and maximum voltage swing at the emitters, but these have no positive influence on the circuit performance (in fact quite the opposite, since the voltage swing at the emitters causes non-linearities and the LO pump amplifiers must be sized to supply large currents into the bases). For these reasons, the conjugate match is the most common type of impedance matching. For ease of measurement and to make the circuits more general, it is customary to provide conjugate matches at all circuit interfaces by matching to a characteristic (or system) impedance, most commonly 50 Ohms. In this work, no characteristic impedance has been used and all circuits have been designed to work in a specific impedance environment.

The power transfer, or gain, is only improved by matching if the matching components (inductors and capacitors) are not too lossy. It is also not

desirable to let matching components consume excessive die area. For these reasons, it is advantageous if components already present in the circuits can be dimensioned to provide the necessary impedance transformations. In this thesis, the DC feed inductor (between Vcc and collector), together with the AC coupling capacitors, have been used extensively as matching components. This method has the added advantage that physically much smaller components can be used, compared to using (the perhaps more intuitive) large inductors for signal blocking in combination with large coupling capacitors. This type of impedance transformation is most easily understood by using the Smith chart, as described below.

Consider a typical input impedance Z_{in} of some arbitrary circuit, represented here by the base of a npn transistor. It is typically low ohmic and capacitive. This impedance needs to be transformed into the conjugate of the output impedance Z_{out} of some other circuit, here represented by the collector of another npn transistor. For simplicity, the single-ended case is shown. The configuration and impedances are shown in Figure 3.1. By using a small capacitance C (about 100-200 fF at 24 GHz) and a small inductance L (about 0.2-0.6 nH at 24 GHz), Z_{in} is moved along the arcs shown in the Smith-chart to the conjugate of Z_{out}. This method is applicable under most practical conditions, e.g. when $Re(Z_{out}) > Re(Z_{in})$.

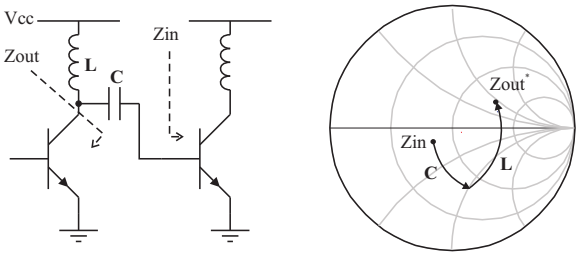


Figure 3.1: Conjugate matching using signal blocking inductor and coupling capacitor

3.0.4 DC Biasing Circuitry

DC biasing of active devices provides the required operation condition, i.e. U_{CEQ} and I_{CQ}, which should be stable over input power, temperature and technology process variations. Since two types of biasing schemes are used throughout, they are discussed in this section and only briefly mentioned in

the text concerning each specific RF circuit.

Biasing of circuits with two stacked transistors

Almost all amplifiers in the transceiver are based on a cascode configuration and therefore falls in the category of devices with two stacked transistors (together with the up and down mixer cores). Since the voltage headroom is restricted to 3 V for the transceiver, and 1.5 V is ideal for optimum high frequency performance, no biasing transistor can be further stacked to set the quiescent current. Instead, current mirrors [29] are used to set the base current of the bottom stage together with a resistive voltage divider that gives the potential at the bases of the upper stage.

Referring to Figure 3.2, the current through T1 is given by R1 according to $(V_{cc} - V_{BEQ})/R1$. Since U_{BEQ} is identical for T1 and the transistors to be biased (T2 and T3), for sufficiently small R2 ($\sim 1k\Omega$, so that the voltage drop from the base current is negligible), I_{CQ} is selected. Resistor R3 isolates the current mirror from the RF input and resistor R1 provides negative feedback that sets and stabilizes the operating point. By using different emitter areas of T1 and the transistors to be biased, the current through T1 can be scaled down significantly reducing the overall current consumption. To minimize quiescent current variations over temperature, the ratio of resistors $R2/(R3 \parallel R3)$ must be equal to the device area ratio $T1/(T2 + T3)$ (where T2 and T3 are the transistors to be biased).

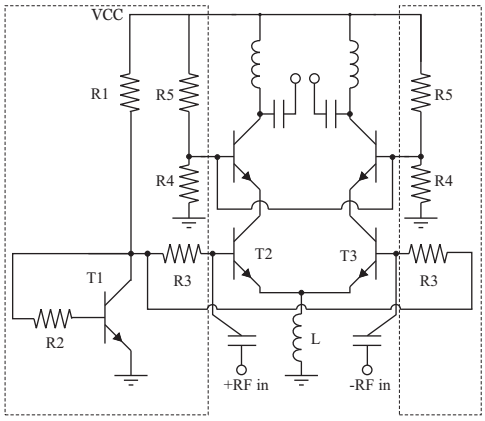


Figure 3.2: Schematic of biasing arrangement for circuits with two stacked transistors

With the current given by T1 and R1-R3, U_{CEQ} is selected for both tran-

sistor layers by the voltage divider R4 and R5. R4+R5 is first chosen so that $I = Vcc/(R4 + R5)$ is much larger than the base current (for stable operation), $\sim 10\%$ of I_{CQ} as a rule of thumb, and R5 is then typically 4-5 times R4 so that the potential at the base is 2-2.5 V (i.e. 0.7 V above U_{CEQ}).

This way, I_{CQ} and U_{CEQ} of both transistor levels can be easily set. The inductor L is used as an AC current source to increase common mode rejection. Further rejection can be obtained by putting a capacitor in parallel with L, selected to give an anti-resonance at 24 GHz. This however reduces the bandwidth of the current source.

Biasing of circuits with no stacked transistors

The circuits that do not use stacked transistors, e.g. the VCO and the last stage of the LNA, are biased using a transistor current source, see Figure 3.3. All details are identical to that described in the previous section, except that the current source now replaces the inductor L and therefore both gives the quiescent current and provides common mode rejection. Since one less inductor is used, this arrangement consumes much less chip area. If further common mode rejection is needed, resistors can be placed at the emitters of the current mirrors to increase the output impedance.

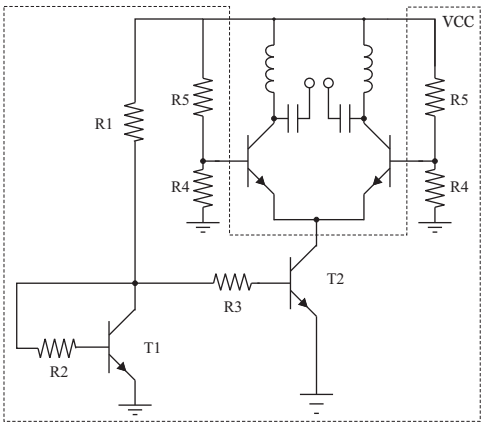


Figure 3.3: Schematic of biasing arrangement for circuits with no stacked transistors

3.0.5 Low Noise Amplifier (LNA)

The low noise amplifier (LNA) is the first circuit block in the front-end and must provide sufficient gain to minimize the impact of mixer noise on the overall noise figure of the receiver (the well-known gain distribution problem, as quantified in Friis equation 3.1). Since the subharmonic mixers, due to the higher transistor count compared to standard Gilbert cells, have a high noise figure (> 15 dB), the LNA needs to provide more than 15 dB of gain without itself adding excessive noise.

$$F_{tot} = F_{LNA} + \frac{F_{Mixer} - 1}{G_{LNA}} + \frac{F_{Baseband} - 1}{G_{LNA}G_{Mixer}} + \dots \tag{3.1}$$

For design of amplifiers (LNA, PA, VCO buffers, LO pump amplifiers etc) at high microwave frequencies, techniques to counter the Miller effect (i.e. the feed-back capacitance C_μ transforming into $C'_{be} = C_\mu * (1 - A_v)$, see Figure 2.4, lowering the input impedance of the active device) is needed. The most common approach to handle this problem is the cascode, i.e. two stacked transistors with the lower in common emitter (CE) and the upper in common base (CB) configuration. Since the upper transistor presents a load of $1/g_m$, where g_m is the transconductance of the upper transistor and is given by $g_m = (q/kT) * I_{CQ}$, the voltage gain of the input (lower) transistor is $A_v = -g_m * R_c = -g_m * (1/g_m) = -1$. Therefore, the effect of the feedback capacitor is minimized and contributes only $C'_{be} = 2 * C_\mu$ to the total input capacitance $C_\pi + C'_{be}$ making the topology suitable for high frequency usage. Since the transistors are stacked they share DC current. A further advantage of the cascode is increased reverse isolation (S_{12}) making the circuit extremely stable, especially if used with inductive collector loading to kill the low frequency gain. On the downside, the stacked transistors reduces the available voltage headroom (the DC voltage is typically quite low, < 3 V, at higher RF frequencies) and also increases the noise factor of the circuit.

A differential cascode common emitter amplifier configuration was chosen for the LNA in the receiver. To achieve the necessary gain, the LNA consists of two cascode stages and one standard differential stage in cascade, see Figure 3.4. Since the output of the LNA is directly coupled to the emitters of the mixer transistors, there is already a cascode action (i.e. almost no voltage gain at the input transistor) in place and a standard differential pair is therefore sufficient. It was shown through simulations that the conversion gain was higher for a LNA-Mixer conjugate match compared to a using the cascode effect (i.e. the resulting Miller effect was not limiting the amplifier

gain), and so the DC blocking inductors and AC coupling capacitors in the LNA were sized for a conjugate match. The reduced input impedance of the transconductor stage (from the increased input capacitance) also affects the sizing of the DC blocking inductor in the second amplifier stage so as to maintain a good interstage match.

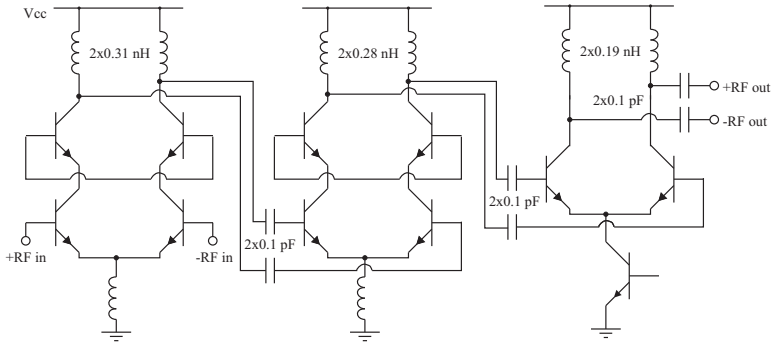


Figure 3.4: LNA simplified schematic

The input stage must have the lowest possible noise figure while having enough gain to suppress the noise contribution from following stages. This was achieved by using fairly large (15 μm) transistors to reduce base thermal noise and a low bias current (6 mA in total, i.e. 3 mA per transistor branch) to minimize shot noise. The second stage is identical to the first, with the exception of using a smaller DC feed inductor (2x0.28 nH compared to 2x0.31 nH) for matching purpose. The third, transconductance, stage uses 20 μm transistors and a large DC current to increase linearity and maximum output power, and a small (2x0.19 nH) inductor for matching purposes. All AC coupling capacitors are 2x0.1 pF.

Since no external image-reject filters are needed between the mixer and LNA in a direct conversion receiver, the impedance levels can be chosen arbitrarily. To maximize the RF currents into the mixer, the LNA output was chosen to be the conjugate of the mixer input impedance. To reduce inductor-inductor coupling and to reduce space consumption, the second stage is flipped upside down, see Figure 3.5. This was possible by not using any emitter degeneration, since that inductor would be extremely close to the biasing inductor of the same stage as well as the DC feed inductors of the adjacent stages. The achieved linearity of the amplifier is reasonable, as shown in Figure 3.6, even without degeneration.

The small signal gain shown in Figure 3.6 was measured on-chip using

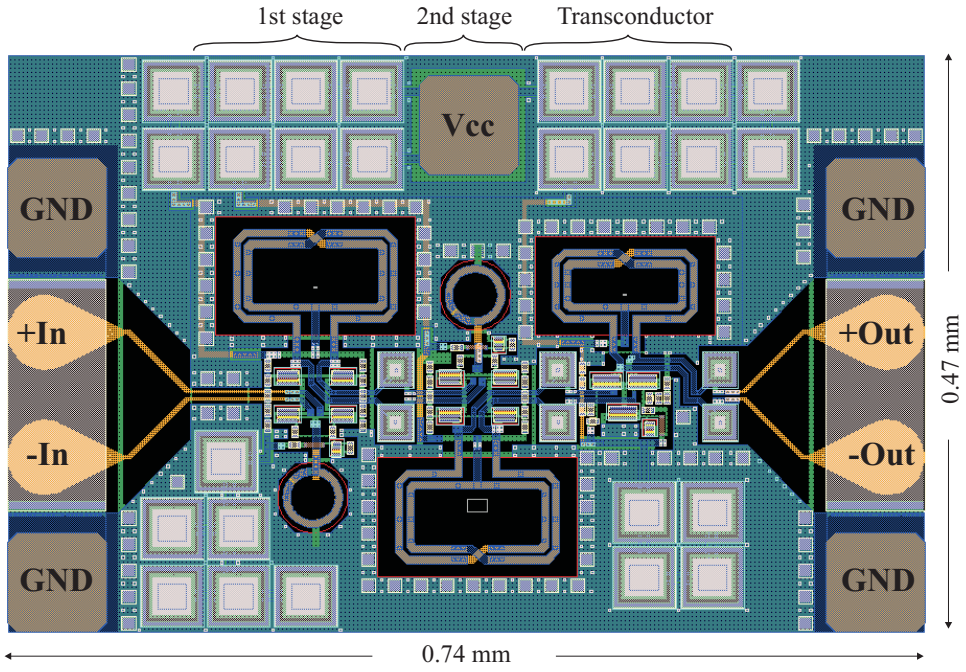


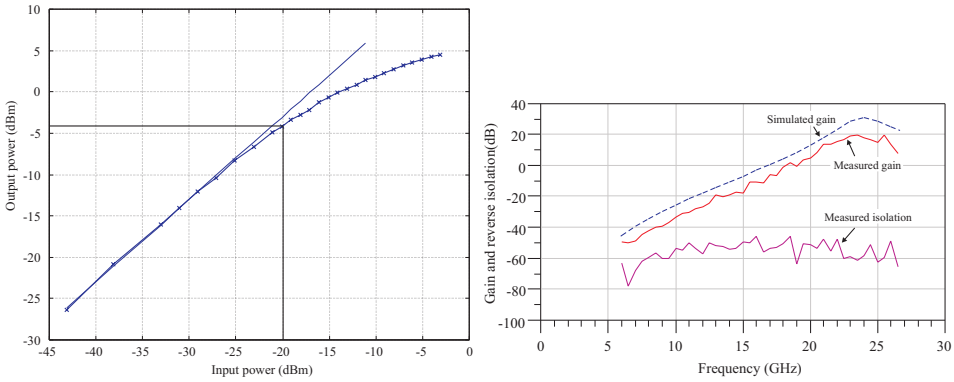
Figure 3.5: LNA Layout

a network analyzer calibrated with an on-wafer calibration kit. The gain curve is identical to simulations except for a reduction in amplitude. This is expected since the simulations use almost ideal inductors, thus predicting a rather optimistic gain of more than 30 dB. The LNA output was matched to the mixer input and so the on-chip gain is expected to be higher compared to measurements.

A reverse isolation (S_{12}) of 50 dB was measured over the entire frequency range 6-26.5 GHz, implying that despite the compact layout (particularly the dense inductor placement) coupling from layout effects are minimal.

The noise figure was measured using a spectrum analyzer, see Section A.1.1.

Important measured characteristics are shown in Table 3.1. The noise figure is given at 24 GHz and was measured with a 100 Ω source impedance. This impedance does not give the lowest possible noise figure, as 100 Ω is relatively far from Γ_{opt} shown in Figure 3.7. It is estimated from simulations that a less than 0.5 dB improvement can be achieved be proper input matching.



(a) 1 dB compression point (b) Gain and isolation

Figure 3.6: LNA linearity, gain and reverse isolation

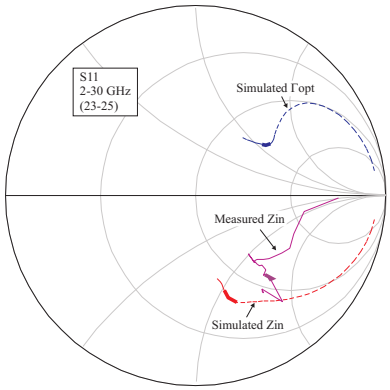
DC Power	73 mA @ 3 V
Gain @ 100Ω	17 dB
Isolation	50 dB
$P_{1dB,in}$	-20 dBm
$P_{1dB,out}$	-4 dBm
3dB gain bandwidth	4 GHz
NF @ 100Ω	6 dB

Table 3.1: LNA measured characteristics

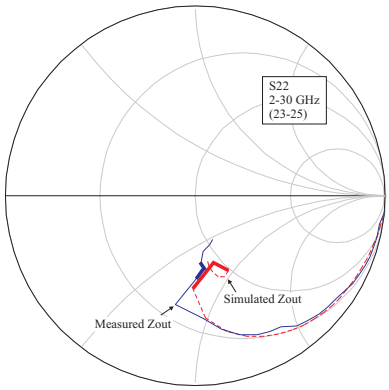
3.0.6 Voltage Controlled Oscillator (VCO)

Frequency translation, i.e. up- and down-conversion, of the information carrying signal is performed in the transceiver by multiplying (using mixers) the signal with a high-frequency carrier. The carrier is generated by a local oscillator (LO) whose frequency is determined by a DC voltage, forming a voltage controlled oscillator (VCO).

An oscillator generally consists of a frequency selective network, or resonator, connected to an amplifier that compensates for losses in the resonator. Most oscillators can be analyzed using either of two models - the feedback type (or "two port") or negative resistance type (or "one port"), see Figure 3.8. In the feedback type, oscillation occurs if the loop gain of the amplifier-resonator is equal to unity and the total phase shift around the loop is zero (the so called Barkhausen's critera). For the negative resistance type, the resonator can, for a narrow frequency band, be modelled as a parallel R_pLC-network and if the active circuit provides an impedance



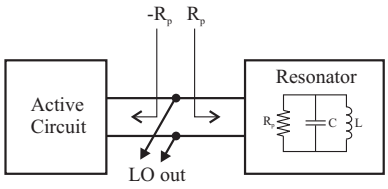
(a) Input impedance and gamma optimum



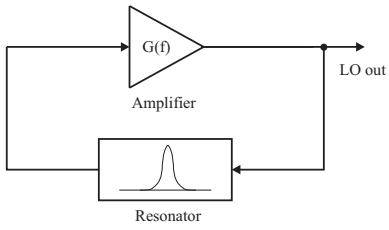
(b) Output impedance

Figure 3.7: LNA input, output and optimum source impedance for lowest noise figure

equal to $-R_p$, oscillation is achieved at the resonant frequency determined by LC as given by $f_{res} = \frac{1}{2\pi\sqrt{LC}}$.



(a) One port type



(b) Two port type

Figure 3.8: One and two port view of oscillators

If the inductor is the limiting component in terms of the quality factor Q (which is always true for on-chip resonators), where Q is defined as $Q_s = j\omega L/R_s$ for a series R equivalent circuit or $Q_p = R_p/j\omega L$ for a parallel R equivalent circuit, it is desirable to have a large L in the resonator tank to maximize the voltage swing. This is understood from noting that $R_p \approx Q_s^2 R_s = (\omega L)^2/R_s$ and since L and R_s scales proportionally with size, a large L gives a large R_p and hence a large voltage swing. The inductor size is limited by the self-resonance frequency and by the fact that a large L means a low C (for a constant oscillation frequency) and so the tuning range becomes limited.

Besides output power, the oscillators phase noise is an important figure of merit. Defined as the noise power within a unit bandwidth, at a certain frequency offset $\Delta\omega$ from the carrier ω_0, relative to the signal power, it quantifies how large the signal "skirts" are. Phase noise comes both from noise on the VCOs control terminal, from white (thermal and shot) noise at the carrier frequency, and from up-converted low-frequency (1/f) noise in the active devices. An often cited equation for describing phase noise (PN) is Leeson's formula [30]:

$$PN(\Delta\omega) = 10\log\left[\frac{2FkT}{P_{sig}}\left(1+(\frac{\omega_0}{2Q\Delta\omega})^2\right)\left(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\right)\right] \tag{3.2}$$

Although the formula contains terms that gives the measured $(1/f^3)$ (up-converted 1/f noise), $(1/f^2)$ (from white noise) and the broad-band noise floor components of real oscillators, it contains the empirical fitting parameter F (determined from measurements) making the formula less suited for predicting phase noise in the design phase. Furthermore, the formula gives the boundary between $1/(\Delta\omega)^2$ and $1/|\Delta\omega|^3$ regions to be precisely equal to the $1/f$ corner of the device, which is contradicted by measurements [31]. However, the formula is useful for the qualitative information that increasing the resonator Q and signal amplitude reduces the phase noise.
Concerning phase noise induced by noise on the VCOs control terminal, it can easily be shown [11] that only low frequency signals affects the oscillation frequency. If V_{cont} is applied at the control terminal, the oscillation frequency is given by $\omega_{out} = \omega_0 + K_{VCO}V_{cont}$ where ω_0 is the zero control voltage frequency and K_{VCO} is the "gain" (in rad/s/V) of the VCO. Since phase is the integral of frequency with respect to time, the VCO output signal is given by

$$v_{out}(t) = A\cos\left(\omega_0 t + K_{VCO}\int_{-\infty}^{t} V_{cont}\,dt\right) \tag{3.3}$$

For a sinusoidal modulation of the control voltage, $V_{cont} \rightarrow v_{cont}(t) = V_m\cos\omega_m t$, the oscillator output voltage becomes

$$v_{out}(t) = A\cos\left(\omega_0 t + \frac{K_{VCO}}{\omega_m}V_m\sin\omega_m t\right) \tag{3.4}$$

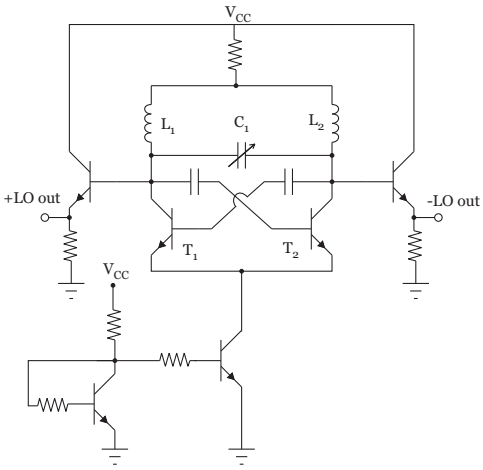
showing that high frequency noise on the control terminal is suppressed by a factor equal to the modulation frequency.

The voltage controlled oscillator (VCO) implemented in this thesis was designed using a negative-g_m oscillator topology, see Figure 3.9. It consists

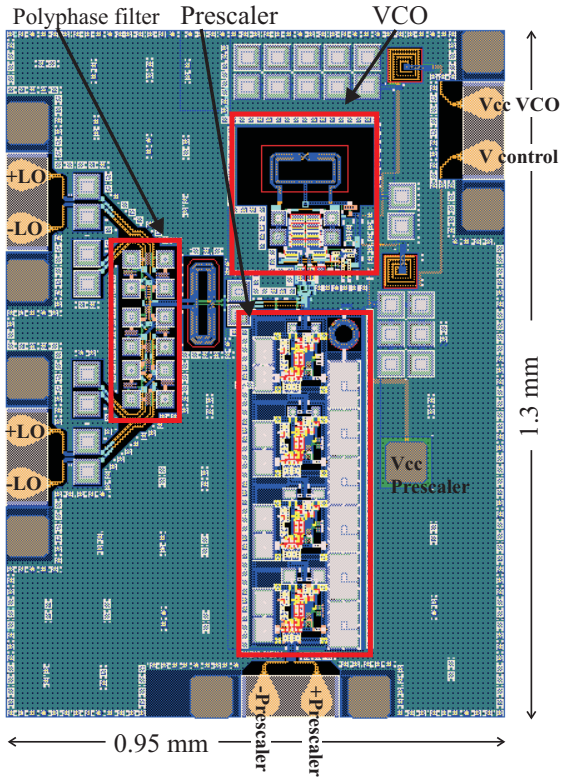
of an on-chip LC-tank and a cross-coupled pair of transistors, T1 and T2, which compensates for the losses in the tank. The tank inductances L1 and L2 (approximately 2x0.3 nH) are implemented as a differential inductor to increase the Q-value and hence reduce phase-noise. The capacitance is provided partly by the parasitic base-collector capacitance of the amplifying transistors and partly by a varactor. The varactor is realized by reverse biasing the emitter-base junctions of 2x4 NPN-transistors connected in parallel (for maximum Q due to reduction of base resistance), see Section 2.2.1, making the depletion zone acting as a tunable capacitor. To further increase the circuit Q-value, two 0.1 pF series back-to-back (for symmetry reasons) capacitors are connected in parallel with the varactor. These are not shown in Figure 3.9.

The output of the VCO core is connected to buffer amplifiers (emitter-followers) to reduce oscillator frequency pulling and increase the output power capability. Since the VCO is loaded with a low impedance (i.e. the inputs of the polyphase filter and prescaler), the buffer amplifiers needs to be able to deliver large currents to sustain the output voltage. To this end, 20 μm transistors with $I_{CQ} = 15$ mA were used as buffers. The differential output impedance of the buffer amplifers were simulated to $Z_{out} = 10.3 - j9.5\Omega$, indicating a lower limit of suitable load impedances. The DC potential at the buffer transistor bases has been lowered to increase U_{CEQ}, which increases the output linearity, by interposing a resistor R to Vcc. Since the thermal noise from this resistor is in common mode it does not increase the total noise level. Not included in the shown schematic is a resistive voltage divider setting the base voltages.

The operating principle of this circuit is easily understood by using the concept of negative resistance. The collector of T1 is connected to the base of T2, and vice versa. By applying a differential voltage at the collectors T1-T2, the potential at T2:s base is raised and the potential at T1:s base is reduced. This leads to an increase of current at T2:s collector and a reduction of current at T1:s collector. Or simply stated, by increasing the voltage the current reduces, hence there is a negative resistance (theoretically $Z_{in} = -\frac{2}{g_m}$) between the collectors of T1 and T2. This negative resistance is connected to the real resistance R_p in the LC resonator tank and if $|Z_{in}| > R_p$ the oscillating condition is fulfilled at the resonant frequency $f_{res} = \frac{1}{2\pi\sqrt{LC}}$. Simulated small-signal Z_{in} of the cross-coupled transistor in this VCO was -27-j40 Ω @ 12 GHz (compared to -5-j33 Ω @ 24 GHz), with a resonator tank impedance of 17+j79 Ω (the varactor impedance was 10-j128 @ 1 V reverse bias). The extra capacitance needed for resonance is provided



(a) Schematic of VCO



(b) Layout of VCO

Figure 3.9: Schematic and layout of manufactured 12 GHz Voltage Controlled Oscillator, with polyphase filter and 1/16 prescaler included in layout

by the buffer amplifiers.

The output power was measured through the polyphase filter and with the prescaler active to simulate the loading conditions when the VCO is integrated in the receiver. Compensating for losses in cables, balun and polyphase filter, the output power is estimated to 0 dBm over the oscillating frequency range of 11.8-12.6 GHz. Measured phase noise is below -95 dBc @ 1MHz offset above 12.1 GHz, see Figure 3.10, with increasing phase noise as the reverse bias is reduced (i.e. higher phase noise for lower frequencies). It is believed that the measured phase noise is dominated by low frequency noise pick-up by the voltage probe, which explains the improvement when the probe was removed (measured at the same frequency). Important measured characteristics are shown in Table 3.2.

As the input impedance of the polyphase filter is low (and capacitive), a parallel 2x0.28 nH differential inductor was interposed between the VCO output and filter input. This increases the output voltage of the VCO and also increases the VCO output linearity.

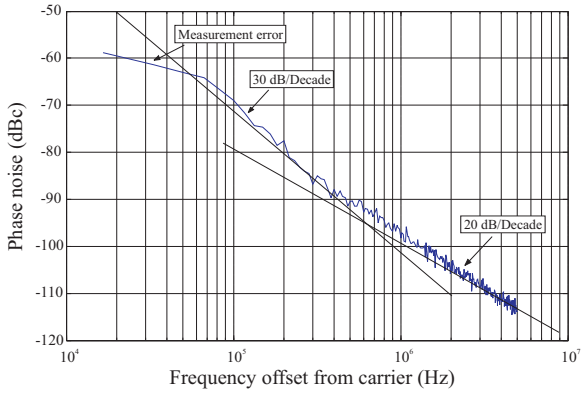


Figure 3.10: Measured close-in phase noise of the VCO

3.0.7 Polyphase filter

The four necessary LO phases for the I and Q mixers are generated by a RC polyphase filter [16] with two parallel sections. One section contains an even number of poles (=two) and the other section an odd number of poles (=one) to ensure a 45° shift between the different mixers and a 90° shift between the two switching sections of each mixer, see Figure 3.12.

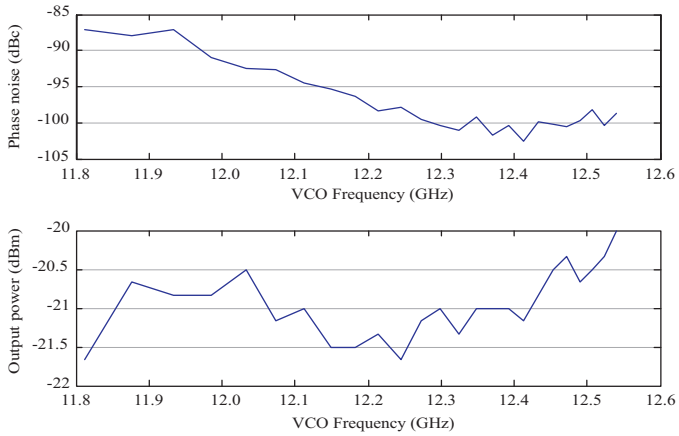


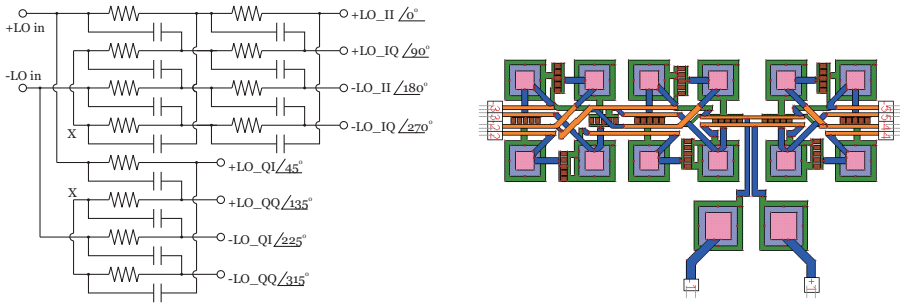
Figure 3.11: Measured output power (bottom) and phase noise at 1 MHz offset from carrier (top) of VCO

DC Power	36 mA @ 3 V
Output Power	0 dBm
Phase noise @ 1 MHz	-95 dBc
Tuning range	11.8 - 12.6 GHz
Output impedance @ 12 GHz	10.3-j9.5 Ω

Table 3.2: VCO characteristics

A polyphase filter has only two degrees of freedom - the number of poles and the impedance level. More poles ensures a higher frequency bandwidth within which the output phases are correct, but more poles also means higher signal attenuation. There is therefore a trade off between bandwidth and attenuation. Also, more poles implies a physically larger structure which consumes more silicon area (higher cost) and more importantly introduces more parasitic inductance distributed over the entire network. The minimum number, one and two poles, were selected in this work since the relative bandwidth of the 24 GHz band is narrow ($< 1\%$), since the gain of the active devices is limited at 12 GHz and so the excessive attenuation would necessitate an extra amplifier stage in the LO pump amplifiers resulting in higher power and area consumption, and since at 12 GHz the interconnect inductance is troublesome enough for one and two poles.

The design frequency of the filter (i.e. where the output phases differs by 45°) is determined by $f = 1/2\pi RC$. For a given frequency it is therefore pos-



(a) Schematic

(b) Simulation layout model

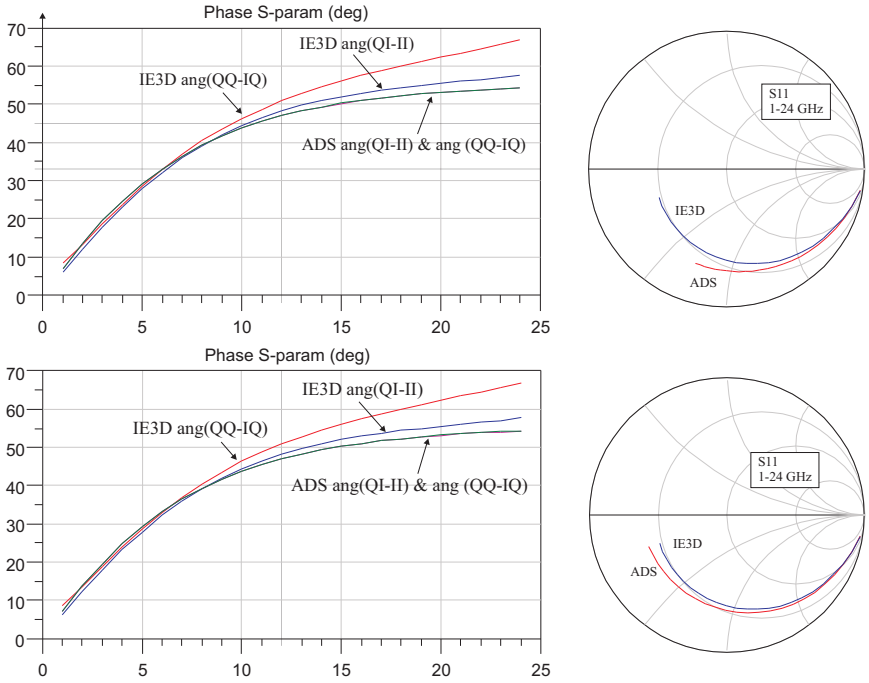
Figure 3.12: Schematic of polyphase filter and layout model for IE3D simulations

sible to select either a high or low impedance level of the circuit. The proper selection is determined by the load and preceding (drive) circuits connected, which have conflicting needs (implying another trade off). A high impedance does not load the driving circuit (i.e. the VCO) substantially meaning that the output voltage and linearity (since the LO output is current limited) will improve with increasing impedance. On the other hand, the filter must be loaded by an impedance higher than its output impedance to avoid excessive voltage attenuation. Since the load of the filter (the input impedance of the buffer amplifiers) is quite small at 12 GHz ($Z_{in,LOpump} = 25 - j53\Omega$), the values $R = 50\Omega$ and $C = 0.25pF (\rightarrow X = -53\Omega$ at 12 GHz) were selected to give an operating frequency slightly above 12 GHz, an input impedance of $Z_{in,PF} = 19 - j22\Omega$ and an output impedance of $Z_{out,PF} = 40 - j20\Omega$. The low input impedance stems from the parallel connection of the two sections.

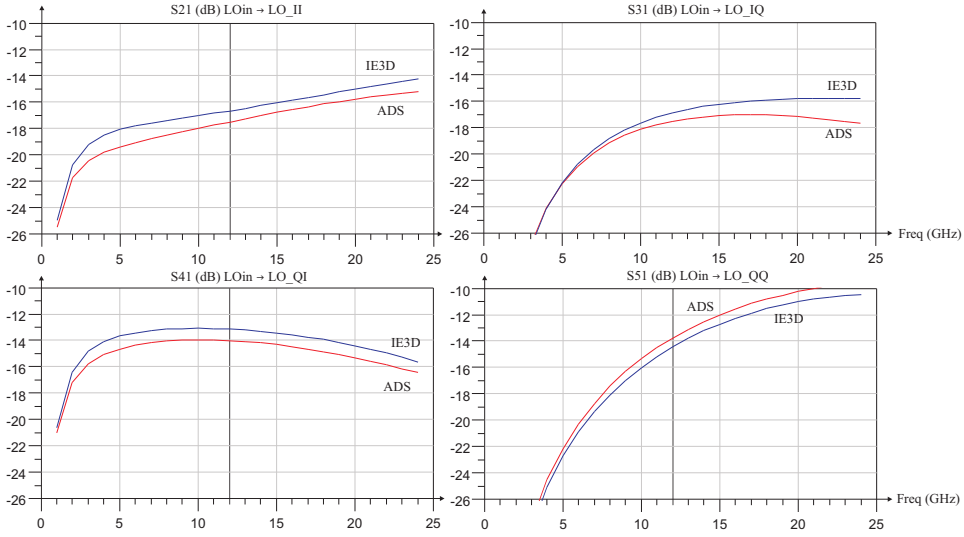
Since the complete polyphase filter contains a lot of interconnect lines with different lengths, an EM-simulation of the complete layout was conducted in IE3D (see Figure 3.12) to investigate if any effects on the phase and/or amplitude balance was to be expected.

A minor difference ($<$ 2 dB worst case) in amplitude attenuation compared to the schematic simulations (using the models of capacitors and resistors from the design kit) could be seen. From the LO input impedance of the polyphase filter, shown in Figure 3.13 it is clear that the main difference comes from the distributed inductance included in the EM simulation.

To increase the accuracy of the schematic simulations without the increased complexity of including small inductances between all components, all stray inductance was lumped together into two (one per terminal) inductances of 0.085 nH each, improving the simulation accuracy.



(a) LO input impedance (right) and output phase differences (left) of filter, without inductors in schematic (top) and including inductors (bottom)

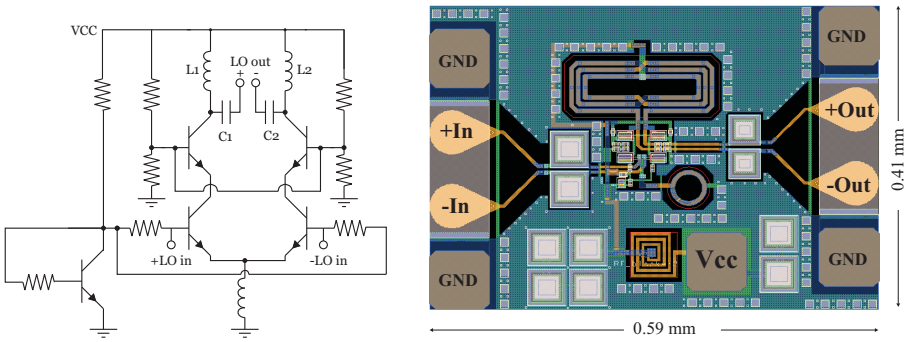


(b) Filter amplitude attenuation from EM and schematic simulation, including lumped 2x0.085 nH inductances in schematics

Figure 3.13: Simulations of polyphase filter with and without lumped 2x0.085 nH inductances in schematic

3.0.8 LO Pump Amplifiers

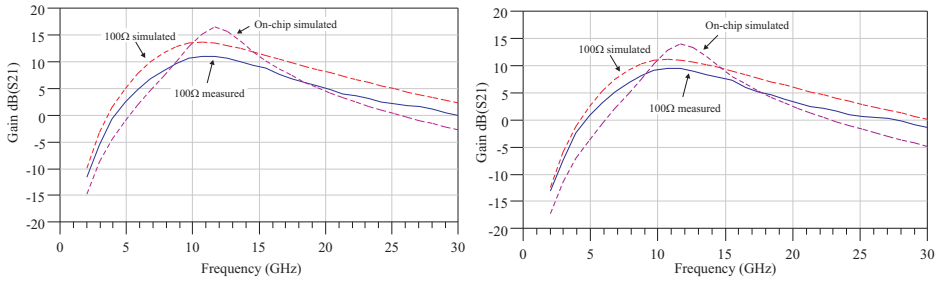
Due to losses in the polyphase filter, the LO signal must be amplified before connected to the switching sections of the mixer cores. Also, as the number of poles for the polyphase filter are different for the I- and Q mixers, the LO signals are unevenly attenuated and needs different amplification. The amplifiers have been implemented in a differential cascode configuration, see Figure 3.14, with a differential inductor as collector loading (L_1 and L_2, 2x0.77 nH differentially) which together with capacitors C_1 and C_2 provides a conjugate match to the LO input impedance of the mixer cores for maximum LO voltage swing. At lower frequencies, it is common to use limiting circuits (e.g. amplifiers driven until the output signal waveform is clipping) to ensure equal LO drive levels of both mixers (or both LO ports of each mixers). At 24 GHz however, this is not possible since the gain of the active devices are limited at the LO frequency harmonics that would constitute the output waveform.



(a) Schematic (b) Layout

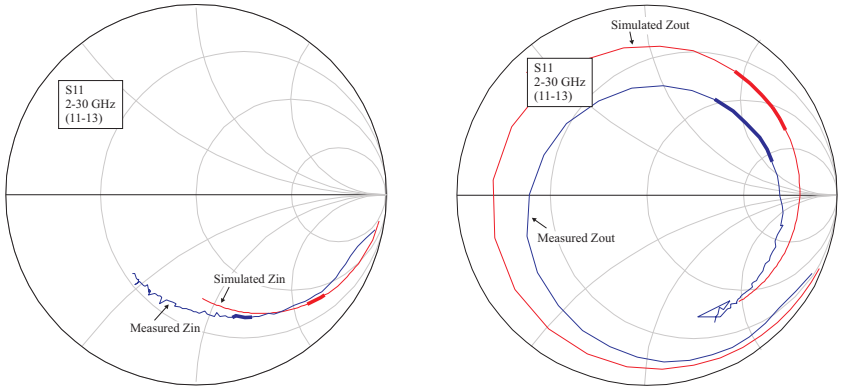
Figure 3.14: Schematic and layout of LO pump amplifier

By using different collector currents for the different amplifiers, the gain was set so as to compensate for the different losses in the one and two pole signal paths in the polyphase filter. Measured gain of the amplifiers was 9.8 dB (20.4 mA) and 8.0 dB (13.5 mA) respectively at 12 GHz in a 100Ω environment, which was lower than simulations (13.3 dB and 10.9 dB at 100Ω, rising to 16 dB and 13.5 dB in an on-chip environment) as indicated in Figure 3.15. Since the measured curves are identical in shape to the simulations (except for the 3.5 dB and 2.9 dB gain reduction), it is believed that the deviation is caused by unaccounted losses - partly from interconnect lines and partly by the inductor having a lower Q than expected.



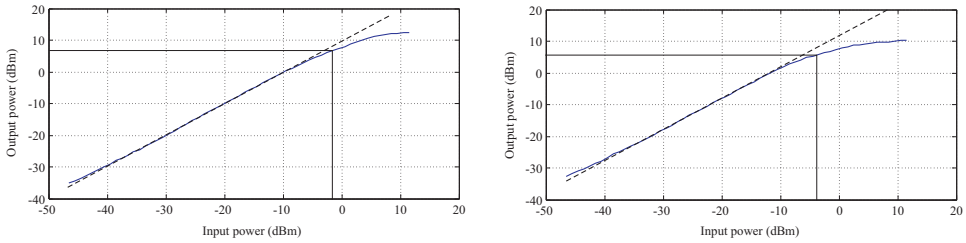
(a) Gain of high current amplifier (b) Gain of low current amplifier

Figure 3.15: Gain measurement and simulation of LO pump amplifiers



(a) Input impedance (b) Output impedance

Figure 3.16: Impedances of high current LO pump amplifier



(a) High current amplifier (b) Low current amplifier

Figure 3.17: Measured 1dB compression points of LO pump amplifiers

3.0.9 Subharmonic Down-conversion Mixers

The I and Q mixers used in the receiver are double-balanced active mixers (also known as Gilbert cells). Although passive mixers, using diodes instead

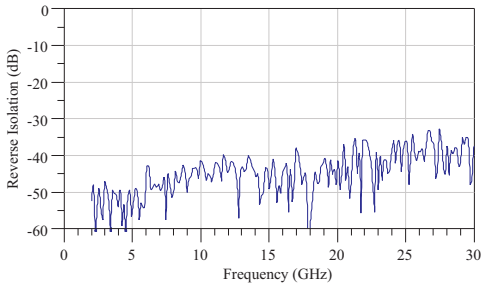


Figure 3.18: Measured reverse isolation (S12) of LO pump amplifers

DC Power	20.4 mA @ 3 V	13.5 mA @ 3V
Gain @ 100Ω	9.8 dB	8.0 dB
Reverse isolation	< 35 dB	< 35 dB
$P_{1dB,out}$	7 dBm	6 dBm

Table 3.3: LO pump amplifiers measured characteristics

of transistors, exhibit higher linearity and typically lower noise figure compared to active mixers, the importance of having a combined gain from the LNA and mixer, which must be sufficient to overcome $1/f$ and thermal noise in the baseband stages, rules out lossy passive mixers in direct conversion receivers.

Mixing action in general can be understood by noting that multiplication of two sine-waves produces sum and difference frequencies, where the unwanted term is filtered out. For a down-converter, the difference term is used; for the up-converter the sum term is used. The mixing principle of a Gilbert cell is based on the so called controlled transconductance mixer [16], see Figure 3.19. For a down-conversion application, the information carrying high frequency (RF) signal is applied as a voltage that modulates the current source (where di/dv is called the transconductance g_m) with quiescent current $2I_0 = I_1 + I_2$. First, assuming no v_{RF} signal, the current is divided up in the currents I_1 and I_2 depending on the applied voltage v_{LO} through

$$I_1 = \frac{2I_0}{1 + e^{-V_{LO}/V_T}} \tag{3.5a}$$

and

$$I_2 = \frac{2I_0}{1 + e^{V_{LO}/V_T}} \tag{3.5b}$$

from the exponential voltage to current relation of the bipolar transistor. Here, $v_T = kT/q$ denotes the thermal voltage ($v_T = 26mV$ at room temperature). The differential output current i_0 is then given by

$$i_0 = I_1 - I_2 = 2I_0 \tanh \frac{v_{LO}}{2V_T} \tag{3.6}$$

shown graphically in Figure 3.19. If v_{LO} is small ($<< v_T$), $\tanh \varphi \approx \varphi$ and so the output current i_0 is approximately linearly proportional to v_{LO} (the mixer is said to be working in the "multiplication region")

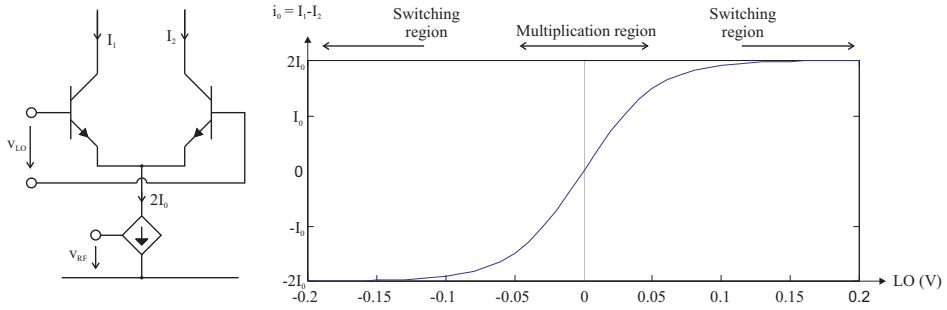


Figure 3.19: Principle of controlled transconductance mixer

$$i_0 \approx I_0 \frac{v_{LO}}{V_T} \tag{3.7}$$

Now, if v_{RF} is a small signal voltage and the transconductance of the current source is g_m, $2I_0$ is replaced by $2I_0 + g_m v_{RF}$ in (3.6) and

$$i_0 \approx (2I_0 + g_m v_{RF}) \frac{v_{LO}}{2V_T} = I_0 \frac{v_{LO}}{V_T} + \frac{g_m v_{RF} v_{LO}}{2V_T} \tag{3.8}$$

where the first term is called LO leakage or feed-through and the second term is the wanted one. The first term can be cancelled by employing a second, identical, circuit, driven by $-v_{LO}$, which output current is

$$i_{02} \approx I_0 \frac{v_{LO}}{V_T} - \frac{g_m v_{RF} v_{LO}}{2V_T} \tag{3.9}$$

and the output current is taken as the difference between i_0 and i_{02}

$$i_{IF} = i_0 - i_{02} \approx \frac{g_m v_{RF} v_{LO}}{V_T} \tag{3.10}$$

The resulting schematic, with BJT:s used as the current sources, is shown in Figure 3.20. The ratio between the low frequency output current (i_{RF}) and the high frequency input voltage (v_{RF}) is called the conversion gain

$$Conv.gain = \frac{i_{IF}}{v_{RF}} \tag{3.11}$$

This current is preferably coupled to a low-impedance amplifier (either a transimpedance or current-current amplifier) before being processed by the A/D-converter.

At microwave frequencies, where power is preferably measured instead of voltages or currents, the following definition is more common

$$Conv.gain = \frac{P_{IF}}{P_{RF}} \tag{3.12}$$

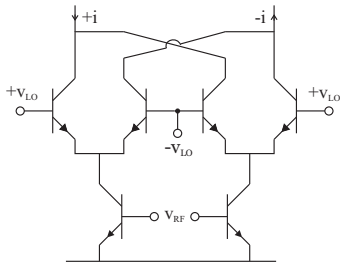


Figure 3.20: Schematic of double-balanced active mixer (Gilbert cell)

The previous calculations have assumed a constant g_m, i.e. a perfectly linear input voltage to current output relation (which is valid for small input signals). For large input signals, the transfer function is given by

$$i_{out} = I_{CQ} \tanh \frac{v_{in}}{2V_T} \tag{3.13}$$

where i_{out} is the differential output current, v_{in} the differential input voltage and I_{CQ} the quiescent current in each branch. g_m is now obtained from di_{out}/dv_{in}

$$g_m = \frac{I_{CQ}}{2V_T} sech^2 \frac{v_{in}}{2V_T} \tag{3.14}$$

Equation 3.14 is illustrated in Figure 3.21, where g_m has been normalized to $I_{CQ}/2V_T$, showing that the transconductance is reduced to less than 50%

of the peak value (for $v_{in} = 0$) at input signals of 50 mV (amplitude). By using several differential pairs in parallel, with different emitter sizes of the transistors, it is possible to obtain a flatter $g_m = g_m(v_{in})$ dependence (from the so called "multi-tanh principle" [32]). This however also increases the noise figure of the circuit due to the larger transistor count. Other means to increase the linearity is to use emitter degeneration of the differential pair. In some cases, linearity can be limited by saturation of the switching quad. This problem can be reduced by using inductive collector loading (at least for the up-conversion) instead of resistive to enable larger voltage swings.

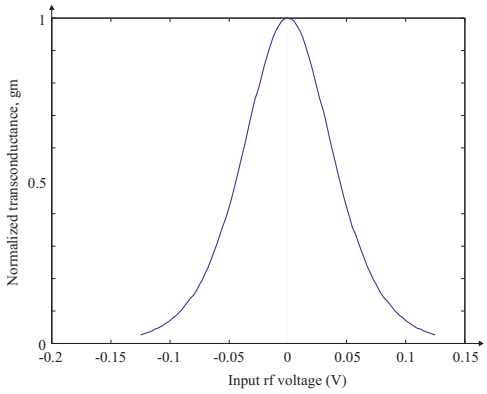


Figure 3.21: Transconductance g_m of RF input stage for large signals

Ideally, Gilbert cells are used as "switching modulators", i.e. v_{LO} is driven as a large square wave hard-switching the LO transistors (switch quad) alternately on and off. The reason for this is to maximize the signal-to-noise ratio at the output (i.e. minimizing the noise figure). It can be shown that the noise behavior of switching modulators are always much better than non-switching (multiplying) types. Although not trivial to derive, it can intuitively be understood from the following: The output signal level is increased with large v_{LO} levels as seen from Eq. (3.10), up to a certain level (about 100 mV peak, see Figure 3.19). At the same time, the noise from the switching transistors are kept to a minimum since half of them are alternately turned off (and are therefore not contributing any noise). At microwave frequencies, and especially when operating close to the transistors f_T (as in this thesis), two problems arises. First, it is not possible to generate a square wave for the LO voltage as the active devices have almost no gain at the necessary harmonics that comprises the square wave. Therefore, a large sine wave is used instead. The amplitude of the sine needs

to be large partly to hard-switch the transistors but also to minimize the rise-time to reach the on-off stages (during which no transistors are off and all transistors are therefore contributing noise). If the LO voltage is made too large, high-current effects in the bases of the BJT:s can actually reduce the switching speed and cause an increase of LO feed-through. Typically 100-300 mV peak is a recommended LO level in the literature [16]. The second problem of operating at high frequencies is that the ∼100-300 mV needs to be applied to the intrinsic base-emitter junction of the active device (the capacitor C_π), so the voltage at the external transistor terminals needs to be much bigger since most of it will be across the base resistance r_b. Because the input impedance of the LO transistors are low, a lot of power needs to be dissipated to obtain the necessary switching voltage level.

The 24 GHz down-conversion mixers used in the receiver are based on a modified Gilbert cell topology [33] with two stacked switching sectors ("three-level multiplier" [34]) pumped with 12 GHz LO signals 90° out of phase. Since the Gilbert cell can be thought of as a multiplying circuit, the subharmonic mixing action can be understood from noting that the extra switching stage adds another LO multiplication term, see Eq. (3.15),

$$v_{IF}(t) = A\cos(\omega_{RF}t+\varphi)\sin(\omega_{LO}t)\cos(\omega_{LO}t) = B\cos(\omega_{RF}t+\varphi)\sin(2\omega_{LO}t) \tag{3.15}$$

meaning that the VCO can operate at half the RF frequency [33]. This has several advantages for the VCO design (see Section 3.0.6), but more importantly for the system level performance (see Section 2.1).

As the voltage headroom for the receiver is limited to 3V, only two transistors can be stacked for optimum high frequency performance. Therefore, the transconductance amplifier (differential pair) that usually forms the bottom of the mixer has been folded and is biased in parallel with the switching stages, see Figure 3.22.

The RF output current of the differential pair is coupled to the emitters of the first switching sector through capacitors C_1 and C_2. The inductors L_1 and L_2, implemented as a differential inductor, are large and acts as current sources for signal frequencies. Inductors L_3 and L_4 (also realized as a differential inductor) and capacitors C_1 and C_2 transforms the low input impedance of the bottom switching section into the conjugate of the output of the transconductor, resulting in higher RF currents and ultimately higher conversion gain. Inductors L_5 and L_6 (one differential inductor) introduces feedback that increases the input impedance and linearity but lowers the

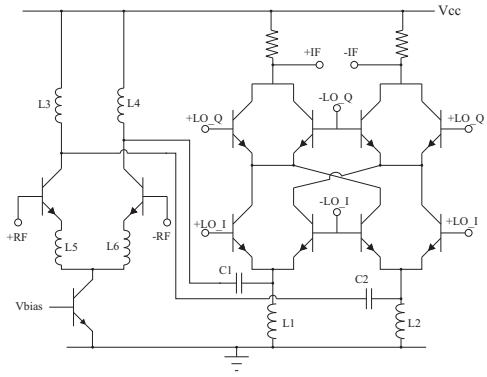


Figure 3.22: Simplified schematic of down-conversion mixer

gain. By choosing emitter lengths of the input transistors and the values of L_5 and L_6, a simultaneous power and noise match at 50 Ohms has been obtained [35].

For the IQ-demodulator, an additional mixer core is connected in parallel sharing the transconductor amplifier with the first mixer core, see Figure 3.23. This significantly reduces the area requirement of the circuit, especially since only two inductors are needed for the transconductor instead of four. Also, the current consumption is reduced compared to having two complete mixers, and the input impedance is twice as high and therefore easier to match. For the complete receiver, the transconductor stage was instead integrated (and slightly modified) as the third stage of the LNA. No stand-alone mixer was manufactured, instead the complete IQ-demodulator has been evaluated.

DC consumption of the complete IQ demodulator was 80 mA at 3 V.

Conversion gain was measured by connecting the baseband output to a two channel low frequency oscilloscope, as described in Appendix A, and is shown in Figure 3.26. The conversion gain shown is using only the I or Q port, when using both channels 3 dB should be added to the conversion gain.

For subharmonic zero-IF receivers another important figure of merit is the "LO rejection (LOR)", defined as [33]:

$$LOR = \frac{\text{Conversion gain at RF frequency}}{\text{Conversion gain at LO frequency}} \tag{3.16}$$

For a fundamental mixing receiver (i.e. not sub-harmonic), the LO and

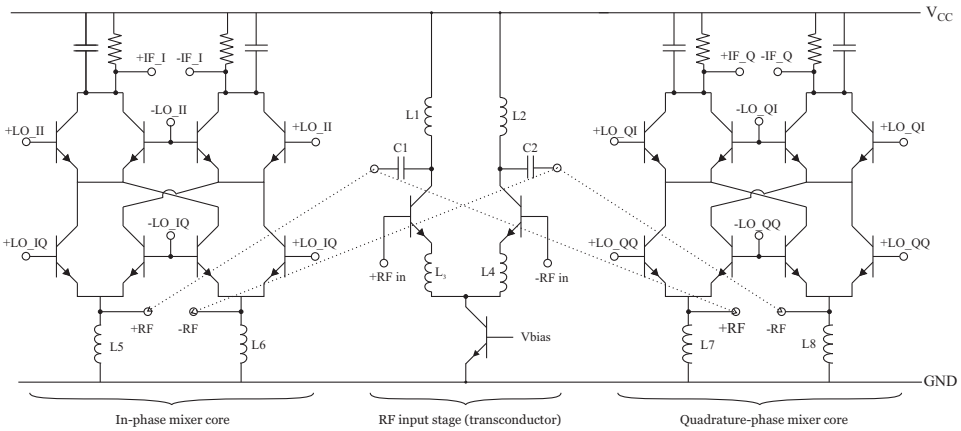


Figure 3.23: Simplified schematic of IQ demodulator

RF frequencies are equal and so LOR is 0 dB. For a sub-harmonic mixer, it is a measure of how well DC offsets are suppressed. Measured LO rejection for the IQ-demodulator was 38.5 dB.

The 1-dB input compression point is shown in Figure 3.27 (only relative output power is shown, i.e. the output 1-dB compression point cannot be estimated from this figure) and is given as -4 dBm. As the input compression point of the LNA is -20 dBm with a (compressed) gain of 16 dB, the IQ demodulator is not the limiting device concerning total system linearity.

Measured conversion gain is fairly constant in the 21-24 GHz frequency range, shown in Figure 3.26, with a gain peak at +3 dBm (external) LO power. This corresponds to a much lower on-chip power level (delivered by an integrated VCO) as the external signal source (100 Ω) is highly missmatched to the input of the polyphase filter (19-j22 Ω).

Due to the high transistor count in the switching sections of the mixer, the noise figure is high. Shown in Figure 3.27 the noise figure is a constant 20 dB from 20-24.5 GHz after which it sharply increases, caused by the reduction of conversion gain after 24.5 GHz.

A 1-pole RC low pass filter has been placed at the output of the down-conversion mixers, with R=$2x110\Omega$ and C=2x1.5 pF, as shown in Figure 3.23. The calculated 3-dB bandwidth is BW=$1/(2\pi RC)$=965 MHz, in perfect agreement with measurements.

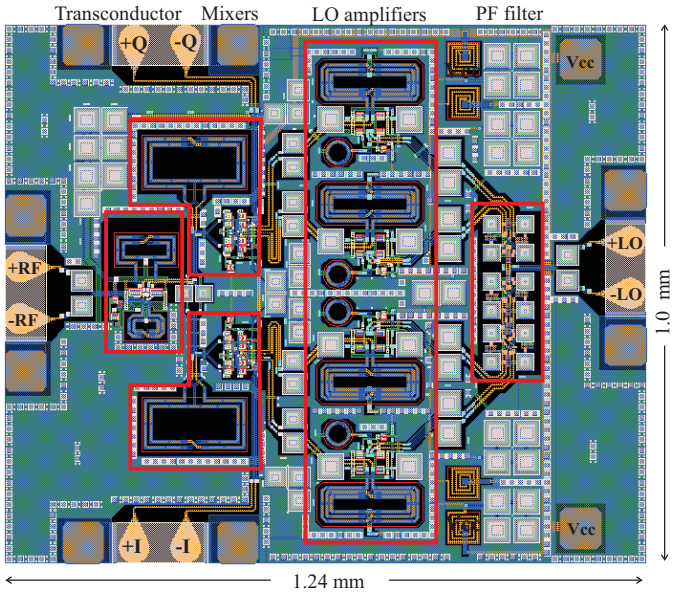
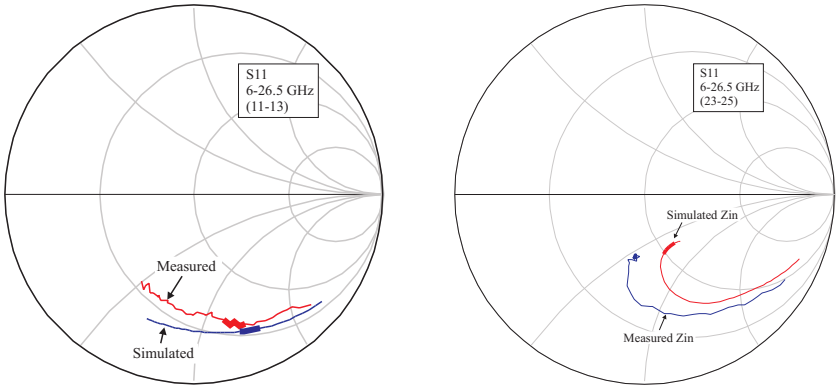


Figure 3.24: Layout of IQ demodulator

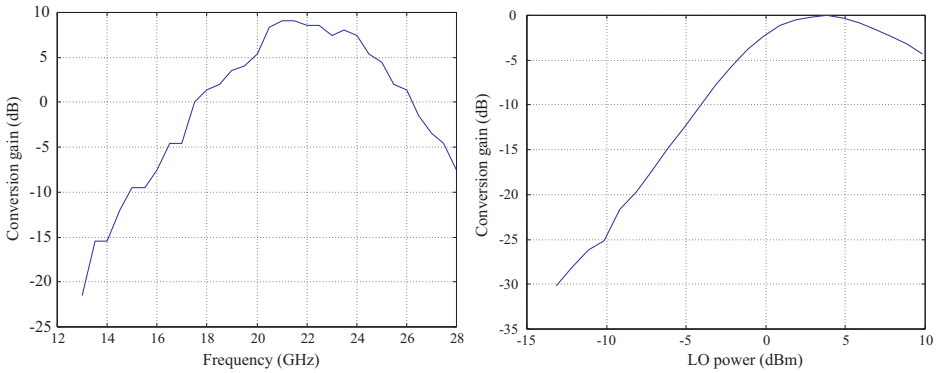


(a) LO port (b) RF port

Figure 3.25: Measured and simulated input impedance of IQ demodulator

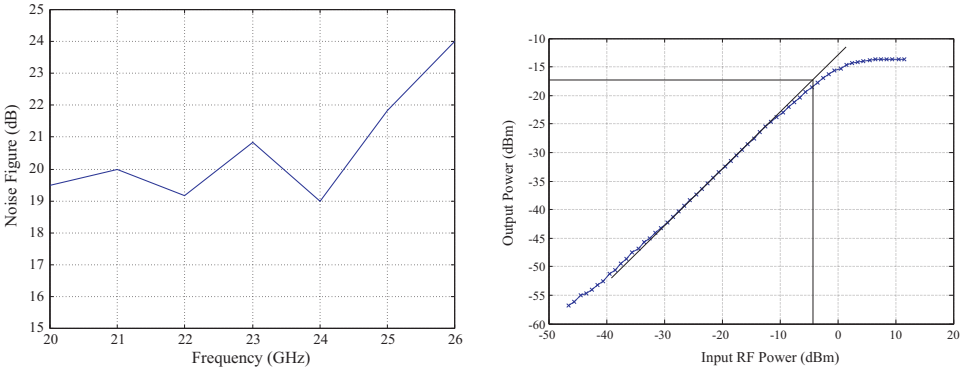
3.0.10 Subharmonic Up-conversion Mixers

The down-conversion mixer cores can not be used for up-conversion since the input signal is capacitively coupled from the transconductor to the switching stages, which of course is not possible for baseband signals. Instead, an



(a) Conversion gain vs frequency (b) Conversion gain vs LO power

Figure 3.26: Conversion gain and normalized conversion gain as a function on LO power of IQ demodulator



(a) Noise Figure (b) Linearity

Figure 3.27: Measured noise figure and linearity of IQ-demodulator

DC Power	80 mA @ 3 V
Conversion gain @ $1M\Omega$	7 dB
Noise figure @ 100Ω	20 dB
$P_{1dB,in}$	-4 dBm
LO rejection	38.5 dB

Table 3.4: IQ demodulator measured characteristics

alternative topology, shown in Figure 3.28, has been used where the mixer has been folded between the switching stages. At the folding junction, the

baseband signal has been translated to the "intermediate" frequency 12 GHz which is easily AC coupled to the next switching section. Again, the inductors and capacitors have been selected to provide a conjugate match for maximum RF current amplitudes. The up-conversion mixers were included in an IQ modulator, shown in Figure 3.30. The layout is similar to the IQ demodulator in Section 3.0.9 with the exception of the mixer cores being replaced. No stand-alone up-conversion mixer was manufactured, instead the complete IQ modulator (also known as vector or quadrature modulator) was evaluated.

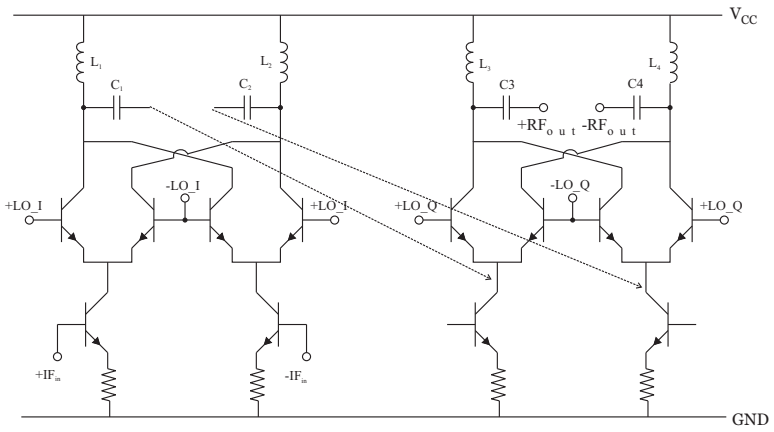
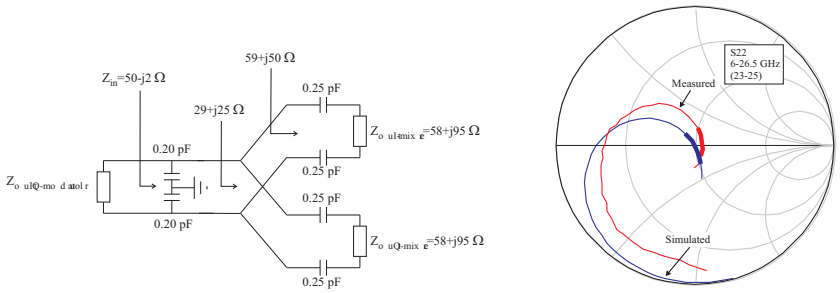


Figure 3.28: Simplified schematic of up-conversion mixer

Because the power amplifier (PA) used for the transmitter was designed by a research group at Ulm, Germany (i.e. not in-house at Uppsala University) [36], the IQ modulator was designed for use in a standard 50 Ω environment. This also makes the circuit applicable for use in other transceiver systems. The output impedance was matched to 50 Ω by selection of signal coupling capacitors and using two small capacitors in parallel, as shown in Figure 3.29.

The measured output power of the mixers is shown in Figure 3.32 for DC power levels of 2.5-4 V, with only one port fed with baseband signal. Maximum output power of each sideband was -18 dBm, expected to increase by 6 dB to -12 dBm when feeding both I and Q ports (ideally removing one sideband). No substantial increase of maximum output power level or linearity was achieved by increasing the DC voltage to 3.5 V, and using 4.0 V even degraded performance. The carrier rejection was $>$ 28 dB ($>$ 31 dB 12



(a) Matching network (b) Output impedance

Figure 3.29: Matching network and output impedance of RF output of IQ modulator

DC Power	107 mA @ 3 V
Output Power	-12 dBm
Carrier suppression	$>$ 28 dB
LO suppression	$>$ 31 dB
Output noise	$<$ 150 dBm/Hz

Table 3.5: IQ modulator measured characteristics

GHz LO rejection) as shown in Figure 3.31 together with the uncalibrated output noise floor close to the carrier. To suppress the noise figure of the spectrum analyzer, the RF output was amplified using a K-band LNA ($>$ 30 dB gain and $<$ 3 dB noise factor). The spectrum analyzer noise was still dominant, with the carrier leakage power preventing the possibility of cascading another LNA, meaning that only an upper bound of the noise floor could be estimated. Measured noise floor was -85 dBm/Hz using a resolution bandwidth (RBW) of 10 kHz, giving an estimated maximum noise floor of -85 dBm/Hz - 10log(10E3 Hz) - 30 dB (LNA gain) + 5 dB (cable losses) = -150 dBm/Hz. A summary of the measured characteristics of the IQ modulator is shown in Tabel 3.5.

3.0.11 Wilkinson coupler

The Wilkinson coupler [37] is a passive three-port component used for equal-phase power division or combining, featuring (ideally) losslessness, high port isolation and the option of non-equal power splits. At microwave frequencies, the coupler is almost exclusively implemented in transmission line form, usually using microstrip or stripline technology [38], see Figure 3.33. Look-

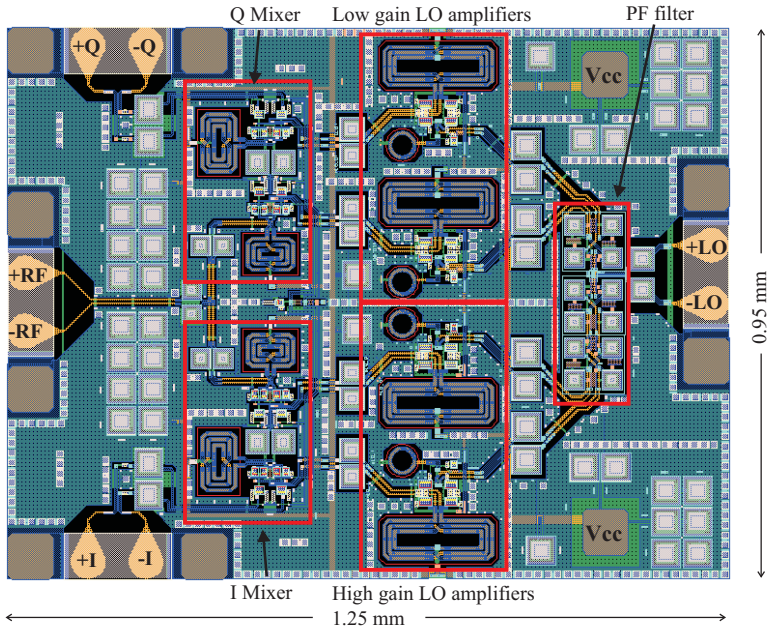
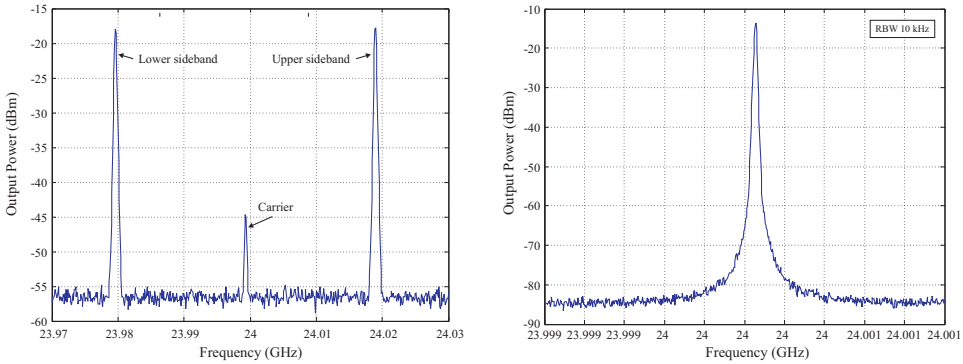


Figure 3.30: Layout of IQ modulator



(a) Carrier suppression (b) Output noise floor

Figure 3.31: Measured output spectrum of IQ modulator

ing into Port 1, the $\lambda/4$ lines transforms the Z_0 impedance at Port 2 and 3 into $2 * Z_0$, which when connected in parallel at Port 1 equals Z_0, resulting in a perfect match. The resistor R together with the quarter wave sections provides isolation between Port 2 and 3 for the odd-mode case, i.e. when

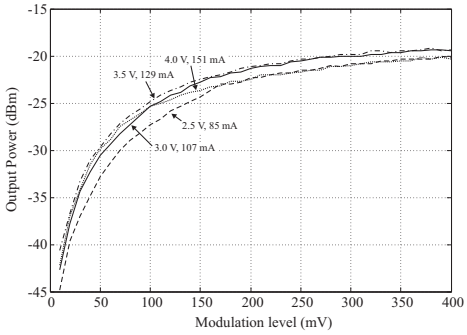
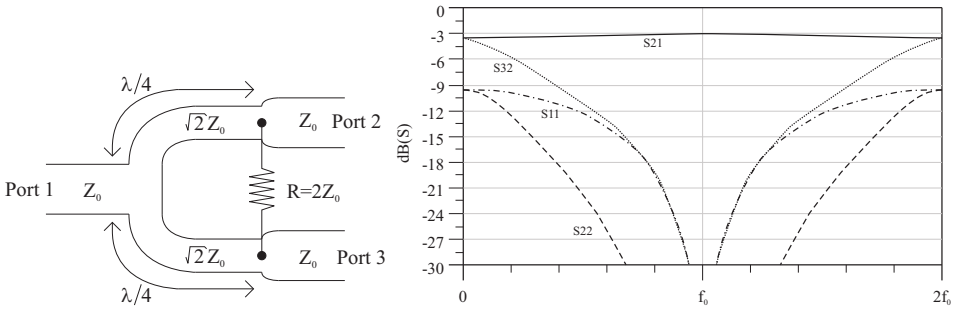


Figure 3.32: Output power level vs baseband modulation level of IQ modulator

unequal signals appear at port 2 and 3. Because of the $\lambda/4$-sections, the behavior of the circuit is periodical in $2f_0$ where f_0 is the design frequency, see Figure 3.33. The circuits frequency sensitivity stems from the use of quarter wave transmission lines; if more bandwidth is needed a quarter wave section with $< Z_0$ can be placed in series with Port 1 and using $Z_0 < Z < \sqrt{2} * Z_0$ lines at Port 2 and Port 3.



(a) Transmission line type Wilkinson coupler

(b) S-parameters of Wilkinson coupler

Figure 3.33: Transmission line type Wilkinson coupler, layout and S-parameters

Since the output impedances of the active devices in the used process are relatively low at 24 GHz, output signals can simply not be connected together without cross coupling and so there is a potential need for on-chip Wilkinson couplers. The transmission line type Wilkinson is not practical

for implementation in the monolithic transceiver due to excessive area requirement. Furthermore, to be compatible with other on-chip circuitry, it needs to be differential.

A transmission line element can, for a narrow band of frequencies, be modeled using inductors and capacitors in a "tee" or "pi" configuration, see Figure 3.34. The pi configuration is usually preferred as it only uses one inductor. The ratio between L and C gives the characteristic impedance Z_0 according to $Z_0 = \sqrt{L/C}$. The absolute values of L and C are dependant on the design frequency and the length (=phase) of the transmission line. For a quarter wavelength long transmission line with characteristic impedance Z_0, the values of L and C are calculated using the formula [39] $Z_0 = j\omega_0 L = 1/(j\omega_0 C)$, where ω_0 is the design frequency (i.e. 24 GHz in this work).

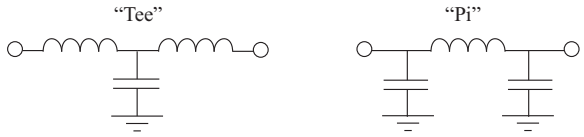
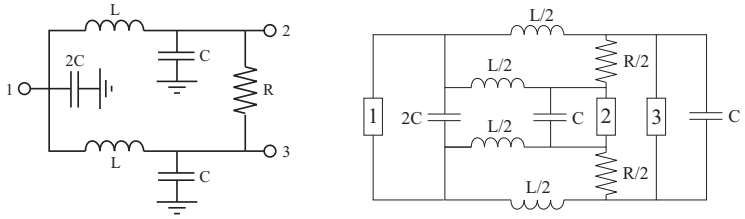


Figure 3.34: Lumped element equivalents of a transmission line segment

By directly replacing the $\lambda/4$-sections in Figure 3.33 with Pi-equivalents from Figure 3.34, the single-ended circuit in Figure 3.35 is obtained. The differential version, using the same characteristic impedance, is also shown.



(a) Single-ended Wilkinson

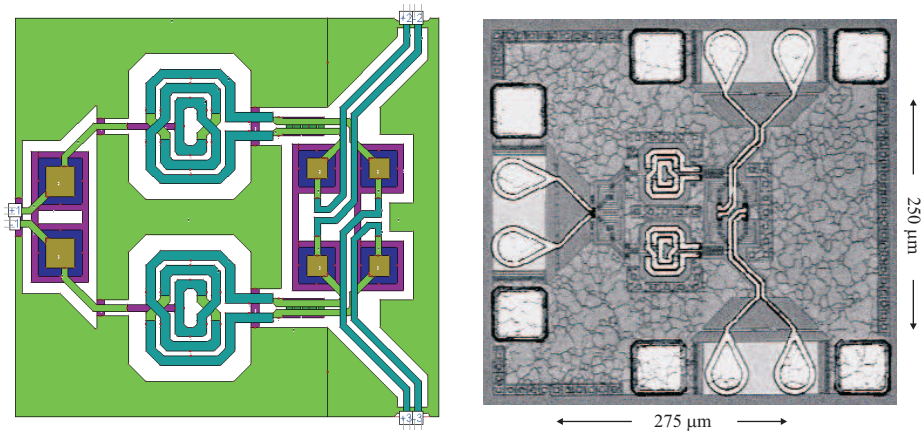
(b) Differential Wilkinson

Figure 3.35: Schematic of single-ended and differential Wilkinson using lumped components

At 24 GHz and $Z_0 = 50$ Ohm, L = 0.47 nH and C = 93.8 fF. The differential design uses four inductors instead of two for the single-ended case,

greatly complicating the layout work and possibly introducing uncontrolled magnetic coupling between the inductors. This problem was solved by using centre-tapped differential inductors [16], pairing the top two inductors together and the lower two together. The differential terminals were connected to R/2 and the single-ended terminals were connected to Port 1. By using inductors with three turns, the centre-tap is located on the opposite side of the differential input, which significantly reduces the lengths of the interconnect lines to Port 1. Since the on-chip capacitors are not fully symmetrical they were replaced by two back-to-back capacitors with twice the capacitance. The double capacitors, due to their larger size, were also easier to realize compared to the 93.8 fF versions.

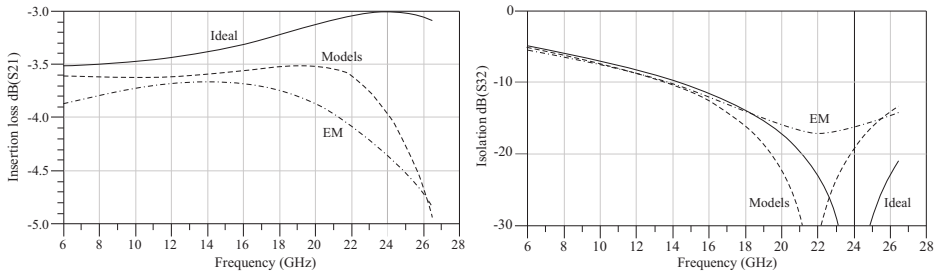
Schematic simulations of the complete circuit was performed in ADS, using models for the capacitors and resistor provided in the design kit and using S-parameters obtained from IE3D for the inductor. To evaluate the effect of layout parasitics, EM simulations of the complete Wilkinson were conducted, see Figure 3.36. As seen in Figure 3.37, the simulated S21 indicates an insertion loss of around 1-1.5 dB below the ideal 3 dB. More seriously, the isolation (see Figure 3.37) between the output ports (S_{32}) is potentially degraded by more than 15 dB due to layout effects not accounted for in the schematic simulations. Input reflections were not substantially affected, as seen in Figure 3.38.



(a) EM model of Wilkinson coupler in IE3D

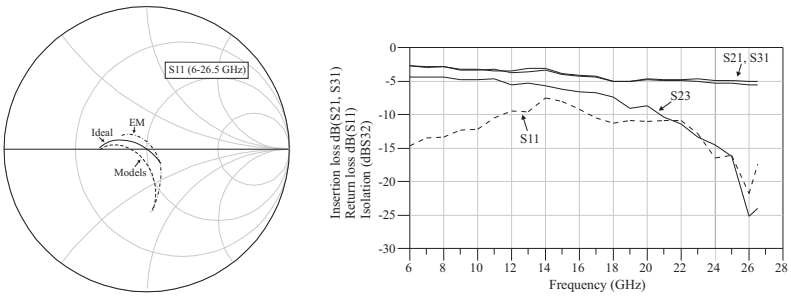
(b) Photograph of manufactured Wilkinson coupler

Figure 3.36: EM model and chip photograph of Wilkinson coupler



(a) Insertion loss S21 (b) Port isolation S32

Figure 3.37: Simulated insertion loss and port isolation of Wilkinson coupler



(a) Simulated input impedance (b) Measured S-parameters

Figure 3.38: S-parameters of Wilkinson coupler

Measured results shows an elevated $f_0 = 26$ GHz compared to the targeted 24 GHz, with isolation S_{23} = - 15 dB and insertion loss $S_{21} \approx -5$ dB at 24 GHz, which is close to simulated values. At 26 GHz the isolation and input return loss reaches a minimum of $< -20dB$. Input return loss S_{11}, S_{22} and S_{33} were all below -15 dB at 24 GHz and so do not contribute significantly to the insertion loss. Total area consumption, without pads, is 0.07 mm^2.

The Wilkinson coupler was designed and evaluated early in the ARTEMIS project for potential inclusion in the transmitter. It was later decided that it would not be included in either the receiver nor transmitter.

Chapter 4

RFIC Systems

Using the components described in Chapter 3, complete receiver and transmitter systems have been designed and manufactured. Although all devices for the transmitter shows satisfactory results, the transmitter is not reported in this thesis due to insufficient measured system performance (likely caused by DC biasing errors).

Two versions of the receiver has been included - with and without integrated VCO. For the version with integrated VCO, an LNA [6] designed by project partner Ulm University, Germany, has been used. For the version without integrated VCO, the LNA reported in this thesis was integrated. Furthermore, the 1/16 frequency divider (or prescaler) used was also developed at Ulm University.

4.0.12 Monolithic Receiver with external LO

A fully differential 24 GHz receiver using an external LO source is shown in Figure 4.1, based on subcomponents reported in Chapter 3. A block schematic of the system is shown in Figure 4.2. The Vcc terminal of each circuit block is connected through a local LC low pass filter before being connected together at the Vcc bond pad to minimize inter-circuit block signal coupling through the Vcc line. This type of coupling is further reduced due to the complete differential topology throughout the system.

The receiver has a higher conversion gain and lower noise figure at 23 GHz instead of the targeted 24 GHz, see Figure 4.3, which is directly related to the higher LNA gain at 23 GHz. This is expected since the noise of the IQ demodulator (NF=20 dB) is not fully suppressed by the LNA. The input compression point was measured to -20 dBm, identical to that of the stand-

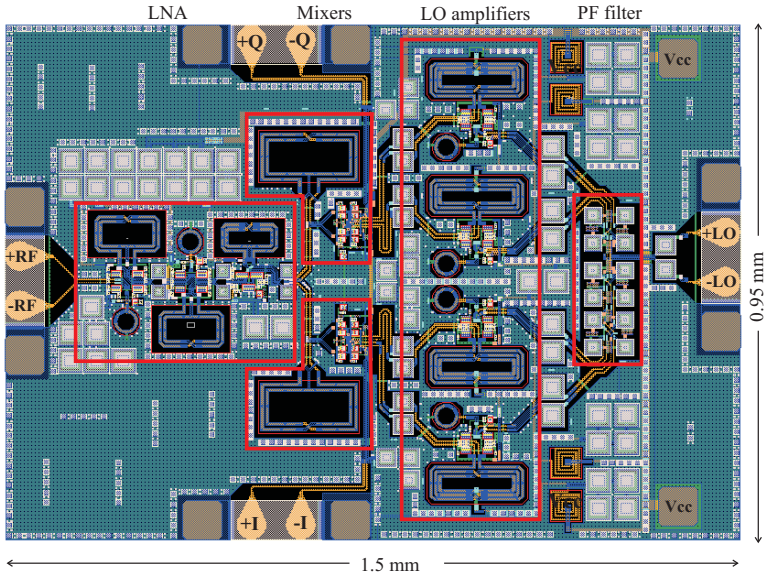


Figure 4.1: Layout of receiver with external LO

alone LNA. This means that system performance can easily be increased by re-tuning the LNA frequency response for a 24 GHz gain peak without sacrificing receiver linearity. Further improvement can be achieved by connecting the device by bond wires (or flip-chip technology) (as in a real application), choosing the wire lengths to add a series inductance to compensate for the capacitive LNA input impedance. This would reduce the LNA noise figure and increase the gain, directly impacting system performance.

The receiver noise figure was measured by connecting the baseband output via a low frequency balun to a spectrum analyzer. As the system conversion gain is not sufficient to compensate for the spectrum analyzer noise floor, a low frequency amplifier was interposed in the signal chain. The noise figure of this amplifier was not removed from the presented receiver noise figure.

The conversion gain was measured by connecting the baseband output to the 1 $M\Omega$ input port of a low frequency oscilloscope (through a balun). Phase and amplitude imbalance between the I and Q baseband channels, from phase and gain errors in the LO signals, was measured using the evaluation PCB (with a receiver having an integrated VCO) described in Section 5.3, showing 22° and 0.1 dB imbalance respectively. Although the phase imbalance is poor (typical acceptable values are 1 dB and 5° [11]), signal

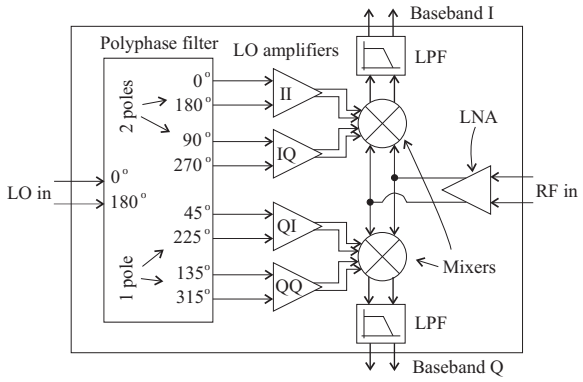
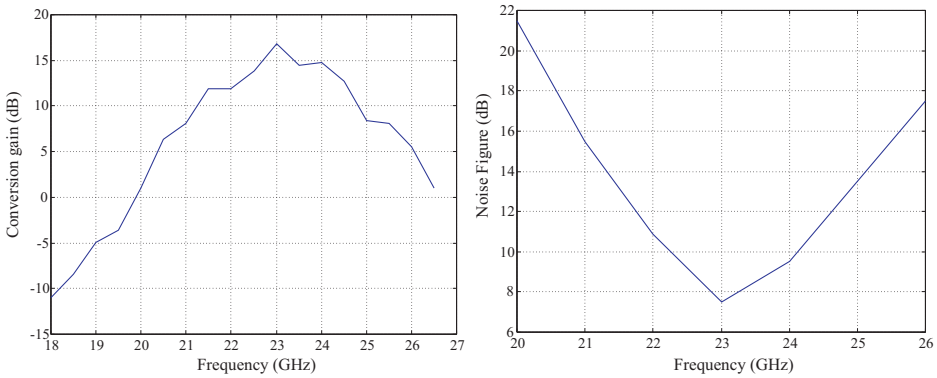


Figure 4.2: Block schematic of receiver with external LO

processing techniques can be utilized to correct the I/Q constellations. The low amplitude error indicates that both mixers are working as intended in the switching region; the phase error is most likely caused by the polyphase filter not giving the correct 45° shift between the one and two pole sections.

Important measured characteristics are summarized in Table 4.1. Total current consumption was 170 mA at 3 V and total area consumption was 1.4 mm^2.



(a) Conversion gain (b) Noise figure

Figure 4.3: Measured conversion gain and noise figure of receiver with external LO

DC Power	170 mA @ 3 V
Conversion gain @ 1 $M\Omega$	15 dB
$P_{1dB,in}$	-20 dBm
NF_{min} @ 100 Ω	7.5 dB
NF @ 100 Ω @ 24 GHz	9.0 dB

Table 4.1: Receiver with external LO measured characteristics

4.0.13 Monolithic Receiver with internal LO

A fully differential, fully monolithic receiver with integrated VCO is shown in Figure 4.4 with a block schematic in Figure 4.5. The LNA, developed at University of Ulm [6], is marked by a red box in the layout, with important electrical characteristics compiled in Table 4.2. Other components are recognized from Chapter 3. All measurements have been conducted at a single frequency (i.e. 24 GHz) due to the limited tuning range of the VCO. The Vcc terminal of each circuit block is connected through a local LC low pass filter before being connected together at the Vcc bond pad to minimize inter-circuit block signal coupling through the Vcc line

DC Power	55 mA @ 4 V
Gain @ 50Ω	21.5 dB
Isolation	$>$ 60 dB
$P_{1dB,in}$	-16.5 dBm
$P_{1dB,out}$	+4 dBm
NF_{min}	5.8 dB

Table 4.2: LNA characteristics

The system noise figure was 9 dB (at 24 GHz), which is identical to the noise figure of the version with external LO signal (at 24 GHz) even though using an LNA with higher gain and lower noise figure. This could be explained by insufficient LO drive levels from the integrated VCO making all transistors in the mixer switching quads contributing noise over the entire LO cycle. The good amplitude balance of the I and Q port however indicates that this is not the case. Another, more likely, explanation is that the LNA used with the external VCO was optimized for integration with the I/Q mixers, thus providing higher gain on-chip than what was measured using 100 Ω load impedance.

A 35.5 dB conversion gain, with a 24 dB gain IF amplifier cascaded, was measured by connecting the baseband output to a 1MOhm oscilloscope. By

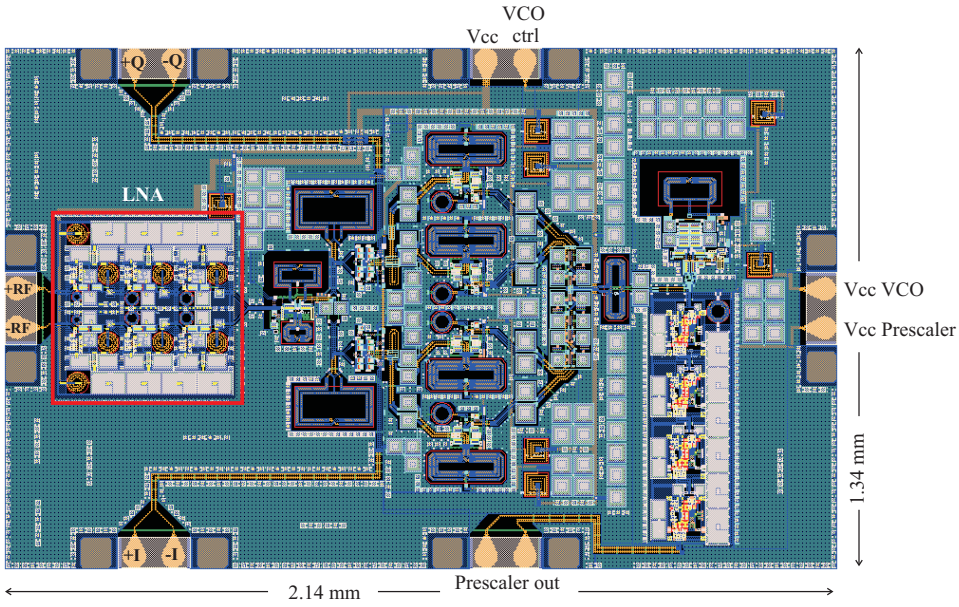


Figure 4.4: Layout of receiver with internal LO

removing the 24 dB IF amplifier gain (ignoring eventual impedance missmatch effects) a total receiver conversion gain of 11.5 dB was obtained. The reduction of conversion gain compared to the receiver with external LO indicates that the mixers are operated in the multiplication region, which has a lower gain and higher noise figure compared to when being fully switched. The linearity of the receiver is shown in Figure 4.6, with an input 1-dB compression point of -25 dB (output power un-calibrated). This indicates that the mixers in the IQ-demodulator is the limiting device in the receiver in terms of linearity.

Total current consumption of the receiver was 240 mA at 3 V and total area consumption was 2.9 mm^2. A version of the receiver using flip-chip pads instead of wafer probe pads was also designed, as discussed in Section 5.3.

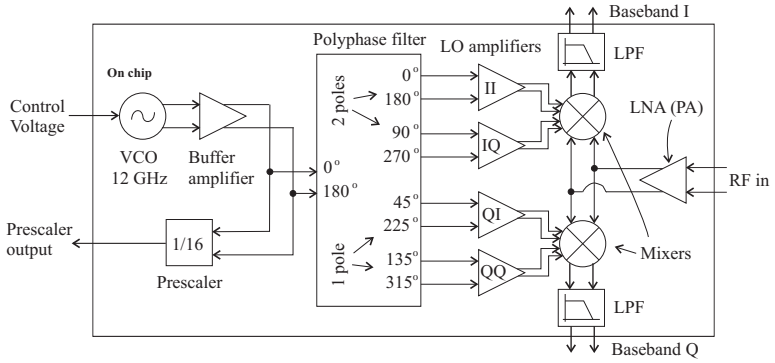


Figure 4.5: Block schematic of receiver with integrated VCO

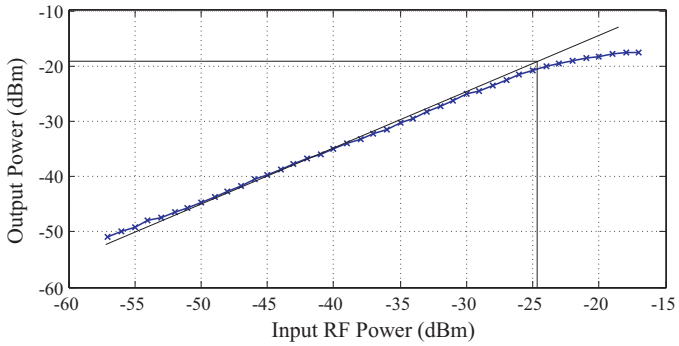


Figure 4.6: Measured linearity of receiver with internal LO

DC Power	223 mA @ 3 V
Conversion gain @ $1M\Omega$	11.5 dB
$P_{1dB,in}$	-25 dBm
Noise figure @ 100Ω	9 dB

Table 4.3: Receiver with internal LO measured characteristics

Chapter 5

RFIC Packaging using LTCC

5.1 LTCC packaging concept

Multi-layer Low Temperature Co-fired Ceramic (LTCC) technology is a packaging solution that has attracted a lot of attention recently for RF applications because of its exceptional high frequency electrical properties [40], including low substrate and metallic losses. Besides constituting an excellent chip carrier due to low manufacturing tolerances (important because of the dense pad placement in typical silicon devices), off-chip high-Q passive components such as inductors, capacitors, transmission lines and antennas can be embedded in the module, reducing the total cost and size of the system. The particular LTCC material chosen for the ARTEMIS radar demonstrator was Ferro A6, see Table 5.1. For this application, since the receiver and transmitter chips are fairly high power devices, the matching thermal expansion coefficient of LTCC to silicon was an essential feature compared to plastic packaging.

A four layer 10 x 7.5 mm^2 module with a two layer deep cavity for the RFIC was designed to provide DC and baseband connections to the PCB, as

layer thickness	100 μm
min spacing	100 μm
ε_r	5.9
tan δ	0.002
metal	12 μm Ag

Table 5.1: Material and processing properties of Ferro A6 LTCC

well as a 24 GHz high frequency transition from the differential on-chip input/output to the single ended PCB antenna. The cavity provides the chip mechanical protection and gives the on-LTCC transmission lines a homogeneous dielectric environment fairly independent on whatever material (if any) that is coating the LTCC module. Two different LTCC versions were manufactured with different via designs for thermal management studies [41].

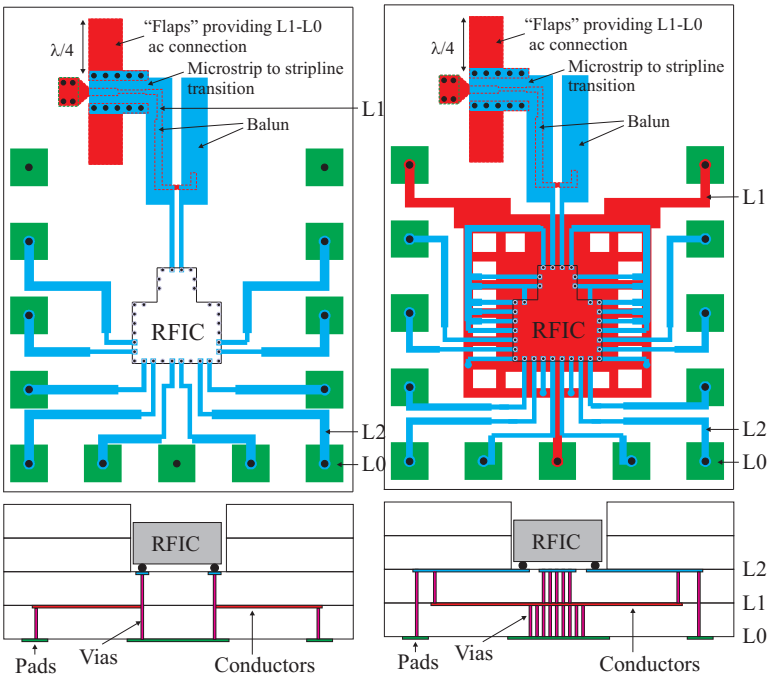


Figure 5.1: Layout of LTCC version 1 (left), with vias connecting all pads, and version 2 (right) with strips connecting all pads

The LTCC modules were mounted on the PCB using conventional solder paste stencil printed on the joint areas. The RFICs were joined onto the LTCC module using flip chip technique. Gold stud bumps were made on the chips using a wire bonder and the flip chip joining was made by thermo compression. Figure 5.1 shows the layout of the manufactured modules, mainly differing in the connections to the RFIC; all via connections (except for the RF input) in the left figure and all strip connections in the right.

5.2 Balun

The balun is based on a fourth order printed Marchand balun [42], shown in Figure 5.2, modified for use at high-microwave frequencies. It was schematically optimized in ADS and further analyzed in the EM software Zeland IE3D.

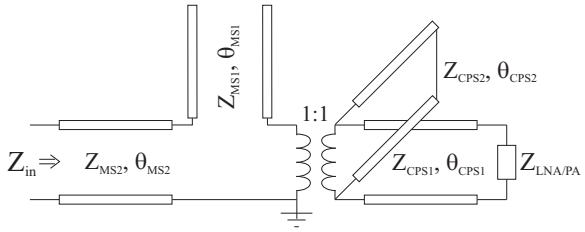


Figure 5.2: Schematic of 4th order Marchand balun

It should be noted that there are several theoretical solutions (values of Z and θ for the stubs and lines) for a standard Marchand balun that not only provides a good wide-band impedance match, but which also gives harmonic filtering up to 96 GHz, which could be advantageous for the PA output in the transmitter. Several of these solutions are also, in theory, easily implemented using standard impedance values (40-80 Ohms for microstrip and 70-90 Ohms for CPS on LTCC). One example of this is shown in Figure 5.3 with simulated results in Figure 5.4

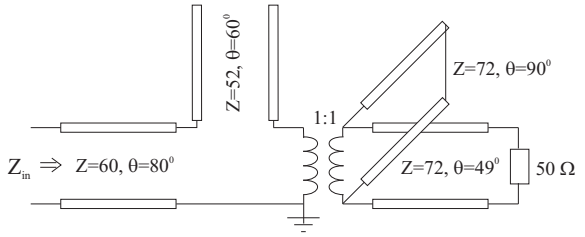


Figure 5.3: Example of Balun with harmonic filtering

However, EM analysis shows that because of the limited Q-values of real lines and stubs, these solutions are not practically realizable. In particular, the short circuit CPS stub has too much radiation losses (it behaves like a notch antenna) and was therefore replaced by an open stub in the implemented structure. The designed balun was manufactured in a back-to-back

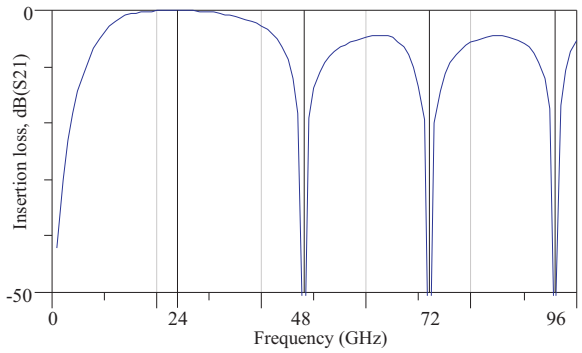


Figure 5.4: Simulated performance of ideal balun

configuration, see Figure 5.5, to facilitate measurements using a single-ended network analyzer. Measured performance was 0.88 dB insertion loss for one balun at 26 GHz, see Figure 5.6, in good agreement with simulations. The large reduction of bandwidth is caused by the probe pads, as predicted from simulations.

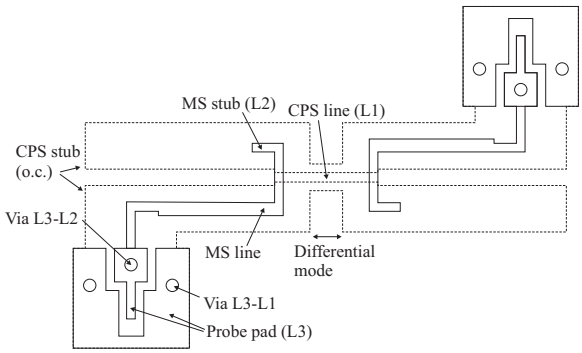
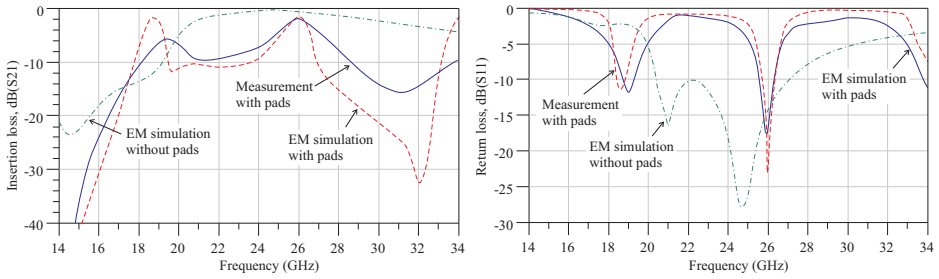


Figure 5.5: Layout of back-to-back baluns

In addition to the LTCC balun, a high frequency transition from LTCC to the PCB is necessary. Shown in Figure 5.7 is the layout of the complete 24 GHz signal path from differential RFIC output/input to single-ended PCB. The microstrip line and signal ground from the balun was bent downwards 90 degrees to keep the open CPS stub symmetrical.

The complete signal chain is, from upper right (RFIC input) to lower left (PCB output) in Figure 5.7, then:



(a) Insertion loss (b) Return loss

Figure 5.6: Measured and simulated return loss and insertion loss of back-to-back baluns

1. RFIC differential output
2. LTCC CPS line
3. LTCC Microstrip line with impedance Z1
4. LTCC Microstrip line with impedance Z2
5. LTCC Microstrip with side walls (via L2-L1) with impedance Z3
6. LTCC Microstrip with side walls (via L2-L1) with impedance Z4
7. Transmission line LTCC/PCB transition
8. PCB Microstrip with side walls (PCB via) with 50 Ohms impedance

The last transition, from LTCC to PCB, is complicated by the fact that the LNA is DC-coupled and hence no connection between LTCC microstrip ground (i.e. bottom CPS strip and lower RFIC terminal) and PCB ground is possible. Therefore, the LTCC microstrip ground is AC-coupled to the PCB ground using two quarter wavelength stubs (seen as horizontal stripes in Figure 5.7). According to simulations, the insertion loss was only increased 0.3 dB by this. No attempt of evaluating the complete signal chain by measurements were made, however, full-wave simulations indicate a total insertion loss of less than 2 dB (see Figure 5.8).

Extensive studies of thermal management and thermo-mechanical reliability of the demonstrator package has been conducted and is reported in [41].

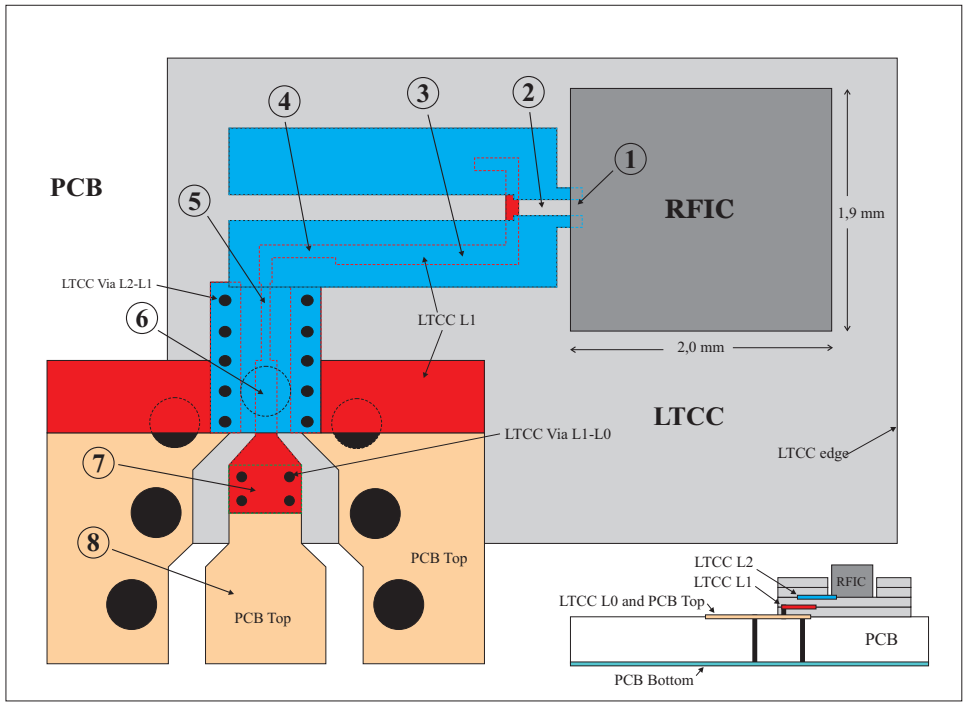


Figure 5.7: Layout of LTCC to PCB transition

5.3 Evaluation PCB

An evaluation PCB has been manufactured to test system performance of the receiver and transmitter. The LTCC module, with a receiver RFIC flip-chipped into the two layer deep cavity, was flip-chip mounted onto the PCB (0.5 mm Taconic TLC-30 substrate). Since the RFIC, shown in Figure 5.9, was designed for use also with an on-chip antenna the pad placement was arranged to be mainly orthogonal to the antenna polarization and mainly placed at the far side of the chip (more clearly shown in Figure 6.2 in Section 6.2. Furthermore, to reduce the capacitive loading of the connected antenna structure, the RFIC metal ground plane closest to the antenna was removed. For these reasons, the chip uses a larger chip size than what is necessary for the circuits alone. The extra available space for circuits could be used, if implemented in a BiCMOS process, for e.g. PLL circuitry.

The PCB is equipped with a two-element patch array (6 dBi simulated gain at 24-26 GHz) connected to the input of the RFIC through LTCC

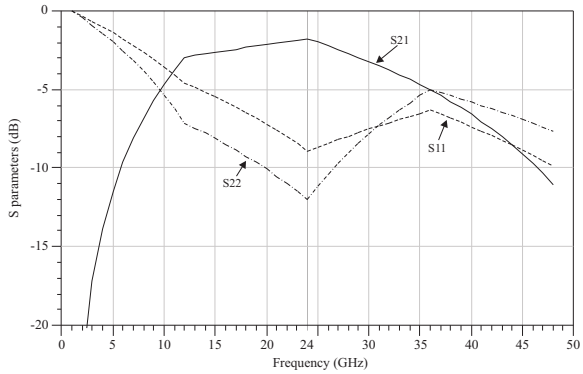


Figure 5.8: Simulated insertion loss of RFIC to LTCC to PCB transition

transitions described in previous sections. All DC traces have one large (10 uF) and one small capacitor (0.1 uF) to ground to shunt any noise picked up by the PCB or cables. In addition, there are several on-chip capacitor banks to shunt any 24 GHz signals coupled to the Vcc line.

The baseband signals are AC coupled to coaxial connectors through a center-tapped transformer useable for 60 kHz to 400 MHz signals. Using the evaluation PCB, phase and amplitude balance of the IQ demodulator could be measured, as reported in Section 4. A full characterization of the evaluation PCB is still to be made.

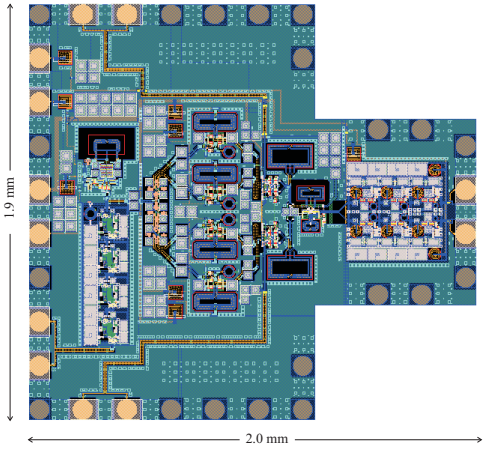


Figure 5.9: Layout of receiver RFIC using flip-chip pads

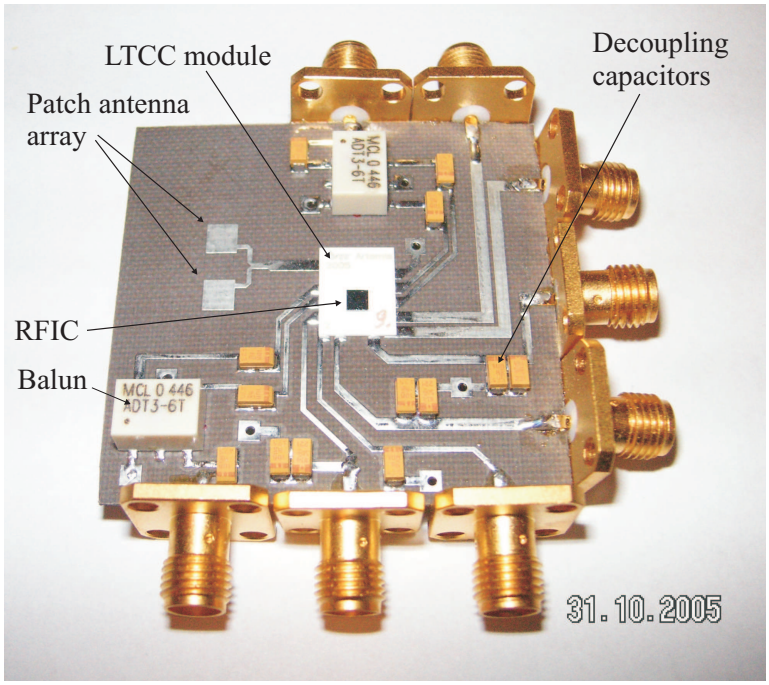


Figure 5.10: Evaluation PCB with RFIC flip-chipped onto LTCC module

Chapter 6

Conclusions and future work

6.1 Conclusions

This thesis has presented SiGe RFIC and LTCC packaging techniques demonstrating the feasibility of low-cost, compact short-range radar and communication devices for the 24 GHz ISM band. Completely monolithic direct conversion receiver and transmitter front-end chips have been manufactured and evaluated. By using a fully differential topology and subharmonic mixers, the typical concerns off LO self mixing and second order distortion associated with direct conversion have been addressed. While the receiver displays satisfactory performance for the targeted applications, the transmitter, although using verified subcomponents, showed insufficient system performance (probably due to biasing errors).

LTCC has been identified as a suitable chip carrier for millimeter-wave transceiver packaging, targeting applications using off-chip high gain antennas. A 24 GHz low-loss chip-to-PCB transition has been designed and evaluated, including a Marchand balun that was modified for high frequency operation.

6.2 Future Work

One of the main objectives in the ARTEMIS project was the development of monolithic transceivers with on-chip antennas for use in Bluetooth-like short range communication devices. Since the antenna would be on-chip, no external high-frequency interconnects would be needed thus simplifying packaging requirements. For circuits on low-resistivity silicon, the antenna

metallization was deposited on a thin layer of BCB and the silicon was etched away in the vicinity of the antenna to remove substrate losses. For circuits on high-resistivity silicon, the top-most metal layer in the semiconductor process was used for the antenna metallization and no post-processing (like etching) was deployed. Although this thesis has mainly focused on the radar application using a LTCC chip carrier, systems with integrated antennas have also been developed and manufactured. These systems, which so far have not been characterized, are briefly described in the next two pages of this section. Further suggestions on future work topics that could be interesting include:

- Correcting the layout problems of the biasing circuitry in the transmitter with internal VCO (see Figure 6.1).
- Replacing all nitride capacitors with MIM capacitors
- Evaluating the true system performance of the transceivers in a radar or communication link application, with the integrated VCO locked to an external PLL.
- Thorough characterization of the evaluation PCB, especially the 24 GHz RFIC-to-PCB transition.
- Replacing the LNA (re-tuned to 24 GHz) used in the receiver with integrated VCO with the LNA optimized for the IQ demodulator.

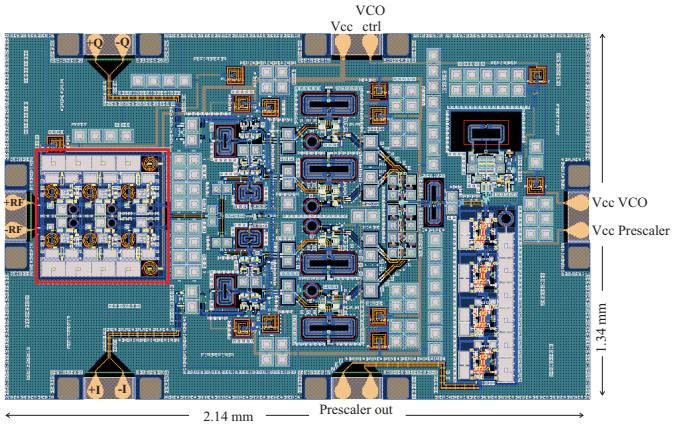


Figure 6.1: Layout of transmitter with internal LO

RFIC with integrated antenna on low-resistivity silicon

A receiver was manufactured with a reserved empty die area in which the p^+-layer was removed, see Figure 6.2. In post-processing, a thin BCB layer was deposited onto the silicon wafer with a meandered dipole antenna structure realized on top. Underneath the antenna, the silicon was etched away forming a BCB membrane. Since the effective dielectric constant experienced by the antenna is close to 1 (i.e. free space), a full size $\lambda/2$ dipole would be very large (>6 mm long) thus consuming too much silicon area. Therefore the dipole antenna was meandered down to a total length of 2.8 mm (trading of radiation resistance (efficiency) for reduced space). Total area consumption for the chip with integrated antenna could this way be restricted to <10 mm^2. The pad placement was arranged to be mainly orthogonal to the antenna polarization and mainly placed at the far side of the chip to reduce electromagnetic antenna-bond wire coupling. Furthermore, parts of the circuit ground plane closest to the antenna was removed to reduce the capacitive loading of the antenna.

A corresponding transmitter using the same antenna and pad configuration was also manufactured, however having the same biasing problem as previously mentioned.

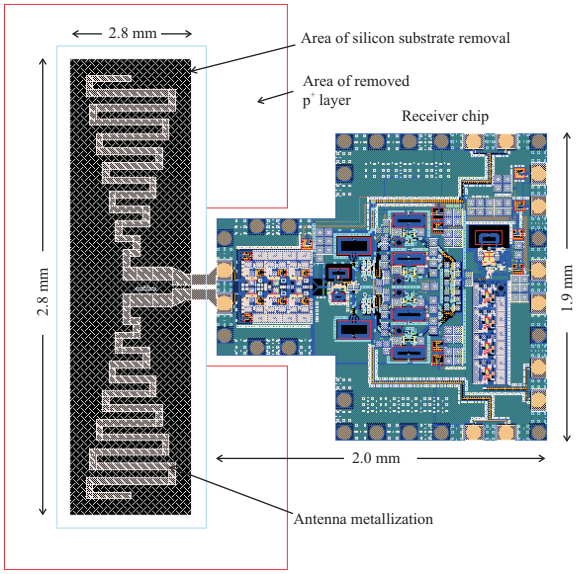


Figure 6.2: Layout of receiver RFIC with on-BCB antenna

RFIC with integrated antenna on high-resistivity silicon

A receiver was manufactured on high-resistivity silicon substrate with an integrated antenna realized using the top metal layer in the semiconductor technology, see Figure 6.3. Since the dielectric loading of the silicon (ε_r=11.9) reduces the antenna size for a given resonant frequency, it was sufficient to bend the outermost parts of the antenna towards the circuit to keep the area consumption within specified limits. Since no post-processing was necessary, the total chip cost and production time is reduced.

Although different design rules applies for circuits on high-ohmic substrates (i.e. a much larger minimum transistor spacing), no modifications were made on the receiver before production. Preliminary measurement results on manufactured circuits have so far not revealed any differences compared to circuits on low-resistivity substrate.

A corresponding transmitter using the same antenna was also manufactured, however having the same biasing problem as previously mentioned.

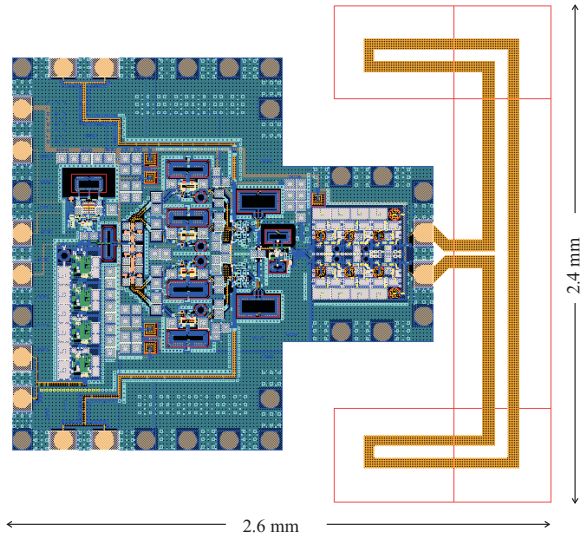


Figure 6.3: Layout of receiver with integrated antenna on high resistivity silicon

Appendix A

Measurement Set-up

A.1 Wafer probing

All measurements have been conducted on-wafer using a probe station with GSSG (Ground-Signal-Signal-Ground) probes for signal inputs and outputs and needles for DC connections. The GSSG probes were connected to a 6-26.5 GHz 180^0 hybrid using two short, equal length, coaxial cables. The hybrid converts the two 50 Ohm coaxial inputs, i.e. 100 Ohm differential impedance at the probe tips, into one 50 Ohm coaxial output that is connected to the measurement instrument. The probe station is placed inside a metal cage providing a common ground potential for all measurement equipment and wafer chuck to remove any potential ESD problems. The needle used for DC connection was connected to ground via the GSSG ground fingers using a wire.

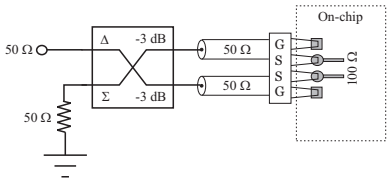


Figure A.1: Coaxial 50Ω to GSSG probe tip 100Ω chain

S-parameters were measured using a 2 port Agilent E8364B PNA Network Analyzer, calibrated using an on-wafer calibration kit (see Section A.1.1.

Noise figure measurements were conducted using an Agilent 8562A Spec-

trum Analyzer. The RF port was fed by an Anritsu MH3694A Signal Generator cascaded with a Pasternack 0-79 dB attenuator. The output (RF or baseband) was connected to low noise amplifiers with sufficient gain to suppress the noise figure of the Spectrum Analyzer and having a lower noise figure than the gain of the device under test (thereby adding negligible noise). By measuring the output signal to noise ratio $(S/N)_{out}$ on the Spectrum Analyzer and knowing $(S/N)_{in}$ (N=-174 dBm/Hz ensured by the attenuator, S measured), the noise figure was calculated from the definition $NF = (S/N)_{in}/(S/N)_{out}$. For frequency conversion devices (i.e. mixers), only double side-band noise figures are reported. This value is 3 dB lower than the single side-band noise figure given by the spectrum analyzer measurement.

Conversion gain for the down conversion mixers was measured by connecting the baseband output to a two channel low frequency oscilloscope with 1 MOhm 20 pF input impedance. By inverting one channel and adding the two signals, only the differential mode component was shown on the display. Since conversion gain is traditionally taken as baseband (or IF) output power divided by input RF power, the output voltage was converted to a power by assuming a 50 Ohm load impedance (which in practice can be facilitated by using baseband buffer amplifers like emitter-followers). In a real application, the baseband impedance is however most likely not 50 Ohms.

It was not possible to measure both I and Q ports, or modulate both ports in the up-converter, on-wafer due to lack of available probes in the measurement set-up. This means that phase and amplitude imbalance could not be measure on-wafer. These figures of merit were obtained for the LTCC packaged receiver from measurements on the evaluation PCB described in Section 5.3.

Phase noise was measured using a Spectrum Analyzer.

A typical measurement set-up for a receiver without integrated VCO is shown in Figure A.2.

A.1.1 On wafer calibration kit

Most circuits measured are designed for use in an all on-chip environment, i.e. as an intrinsic part of the transceiver. The circuit is connected to bond pads (or probe pads) to facilitate on-chip measurements using probes, however the pads are not integral to the circuit and its effect needs to be removed by de-embedding. For characterization of components such as inductors, it is common to use two de-embedding structures: a dummy short and a dummy

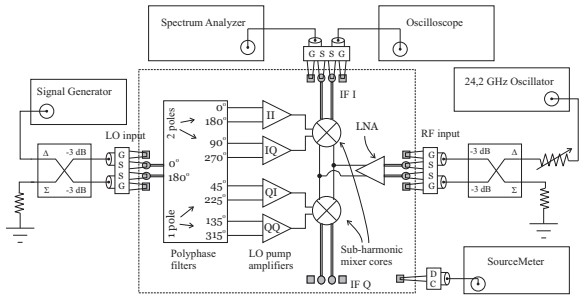


Figure A.2: Set-up for on-chip measurements of monolithic receiver

open [16]. After measurement of the device admittance Y_{DUT}, the dummy open admittance Y_{open} and the dummy short impedance Z_{short}, the pads and pad-to-circuit interconnect lines can be effectively removed from the measurement. This method requires some means of probe calibration, typically using a commercial high quality calibration kit similar to standard coaxial versions. Usually, this is done using single-ended GSG probes.

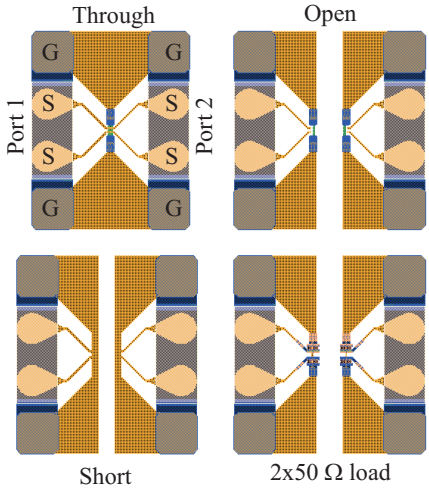
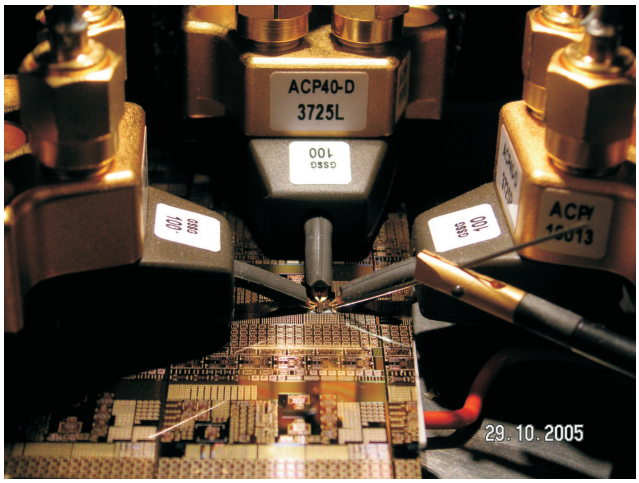


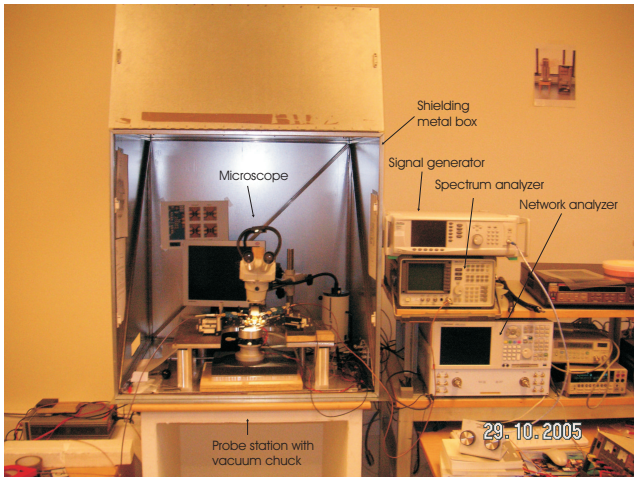
Figure A.3: On-chip SOLT calibration kit

An alternative approach, used in this work, is to calibrate the network analyzer directly on-chip. To this end, a standard SOLT (short, open, load, through) kit was designed and manufactured as shown in Figure A.3. As is

evident from comparisons between simulations and measurements throughout this thesis, this method provides good measurement accuracy. Better accuracy is obtained by using GSGSG probes with associated commercial calibration kit, connecting two single ended ports from the VNA to each differential on-chip port. This way, the complete mixed-mode S-parameter matrix can be measured providing more information compared to the method used in this thesis, e.g. differential to common mode conversion. This however requires a 4-port VNA for measuring a typical 2-port device.



(a) Probe station on-chip measurement



(b) Laboratory measurement set-up

Figure A.4: Pictures of probe station and laboratory set-up

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