Micromachined Antennas for Integration with Silicon Based Active Devices

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To my Parents

Abstract

In this thesis micromachined antennas suitable for on-chip integration with silicon based active devices are treated. The emphasis is put on compact 24 GHz antennas, capable of being integrated in commercial Silicon-Germanium (SiGe) processes using low temperature post processing micromachining techniques.

Antenna types covered are the slot loop antenna, wire loop antenna, meandered dipole and the inverted F antenna. The antennas have been implemented on surface and bulk micromachined low resistivity silicon substrates. It is found that the bulk micromachining method yields antennas with improved efficiency compared to antennas relying on thick dielectrics for reduction of substrate losses.

Two patch antennas, suitable for wafer level integration with actice devices are covered. A 60 GHz micromachined aperture coupled patch antenna with a bandwidth of 59-64 GHz is presented. A novel 24 GHz differentially fed patch antenna, manufactured using a thick organic dielectric, is modelled with a modified transmission line method.

Low Temperature Co-fired Ceramic (LTCC) and glob-top packaging for integrated antennas is evaluated. Epoxy based glob tops are found to have lower losses than silicone based ones.

Finally, crosstalk between the integrated antenna and simple on-chip wire interconnects is analyzed by simulations for slot antennas manufactured in a SiGe process. It is noted that by proper connection of the antenna to the semiconductor substrate a high degree of isolation can be obtained.

Acknowledgements

First of all I would like to thank my supervisor, Prof. Anders Rydberg, for all encouragement and support, as well as giving me the opportunity to work with several industry related projects.

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Contents

Chapter 1

Introduction

1.1 Background and applications

The use of high microwave and millimeter wave frequencies has to this date been restricted to professional applications, like long distance radio links and radar, due to the high costs of the equipment and requirements for individual licenses for use of frequencies. The license free 24 GHz and 60 GHz bands could however host mass market consumer applications like car anti-collision radars and wireless LAN devices, provided that compact low cost transceivers are made available.

The size and cost issues have partly been addressed by advances in semiconductor processes, enabling the design of complex MMIC (Monolithic Microwave Integrated Circuits). The Silicon Germanium (SiGe) bipolar processes are of particular interest since they allow the relatively low cost silicon technology to be used at high frequencies. An integrated single chip 24 GHz receiver [1] has been demonstrated using a commercially available SiGe process.

In order to produce a complete sensor or communication device the implementation of the antenna needs to be addressed. While long distance radio links and radar need large, high gain antennas, the targeted mass market applications will be short range, low power devices. An option in this case is to integrate the antenna directly on chip with the active devices. Advantages of integrated antennas are simplified packaging, no interconnect losses and considerable reduction of the space required by the radio front-end.

1.1.1 The 24 GHz ISM-band

The 24 GHz ISM (Industrial, Scientific and Medical) band covers 24.05-24.25 GHz in most of the world and use of devices in this band is usually free of any license requirements as long as the equipment conforms to certain standards. The most important restriction is that the EIRP (effective radiated power) is restricted to 100 mW, thus limiting the maximum communication or detection range.

The relatively small bandwidth ($< 1\%$) currently required by 24 GHz applications does not mandate the used of wide-band antennas. The antenna can however become de-tuned due to tolerances in manufacturing, or antenna mounting and packaging. It is therefore desirable to have a wide bandwidth unless the selectivity offered by the antenna is needed in order to reject out of band signals.

1.1.2 60 GHz WLAN applications

The 60 GHz band, which extends from 59 to 64 GHz, has been suggested for Wireless Local Area Networks (WLAN) use. The propagation in the band is limited due to the oxygen absorbtion peak in the band, thus naturally leading to small cell sizes appropriate for short range, high bandwidth WLAN applications.

The 60 GHz frequency range has traditionally been in the realm of Gallium Arsenide (GaAs) and other III-V compound semiconductors. However, with recent advances in SiGe processes, silicon is becoming a contender for active devices in this band.

1.2 Performance issues of integrated antennas

One key requirement of on-chip antennas is small size, since total die sizes of < 10 mm^2 are desirable for monolithically integrated antennas on foundry processed SiGe chips, due to the high cost of wafer space. For a square-shaped semiconductor die, an area of 3.3x3.3 mm^2 is available, which compared to the free space wavelength of 12.5 mm at 24 GHz corresponds to a die side length of a quarter of a wavelength. It is not possible to obtain the high antenna gain required by long range radars or radio links with an on-chip antenna of acceptable size (< 10 mm^2). The on-chip antennas described in this work are however suitable in short-range communication and sensor devices, where low antenna gain is feasible due to the omni-directional pattern usually required for such applications. The radiation patterns of all the

treated antennas, except the patch antennas, are bidirectional with maximums in the broadside direction and with back lobes of similar strength as the front lobes. The directivity of such antennas is generally less than 3 dB.

The antenna gain is always lower than the directivity due to conductor and substrate losses in the antenna. The antenna losses are characterized by antenna efficiency defined as

$$\eta = \frac{P_{rad}}{P_{input}} \tag{1.1}$$

where P_{rad} is the radiated power and P_{input} is the power at the antenna input terminals. Due to the fundamental limitations in antenna directivity mandated by the small size of integrated antennas the efficiency is the most important figure of merit for such antennas.

The aim of the work described in this thesis has been to maximize the radiation efficiency of small antennas by using micromachining methods compatible with the active circuits integrated on commercial, low resistivity silicon substrates. The methods studied are surface micromachining by application of the spin-on polymer Benzocyclobutene (BCB), and bulk micromachining where a BCB coated silicon substrate is etched from the backside to release the BCB and form a membrane. This etching can be performed either by wet etching or dry etching methods.

1.3 Outline of the thesis

Chapter two describes the basic micromachining process used for the realization of the antennas in this thesis.

Chapter three deals with slot antennas, which is an antenna type investigated since it is suitable for low loss implementation on micromachined membranes. Slot antennas are also compatible with the large areas of grounded metal typically used in circuits.

Chapter four describes a micromachined wire loop antenna, which offers a differential feed and compact integration in the limited space available on the semiconductor die.

Chapter five outlines the design of a reduced size dipole antenna, which also offers a balanced feed, thus suitable for integration with differential circuits.

The inverted F antenna (IFA) is evaluated and described in chapter six due to its small size, which makes it a good option when the area required by the antenna has to be minimized.

Micromachined patch antennas are considered in chapter six as an alternative antenna type suitable for wafer level integration or for assembly by stacked wafers.

1.4 Contributions

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D.G. Kurup, A. Rydberg and E. Öjefors, "Synthesis of Micromachined Antennas using the Genetic Algorithm", GigaHertz 2001 Symposium, University of Lund, Sweden, Nov. 26-27, 2001 Lund, Sweden.

E. Öjefors, A. Rydberg, M. Lindeberg and K. Hjort, "On the integration of a compact 24 GHz antenna into a commercial SiGe process", presented at the 3rd Workshop on MEMS for Millimeterwave Communication, 26 - 28 June 2002, Heraklion, Crete.

E. Öjefors and A. Rydberg, "Integration of a 24 GHz slot loop antenna in a commercial SiGe process", presented at conference Antenn03, 13 - 15 May 2003, Kalmar, Sweden.

E. Öjefors and A. Rydberg, "Design and cross–talk simulations of on-chip antennas for integration in a SiGe process", presented at the 4th Workshop on MEMS for Millimeterwave Communications (MEMSWAVE), 2 - 4 July 2003, Toulouse, France.

E. Öjefors, F. Bouchriha, K. Grenier, A. Rydberg, "24 GHz ISM-band antennas on surface micromachined substrates for integration with a commercial SiGe process," presented at the European Conference on Wireless Technology 2003, Munich, Germany, 6-10 October, 2003.

P. Abele, E. Öjefors, K.-B. Schad, E. Sönmez, A. Trasser, J. Konle, and H. Schumacher, "Wafer level integration of a 24 GHz differential SiGe-MMIC oscillator with a patch antenna using BCB as a dielectric layer," presented at the European Microwave Conference, pp. 293-296, Munich, Germany, 6-10 October, 2003.

E. Öjefors and A. Rydberg "LTCC and glob top packaging for 24 GHz MMIC with integrated antennas," presented at the symposium GigaHertz2003, Linköping, Sweden, 4-5 November, 2003.

E. Öjefors, A. Rydberg, M. Lindeberg and K. Hjort, "Millimeterwave antennas for integration into a commercial SiGe process", published in the new volumes of the "Micro and Nanotechnologies" series. Edited in the cooperation with Publishing House of the Romanian Academy.

Chapter 2

Micromachining

2.1 Introduction

Micromachining of silicon is a process where the semiconductor substrate is mechanically altered, either by removing parts of the substrate (bulk micromachining) or by adding layers and structures to the top of the wafer (surface micromachining).

In this chapter the specific micromachining processes used for the manufacturing of the antennas presented in this thesis are described.

2.2 Description of the targeted semiconductor process

The 24 GHz micromachined antennas described in this thesis have been designed for the Atmel SiGe2 bipolar process. The semiconductor substrate is p-doped and has a nominal resistivity of 20 Ωcm. In areas close to the transistors a highly conductive p+ doping, with a resistivity of 150 Ω/sq, is introduced at the surface of the substrate in order to suppress parasitic channels from forming between the active devices. This layer can be removed in areas of spiral inductors or on-chip antennas to minimize substrate losses.

High resistivity silicon substrate ($> 1500\Omega$cm) has recently become an option in the manufacturing. Although high resistivity substrates could partly obviate the need for micromachining to reduce substrate losses, restrictive design rules are currently required for the circuits.

2.3 Surface micromachining

2.3.1 Processing of BCB thick dielectric

The substrate losses in low resistivity silicon wafers used for transmission lines and antennas can be reduced if a thick layer of a low loss dielectric is deposited on the top of the wafer, before the transmission lines are metallized. A suitable dielectric is Benzocyclobutane (BCB) which is a polymer with a dielectric constant $\varepsilon_r = 2.65$ and low losses ($tan\delta = 0.0005$) manufactured by Dow Chemicals. The BCB can be applied to the top of the wafer as a conventional photoresist, and thicknesses 20-30 μm can be obtained if the polymer is applied in severeal subsequent spin-on process steps. Photosensitive BCB is also available, allowing patterning of the polymer layer. The BCB is cured in a furnace at 250 degrees Celsius, and the top metallization is finally evaporated, electroplated and patterned on top of the dielectric.

2.4 Bulk micromachining

Bulk micromachining refers to processes where parts of the bulk of the semiconductor substrate are selectively removed by etching processes. Two major techniques are used for bulk micromachining of silicon substrates, wet chemical etching and dry etching.

2.4.1 Wet etching

In chemical wet etching the surface of the silicon wafer is masked by a durable mask, such as silicon nitride, with openings where a liquid is allowed to etch the substrate. Wet etching of silicon substrates can either be isotropic, where the etching progresses with the same rate in all directions, or anisotropic where the etch rate in certain directions is restricted by the crystal planes in the semiconductor. Isotropic wet etching is difficult to control for larger etch depths and is not further considered in this thesis.

Anisotropic etching of silicon is a standard silicon micromachining process [2]. Typical etchant are Potassium Hydroxide (KOH) and Tetramethylammonium Hydroxide ($TMAH$). The etching is restricted by the (111) crystal planes in the substrate, thus leaving slanted walls of etched cavities if a silicon wafer with the standard crystal orientation (100) is used, as illustrated in Figure 2.1. High aspect ratio holes and cavities can therefore not be realized using these etchants. The major advantage of wet etching is that the processes are suited for batch processing since several wafers can

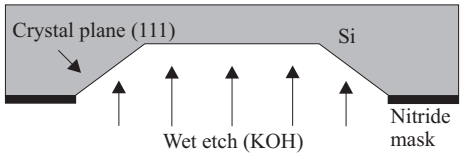

Figure 2.1: Anisotropic etching of (100) silicon

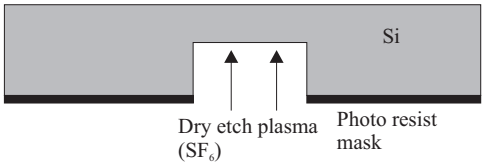

Figure 2.2: Dry etching (DRIE) of silicon

be simultaneously submerged in the liquid etchant.

2.4.2 Dry etching

Dry etching is performed in an evacuated chamber where a plasma is generated and used to etch the silicon substrate. The wafer is masked by photoresist and patterned with photolithographic techniques to enable selective etching.

In the commonly used Deep Reactive Ion Etching (DRIE) process by Bosch [3] the wafer is exposed to an alternating sequence of an etchant and a passivant. The etchant is a plasma of sulfur hexafluoride (SF_6) and the passivant is octafluorocyclobutane (C_4F_8). By the alternation between etching and passivation of the substrate the side walls of the etched holes are protected, thereby enabling high aspect ratio structures to be manufactured as shown in Figure 2.2. Good control over the etching process and selectivity against the mask is also obtained.

A disadvantage of the dry etching methods is that the etching is relatively slow and the machines are usually limited to single wafer processing. Typical attainable etch rates are in the order of 2 - 3 μm per minute [4], thus requiring long processing times if deep cavities are to be etched.

2.5 Membrane technology

Thin membranes of high quality dielectric materials offer a way of integrating high quality transmission line structures and antennas [5] on silicon substrates. By suspending the conductors on membranes in air, an effective dielectric constant of close to one can be achieved. Low losses are obtained since the silicon substrate is removed in the vicinity of the transmission lines or antenna conductors.

A low temperature membrane process, compatible with preprocessed semiconductor wafers, is obtained by combining the spin-on BCB dielectric process described in section 2.3.1 with bulk micromachining. The BCB membrane is released by back-side etching of the wafer using wet etching methods such as KOH or DRIE. DRIE has been used for the processing of all membrane antennas presented in this thesis.

Chapter 3

Slot antennas

3.1 Introduction

The slot antenna consists of an aperture in a ground-plane, where an electric field is excited across the slot. Using Bookers's relation [6] the straight slot antenna can be considered to be the complementary antenna to the wire dipole and many of its properties, such as input impedance, can be directly calculated from the wire antenna equivalents.

Slot antennas are typically analyzed using a magnetic current formulation, where the electric field in the slot and the slot itself are replaced by a magnetic current. The reformulated problem allows a compact representation since the magnetic current in the slot can usually be approximated as a linear combination of line sources, as in the case of electrical current elements on wire antennas, if the slot width is assumed to be small. In the analysis an infinite ground-plane is assumed.

Modelling and simulation of slot antennas using the electrical current formulation of the Method of Moments is also possible although it is less compact and requires all currents of the ground-plane to be considered. An advantage of the electrical current formulation is that the impact of a finite ground-plane can be considered.

By using micromachined membrane technology high performance slot antenna arrays have been built on silicon substrates [7]. The size needed for such antenna arrays, fully implemented on membranes, is however too large for monolithic integration on preprocessed SiGe wafers. In this chapter we consider slot antennas manufactured on low resistivity wafers where BCB dielectric layers and selective bulk micromachining is used to minimize sub-

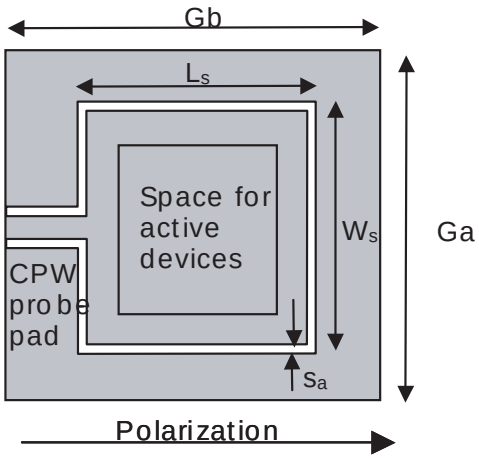

Figure 3.1: Integrated slot loop antenna

strate losses.

3.2 Slot loop antenna

The slot loop antenna consists of an annular or rectangular slot cut in a ground-plane. The circumference of the slot loop antenna is typically one guided wavelength at the frequency of operation since the second resonance of the antenna is normally used [8]. Due to its geometrical properties slot loop antennas are particulary interesting for compact integration on chip. Slot loop antennas integrated with active devices have been demonstrated in hybrid technology [9] and using high resistivity silicon and bulk micromachining [10].

A top view of a slot loop antenna for integration with active devices on a silicon substrate is shown in Figure 3.1. In order to minimize the chip size it is of interest to keep the antenna ground-plane dimensions as small as possible without compromising the antenna performance. The selection of a square loop is mandated by the requirement to maximize the silicon area inside the loop used for the active circuitry.

The circumference of the slot loop antenna is governed by the resonance condition of a total slot length of one guided wavelength [8] at the frequency of operation

$$\lambda_g = 2L_s + 2W_s \tag{3.1}$$

The guided wavelength of the slot-line for different substrates can be determined either using approximate expressions or full wave simulations for micromachined substrates. The influence of the dielectric substrate on the guided slot wavelength is characterized using the effective dielectric constant ε_{eff}, where

$$\lambda_g = \frac{\lambda_0}{\sqrt{\varepsilon_{eff}}} \tag{3.2}$$

is the relation between the free space wavelength and the guided wavelength.

The slot width s_a is not a critical parameter in the design of the antenna. Larger slot widths increase the bandwidth but also increases the size occupied by the antenna. Since the bandwidth requirements for applications within the 24 GHz ISM band are small, a small slot width has been used.

The slot loop antenna is normally fed across one of the voltage maximums as illustrated with the CPW feed in Figure 3.1. For a square slot loop on an infinite ground-plane in free space, an input impedance of 250 ohm can be calculated for an antenna in free space, using the Booker relation and published results for wire loop antennas. Introduction of a dielectric substrate in the antenna will alter the input impedance at resonance as well as change the effective dielectric constant of the slot line as will conductive losses in the substrate.

Matching of the resulting antenna impedance for various substrate selections to values suitable for the integrated circuits is discussed in Section 3.6.

3.3 Surface micromachined slot loop antenna

A 24 GHz surface micromachined slot loop antenna for integration with SiGe circuits on low resitivity silicon wafer has been designed [11] using the BCB process outlined in Chapter 2. The antenna was realized on a 11-15 Ωcm silicon wafer to simulate the substrate properties of pre-processed SiGe wafers.

In the used surface micromachining method, a layer of BCB dielectric is spun on top of the silicon wafer, and shallow trenches are optionally formed in the silicon by front-side etching. The trenches are subsequently filled by the BCB dielectric layer, which extends the height over the silicon substrate by 10-20 μm. The purpose of the spin-on BCB dielectric and the forming of the shallow trenches is to reduce the effective dielectric constant of the slot line and minimize substrate losses.

A schematic sketch of the stacked layers are shown in Figure 3.2. The cross

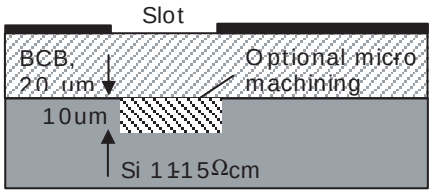

Figure 3.2: Surface micromachined slot loop antenna on BCB layer

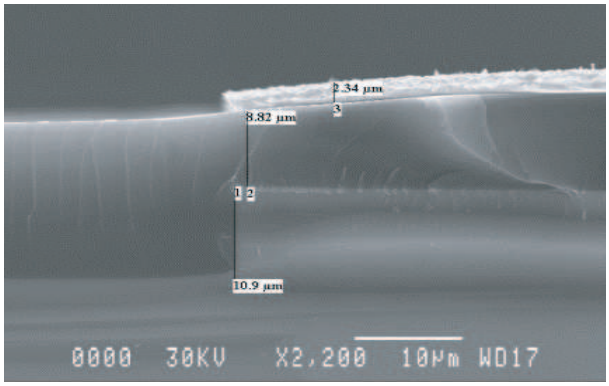

Figure 3.3: SEM view of surface micromachined antenna

section of the processed structure has been analyzed with Sweep Electron Microscope (SEM) and the corresponding photo is shown in Fig. 3.3. It can be seen that the shallow trench in the silicon is filled with the spin on BCB coating.

A square slot loop was designed to maximize the area utilization given a specific loop length. A relatively narrow slot width $s_a = 20$ μm was selected to maintain a slot mode despite the presence of a conductive silicon substrate. For the 20 μm slot width and the post processed substrate with 20 μm BCB a guided wavelength of $\lambda_g = 7$ mm at 24 GHz was determined by HFSS simulations of the compound substrate, corresponding to an effective dielectric constant $\varepsilon_{eff} = 3.2$.

The antenna slot dimensions $L_s = W_s = 2000$ μm, equal to a total loop length of $1.14\lambda_g$, were chosen after HFSS simulation of the antenna, including the finite ground-plane with the size 3x3 mm.

After processing the wafer was diced to individual antennas with chip sizes

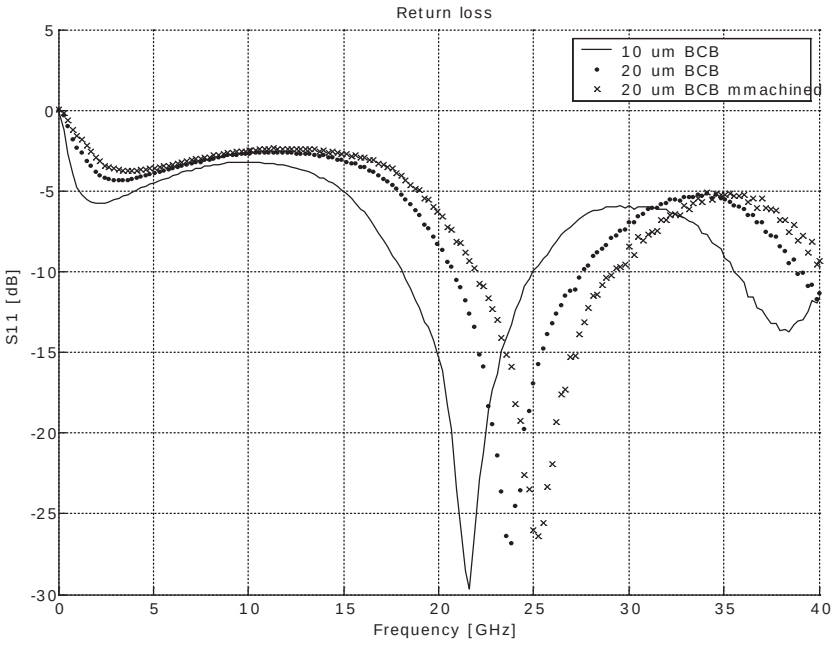

Figure 3.4: Return loss for surface micromachined antenna

equal to the ground-planes of the individual antennas.

3.3.1 Return loss and impedance

In Fig. 3.4 the return loss for antennas with identical metallizations with 10 μm and 20 μm thick BCB layers are shown, as well as results for antennas with shallow trenches. The return loss was measured in free space conditions.

The use of a thick BCB dielectric and the presence of micromachined shallow trenches reduces the effective dielectric constant and thus increases the frequency of resonance from 21 GHz for a 10 μm thick BCB layer to 24 GHz for a 20 μm one. The antenna featuring 10 μm shallow trenches localized under the slot, in addition to the 20 μm thick BCB, yielded a resonance at 25 GHz. It is seen that the distance to the silicon has a clear impact of the effective dielectric constant of the slot, a fact which has also been demonstrated for CPW transmission lines manufactured in the same

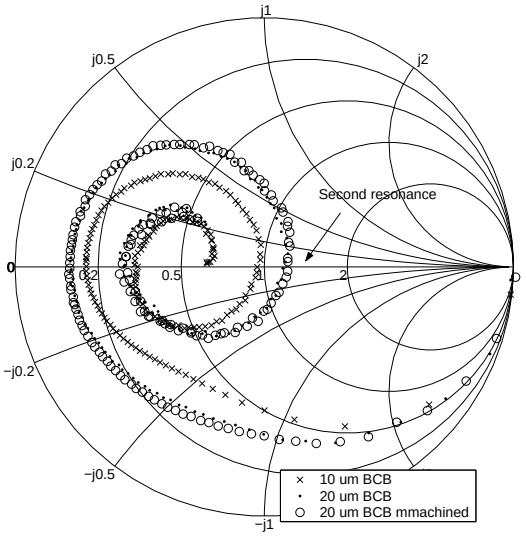

Figure 3.5: Input impedance of surface micromachined antenna for 10 μm BCB (crosses), 20 μm BCB (dots) and 20 μm BCB with shallow trenches (circles)

process [12].

The antenna input impedance, de-embedded to the point where the CPW feed line connects to the antenna slot is shown in Figure 3.5. The use of a 20 μm thick BCB dielectric over the 10 μm one increases the input impedance at the second resonance from 47 Ω to 58 Ω. Only a minor increase is seen by the addition of shallow trenches. The low input impedance largely obviates the need for matching networks in a 50 ohm system, but does also indicate strong interaction with the conductive silicon substrate.

The measured and simulated E- and H-plane radiation pattern for the slot loop antenna is plotted in Fig. 3.6. Nulls in the radiation pattern are obtained in the plane of the antenna as predicted by theory.

In the E-plane the antenna is partly shadowed by the wafer probe setup at angels between 30 and 90 degrees.

The efficiency simulated with HFSS of the antenna with 20 μm BCB but no trenches is 20%, yielding an antenna gain of -2.7 dBi. The measured antenna gain for an antenna with 20 μm BCB was -3.4 dBi at 24 GHz.

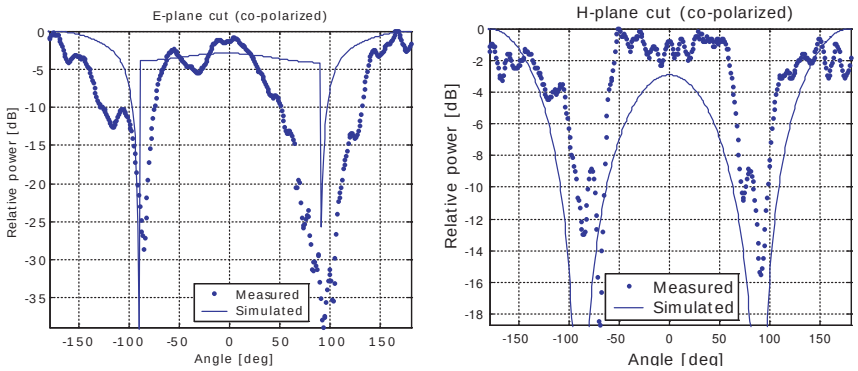

Figure 3.6: E- and H-plane, measured and simulated radiation pattern, -90 to 90 deg. correspond to top side of antenna

3.4 Bulk micromachined slot loop antenna

The use of bulk micromachining to form trenches under the slots in slot loop antennas has been proposed by Chen [10]. In the cited work, high resistivity silicon substrates were used, and the purpose of the micromachining was mainly reduction of the effective dielectric constant, thus increasing the size of the slot loop. The same principle should however also be useful for reduction of losses in an low resistivity silicon substrate.

3.4.1 Design and simulation

The largest improvement in efficiency is expected if the conductive silicon substrate is removed in areas of high electrical field strength as suggested in Fig. 3.7, where the slot loop is partly put on BCB membranes. Two silicon bridges with the width W_{br} are used to maintain mechanical stability of the die. The bridges are located at the E-field minimums in the slot loop, perpendicular to the CPW feed point, in order to minimize substrate losses. Antennas manufactured on non-homogenous substrates, such as micromachined silicon, can generally not be analyzed using the standard planar formulation of Greens functions in the Method of Moments (MoM) simulators like Momentum [13], thus requiring the use of full 3D simulation methods, such as finite elements (FEM) or time domain (FDTD) approaches.

By calculating the effective dielectric constant of the slot loop on the micromachined substrate, the slot dimensions required for resonance at the desired operating frequency can be obtained. The effective dielectric con-

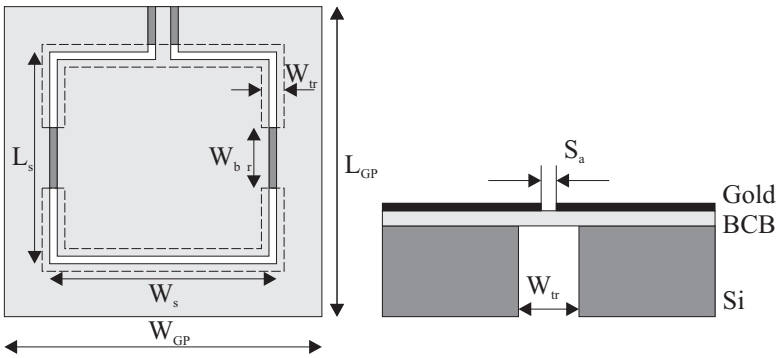

Figure 3.7: Slot loop antenna with bulk micromachined trenches

stant of the substrate is determined by the bridge width W_{br} and the trench width W_{tr}. The use of smaller trench widths or longer bridges yields higher dielectric constant and thus smaller antennas but also larger substrate losses.

An antenna with slot size $L_S = W_S = 2200$ μm and slot width $s_a = 20$ μm, has been manufactured with a trench width W_{tr}=100 μm and a bridge width W_{br}=200 μm.

The simulated antenna efficiency exceeds 50%, for 100 μm wide trenches.

3.4.2 Return loss and impedance

In Figure 3.8 the return loss and input impedance for the bulk micromachined antenna is shown.

A tuning frequency of 23 GHz is obtained. The input impedance at the useful second resonance of the antenna is 100 ohm, but the antenna could be matched by implementing the T-match in Section 3.6 if an impedance of 50 ohm is required.

3.4.3 Radiation pattern and gain

The simulated radiation pattern for the bulk micromachined slot loop antenna exhibits the same properties as the radiation pattern of the surface micromachined ones. 0 dBi antenna gain is calculated and the simulated antenna efficiency is 50%.

The gain of the bulk micromachined slot loop antenna with 100 μm wide trenches was measured at 24 GHz and found to be -0.7 dBi, which is an improvement of 2 dB over the surface micromachined antennas.

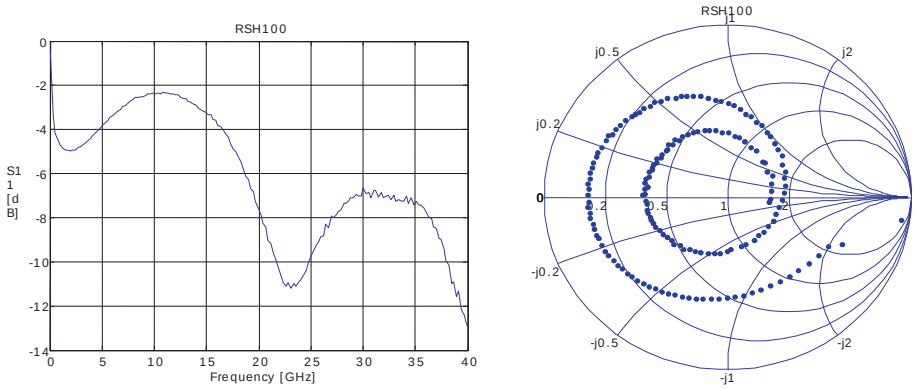

Figure 3.8: Bulk micromachined slot loop antenna, return loss and impedance (40 MHz - 40 GHz)

3.5 Bulk micromachined U-slot antenna

The slot loop antenna can be divided in two parts by short-circuiting the current maximums, thus forming two independent antennas. This can be useful for incorporating separate receiver and transmitter antennas or for beam steering, although the antennas will have to be separated to avoid excessive cross-talk. A single U-slot antenna can also be used to save space, at the expense of lower directivity and higher input impedance at resonance. The high input impedance can be reduced by folding the slot.

An advantage of the U-slot antenna over the slot-loop antenna is that the entire slot structure can be placed on a membrane, thus avoiding the losses encountered in regions where the silicon bridges are needed for the mechanical stability.

A folded U-slot antenna has been designed with the dimensions $L_a = 3000$ μm, $L_b = 1175$ μm, center conductor width 50 μm and slot width 25 μm. A sketch of the antenna is shown in Figure 3.9. The micromachined trench was centered around the slot and had a width of $W_t = 300$ μm.

The measured antenna return loss is plotted in Figure 3.10 and input impedance is plotted in Figure 3.11.

This antenna type has similar performance to the slot loop antenna, but lower directivity due to being only half of the size. The radiation properties of the antenna has not been measured, but HFSS simulations, incorporating the lossy silicon substrate, indicate better than 60 % efficiency.

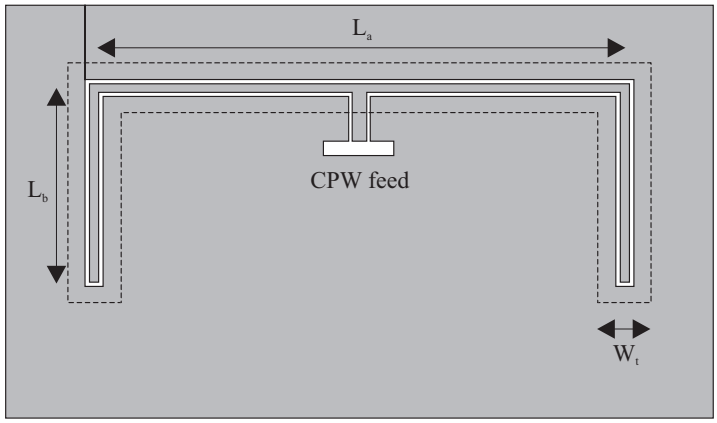

Figure 3.9: Folded U-slot antenna

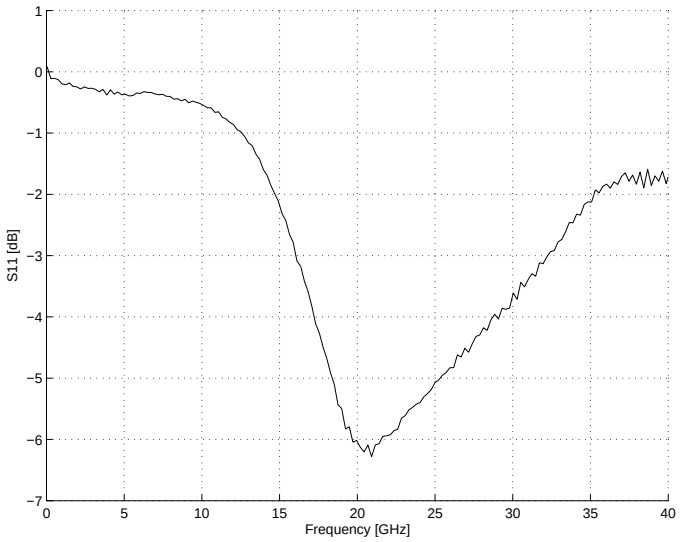

Figure 3.10: Return loss of folded U-slot

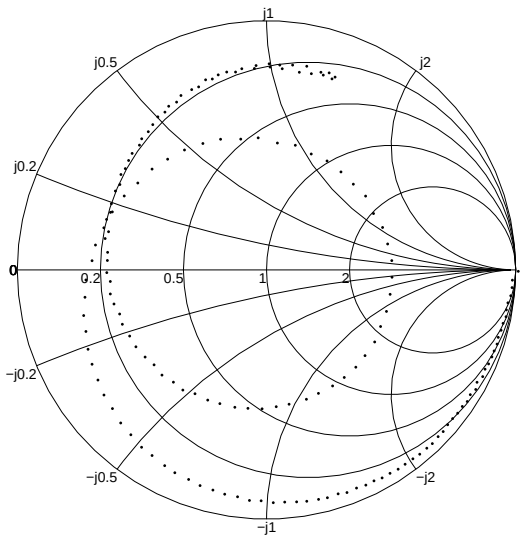

Figure 3.11: Measured impedance 40 MHz - 40 GHz of U-slot

3.6 Feed and matching networks

Depending on the antenna mounting and packaging a matching network might be needed to transform the high impedance of the slot antenna to a value suitable for the active circuits. One way of obtaining a 50 Ω match for a slot antenna is to feed it asymmetrically with respect to the voltage maximum. Such feeding techniques do however require the use of via holes and are thus not suitable for feeding slot antennas on membranes.

The T-match circuit has been suggested [14] for matching the high input impedance of the slot and slot loop antennas to the feed-lines. The advantage of the T-match circuit is that it can be compactly integrated with the antenna in the membrane region, thereby not requiring any additional space. The T-match for the slot loop antenna can be derived by using published formulas [15] for shunt matched wire antennas, and applying the Bookers principle for converting the results to slot antennas. Folded dipole and slot antennas can be treated as special cases of the T-match where the lengths of the matching arms are extended to quarter wavelength long sections, eliminating any capacitive reactance at the frequency of tuning. The applied voltage is divided between the slots s_{t1} and s_{t2}, and if the two slots are of equal width, the voltage division will be unity. The coplanar T-match can

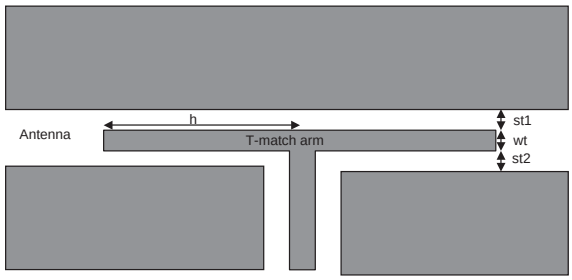

Figure 3.12: T-match layout

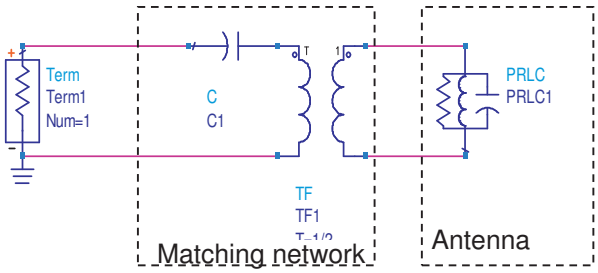

Figure 3.13: T-match equivalent circuit

be modeled by an equivalent circuit as shown in Fig. 3.13. The capacitance C models the coplanar waveguide (CPW) series stub created by the length h of the T-match arm and can be calculated using standard CPW transmission line equations. The transformer ratio is determined by the voltage division between s_{t1}/s_{t1}, where equal spacing yields an impedance reduction of four.

3.7 Summary

Slot antennas are a good choice for an integrated antenna if large ground planes are available in the integrated circuit, for instance in the form of ground shields around inductors. The slot loop is of particular interest since a square antenna footprint suites the typical shape of a processed semiconductor die.

Using a thick layer of BCB dielectric a 24 GHz slot loop antenna with 20 %

efficiency and -3.4 dBi gain has been demonstrated at 24 GHz. To improve the efficiency a similar antenna with bulk micromachined trenches under the slot has been designed, yielding an antenna gain of -0.7 dBi. Further work on characterization of the influence of micromachined trench width on antenna impedance, gain and efficiency is planned.

The high input impedance of slot antennas can be lowered with a compact impedance matching network in the form of a T-match, where the folded slot antenna is a special case. A limitation of CPW fed symmetrical slot antennas is that they are single-ended and thus not suited for connection to differential active circuits without the use of an on-chip balun.

Chapter 4

Loop Antennas

4.1 Introduction

The full wavelength loop antenna has been considered as an alternative for an on-chip antenna. The radiation pattern is bidirectional as in the case of the slot loop antenna, with a back-lobe of comparable size to the front lobe. A property of the loop antenna is its inherently balanced feed, which makes the antenna suitable for integration with differential circuit topologies without the use of on-chip baluns.

For integration on chip the square loop antenna is of special interest since it can be placed around the edge of a chip with active components. The presence of active circuit ground-planes in the center of the antenna will however reduce the radiation resistance and should therefore be considered in the antenna design.

Tabulated values for the impedance of polygonal shape wire loop antennas, calculated by the Method of Moments (MoM), are available in literature [16] for the free space case. At the commonly used second resonance the input impedance of a thin wire square loop is 80-j100 Ω thus requiring a total circumference of 1.15 λ for a resistive input impedance.

The wire loop antenna has a radiation pattern similar to the halfwave dipole, but with a compressed H-plane pattern. The theoretical directivity [15] of the wire loop antenna is 3.3 dBi.

An annular loop antenna has been demonstrated on micromachined silicon substrate, using a BCB membrane to suspend the loop antenna in air [17]. Despite the presence of a low-ohmic substrate at the edge of the membrane the antenna showed close to free space performance. However, implemen-

tation of a full wavelength loop antenna on a micromachined membrane implies poor utilization of the semiconductor substrate. In this chapter we present an alternative solution, where a full wavelength square loop antenna is manufactured using micromachined trenches on a low ohmic silicon substrate.

4.2 Design of micromachined loop antenna

To enable compact integration of circuits on the same substrate as the antenna the full membrane used in earlier approaches can be replaced by localized BCB membranes, here called trenches, under the wire loop as shown in Figure 4.1. The loop dimensions are $W_L = L_L = 3000$ μm, with a loop wire

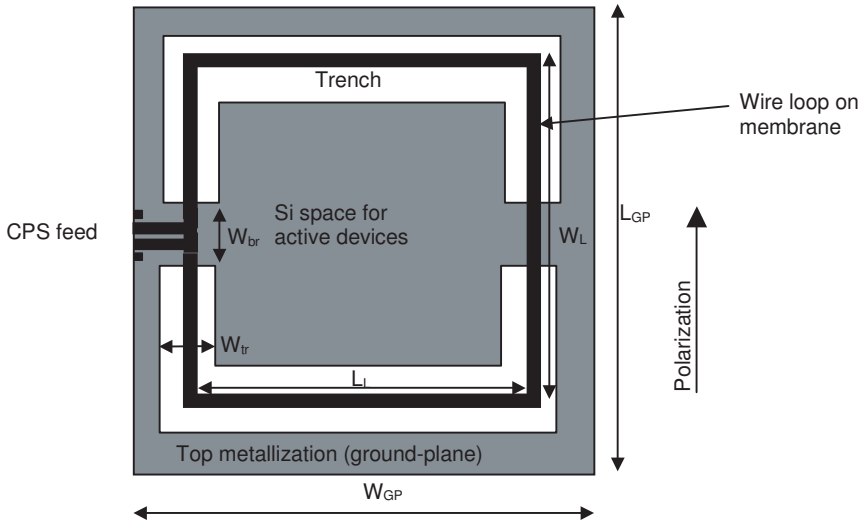

Figure 4.1: Loop antenna with trenches etched in silicon wafer

width of 120 μm and a trench width $W_{tr} = 360$ μm. The trenches were centered around the loop metallization. Two bridges of width $W_{br} = 200$ μm were kept to maintain mechanical stability of the substrate. The bridges were placed at the current maximums of the loop to minimize capacitive coupling to the substrate in the vicinity of the voltage maximums.

4.2.1 Loop antenna return loss and impedance

The return loss and antenna input impedance for the loop antenna is shown in Figure 4.2, together with Momentum [13] simulation results taking the 10 μm thick BCB membrane but not the silicon into account. The presence of the second (radiating) resonance at 23.5 GHz indicates an effective dielectric constant of the loop antenna on the micromachined substrate close to one. The measured and simulated impedance is plotted in Figure 4.3.

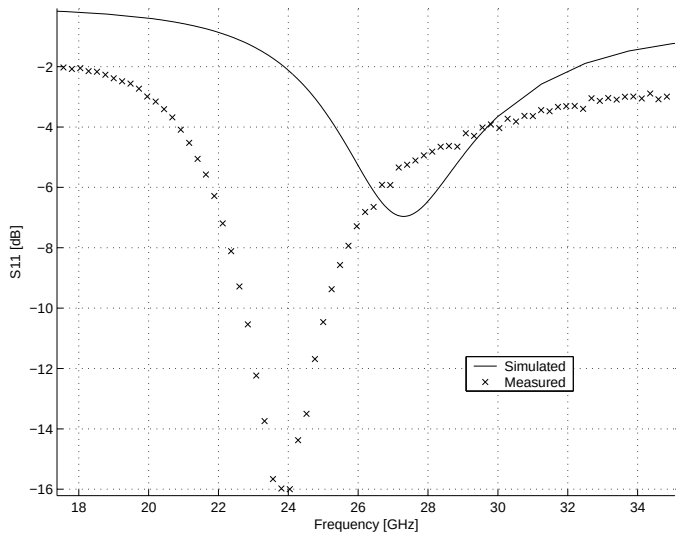

Figure 4.2: Loop antenna with trenches, measured and simulated return loss

The loop antenna can be modeled as a dual resonance circuit where the series resonant circuit represents the useful second resonance. The measured input impedance of 70 Ω is lower than the theoretical free space value and the shown simulated results where the influence of silicon is omitted, thus indicating some remaining interaction with the substrate.

4.2.2 Loop antenna radiation pattern and gain

The radiation pattern for the E-plane is shown in Figure 4.4, where angles between 0 to 180 degrees correspond to the top side of the wafer. The E-plane pattern exhibits typical dipole characteristics with nulls at 0 and 180 degrees and maximums in the broadside directions.

H-plane radiation pattern is shown in Figure 4.5. In the H-plane angles

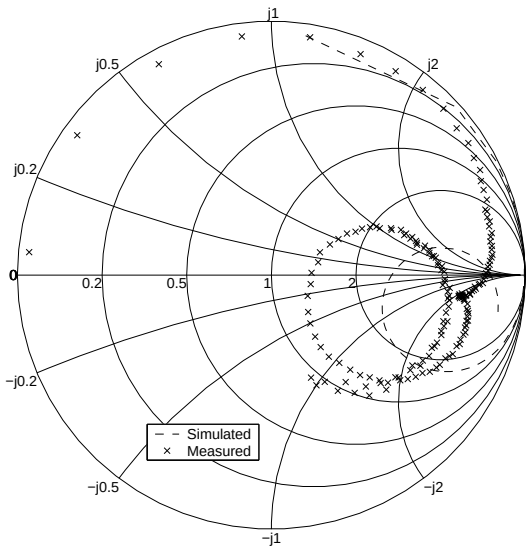

Figure 4.3: Loop antenna with trenches, measured and simulated (no silicon) impedance

between 0 and 50 degrees are blocked by the wafer probe setup and the region between 320 and 360 degrees partially shadowed by the probe support.

The broadside antenna gain was measured at 24.14 GHz and was found to be 1.9 dBi.

4.3 Summary

A square, full-wave loop antenna has been implemented on a micromachined 20 Ωcm silicon substrate using localized BCB membranes to support the loop. The demonstrated loop features a differential feed with an input impedance of 70 Ω at resonance, and is thus suitable for direct connection to an on-chip differential SiGe transceiver circuit.

By further work on modeling of substrate losses it should be possible to optimize the position and size of the localized membranes for lowest loss. Interaction with the metallization of the integrated active circuits placed in the center of the loop should also be investigated.

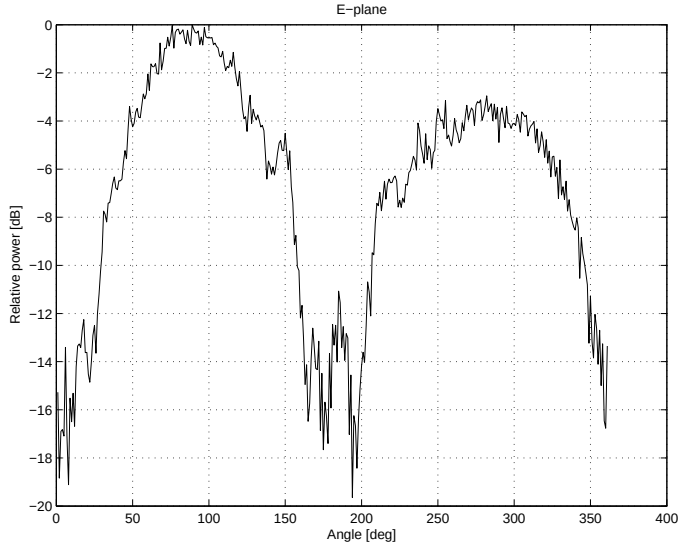

Figure 4.4: E-plane radiation pattern (0-180 deg corresponds to top side of wafer)

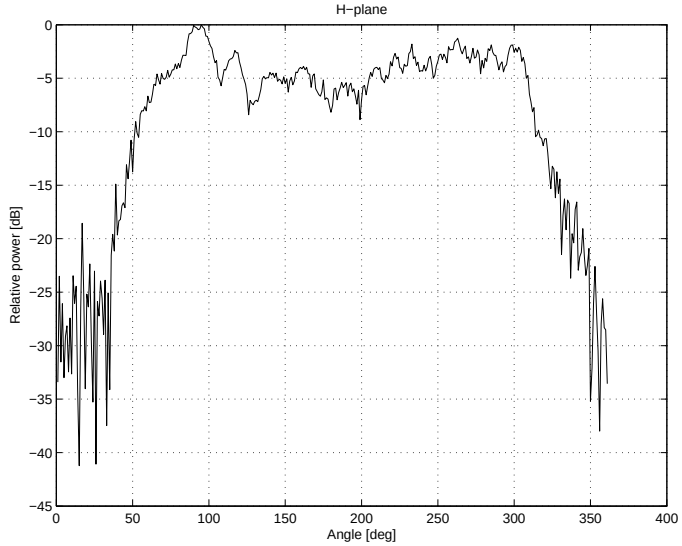

Figure 4.5: H-plane radiation pattern (0-180 deg corresponds to top side of wafer)

Chapter 5

Inverted F Antenna

5.1 Introduction

The inverted F antenna (IFA) is a compact antenna type originally proposed for low profile missile antennas [18]. The antenna consists of a quarter wave monopole radiator bent down towards a metal ground-plane as shown in Figure 5.1. The base of the monopole is connected to the ground-plane

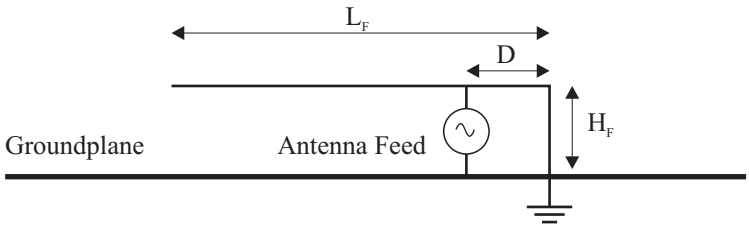

Figure 5.1: Inverted F antenna on infinite groundplane

by a shorting post and the monopole is shunt fed at a distance D from the shorting post. Selection of the feed-point position allows tuning of the antenna input impedance.

The IFA has been adapted to planar printed circuit board (PCB) implementation in several application in mobile communications [19]. Typically the inverted F is placed at the edge of the PCB. In the case of the Planar Inverted F antennas (PIFA) it has been shown [20] that in the absence of an infinite ground-plane the antenna impedance and radiation properties will be strongly dependant on the size and shape of the groundplane. The size of

the ground-plane as well as external connections to the plane must therefore be considered in the antenna design.

Integrated inverted F antennas have been realized on high resistivity silicon [21] at frequencies up to 20 GHz. In this chapter the design and evaluation of an IFA manufactured using a BCB membrane on a low resistivity silicon wafer is described.

5.2 Design of Inverted F Antenna on a BCB Membrane

5.2.1 Design and Simulation

An inverted F antenna, designed for implementation on a BCB membrane on a micromachined low resistivity silicon substrate is shown in Fig. 5.2. The length of the inverted F section L_F is 2500 μm and the distance to

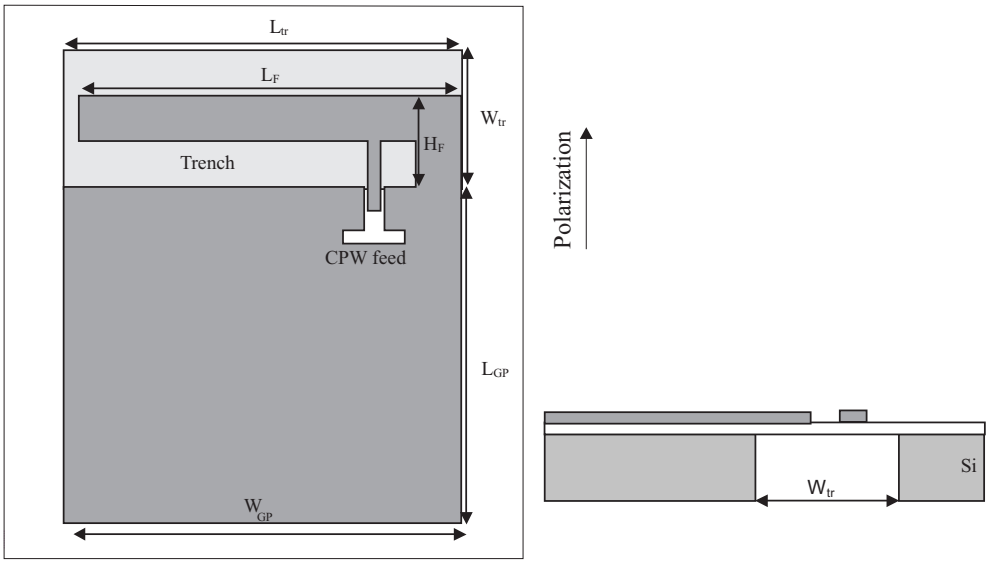

Figure 5.2: Inverted F antenna on micromachined substrate

the ground-plane H_F = 580 μm, thus corresponding to a total length of 3080 μm. According to [22] the distance H_F, corresponding to the straight section of a monopole extending from the ground plane, should be as large as possible in order to maximize the radiation resistance of the resonant

section. Increasing the length of H_F does however also increase the area consumption of the antenna.

The micromachined trench is $L_{tr} = 2600$ μm long, $W_{tr} = 900$ μm wide and centered around the F-section of the antenna in order to minimize the substrate losses in the region of high electric fields around the inverted F element.

The ground-plane size $L_{GP} = 2200$ μm, $W_{GP} = 2600$ μm was chosen to represent a typical circuit size. Since the current flow is largest around the edges the ground-plane does not need to be solid. It should have an outline of the specified size since it affects the antennas resonance frequency and input impedance. The antenna was fed with a single ended CPW feed at a distance $d = 280$ μm from the shorting post. The position of the feed point for a 50 Ω match was determined by simulation with HFSS [23] using a localized voltage source at the input terminals. The simulated directivity of the antenna at 24.1 GHz is 2.1dB with a gain of -0.3 dB, corresponding to a efficiency of 56 %.

5.2.2 Measurements

The measured and simulated antenna return loss for the designed antenna is plotted in Figure 5.3

The measured return loss agrees well with the simulated one with a tuning frequency of 24 GHz and a -10 dB bandwidth of 2 GHz.

The measured input impedance is shown in Figure 5.4 together with simulated results obtained with HFSS. In the Smith chart the short-circuit close to the feed is clearly seen at lower frequencies.

5.2.3 Radiation pattern and gain

The IFA E-plane (parallel to the feed) radiation pattern is shown in Figure 5.5. The pattern exhibits typical dipole characteristics with nulls at 0 and 180 degrees and maximums in the broadside directions.

The H-plane radiation pattern (parallel to the inverted F element) is shown in Figure 5.6. Ripple is present in the H-plane measurement and seems to orginate from currents on the shield of the the wafer probe. The probe enters the antenna pad footprint in parallel to the polarization of the antenna and connects to the antenna ground plane close to the current maximum of the inverted F shorting post.

The gain of the implemented IFA was measured -0.7 dBi at its maximum at 22.3 GHz. At the desired operating frequency 24.1 GHz the measured

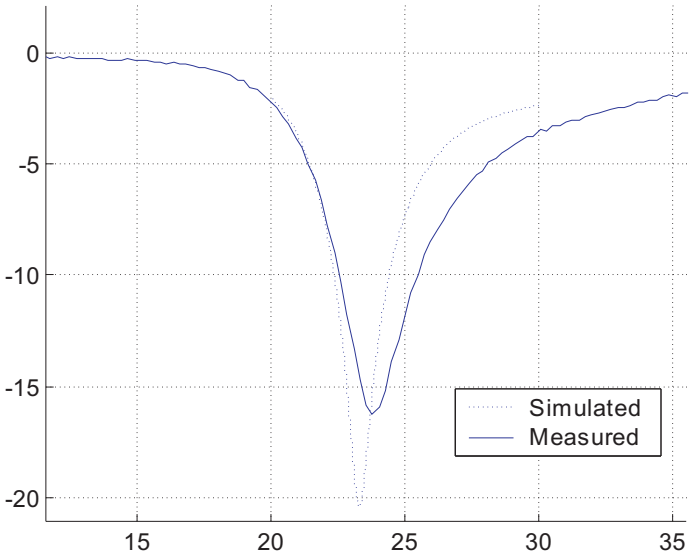

Figure 5.3: Measured and simulated return loss

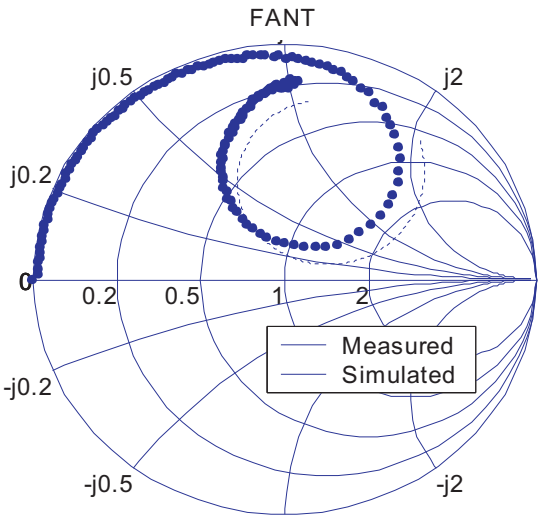

Figure 5.4: Measured (large dots) and simulated (dashed line) input impedance

gain was -2.2 dBi.

5.3 Summary

The inverted F antenna is a compact alternative for an integrated antenna when good polarization purity and independence of ground plane properties is not needed. When the inverted F element is placed on a membrane low substrate loading of the element is obtained, thus enabling the design of the antenna as in the free space case. Further work on identifying the amount of silicon substrate that needs to be removed from the vicinity of the antenna should make it possible to reduce the area requirement of the antenna.

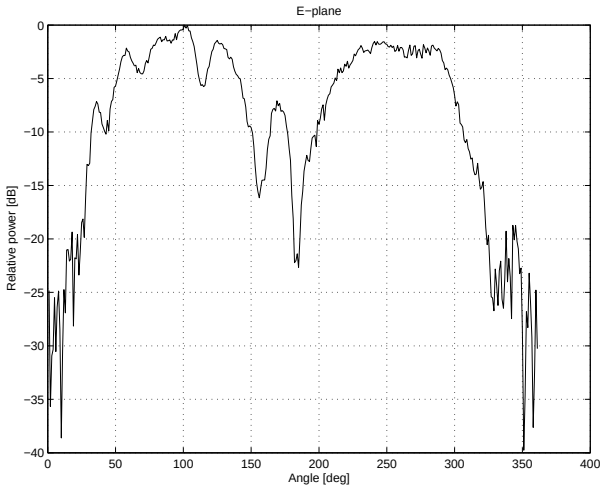

Figure 5.5: E-plane radiation pattern (0-180 deg corresponds to top side of wafer)

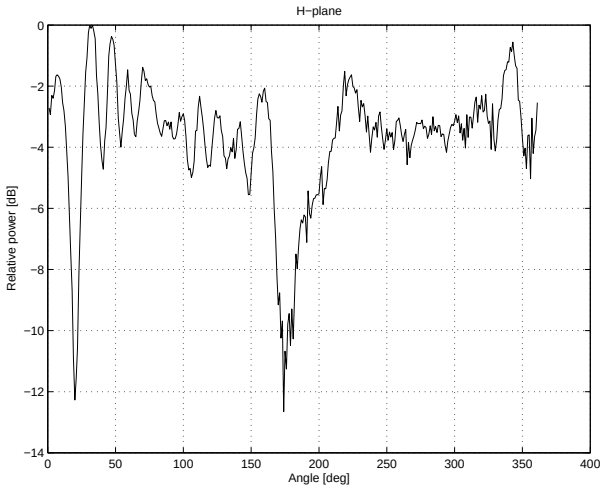

Figure 5.6: H-plane radiation pattern (0-180 deg corresponds to top side of wafer)

Chapter 6

Dipole Antennas

6.1 Introduction

The dipole has been considered as a candidate for on-chip integration. On-chip dipole antennas for clock distribution have been demonstrated at 15 GHz on CMOS substrates [24] and on high resistivity silicon substrates [25]. A 10 GHz dipole antenna has been integrated with a VCO in a commercial BiCMOS process [26].

The balanced feed of the dipole is an advantage for integration with differential circuits. However, its length of half a wavelength typically makes the dipole too large for integration on chip. To reduce the size of a half-wave dipole antenna, the radiator can be meandered [27]. Meandering of an antenna with a certain wire length largely maintains its resonant frequency but also reduces the radiation resistance. Since the loss resistance in the antenna remains relatively constant, the total efficiency of the antenna decreases.

6.2 Meander Dipole on Micromachined Membrane

6.2.1 Design and simulation

A meandered dipole, implemented on a BCB membrane to reduce substrate losses, is shown in Fig. 6.1. The length of the dipole L_{dip} is 3000 μm with a width W_{dip} of the meandered section of 500 μm. The dipole was implemented on a BCB membrane with size $W_{tr} = 760$ μm, $L_{tr} = 3300$ μm. An additional antenna with a larger membrane, where the spacing between the silicon and the meandered line was increased from 125 μm to 425 μm,

was also designed.

The theoretical directivity of a reduced size half wave dipole in free space is bounded by the value 1.8 dBi for an infinitely short dipole and 2.1 dBi for a full size half wave dipole.

6.2.2 Measured Return Loss and Impedance

The measured return loss and antenna input impedance is shown in Figure 6.2, together with an IE3D simulation considering the silicon substrate and a Momentum simulation without the silicon substrate present. The micromachined substrate was modeled by the 3D dielectric capability of the software. The impedance has been de-embedded to the edge of the membrane by on-wafer calibration transmission lines. Good agreement of tuning frequency between measured results and simulations is obtained. The measured impedance for the two different dipoles are plotted in Figure 6.3 together with Momentum simulation results for an antenna without the silicon substrate present.

The radiation resistance R_{rad} is reduced from the standard dipole value of 77 ohm to 20 ohm due to the meandering of the line. The meandered dipole can be accurately modeled for circuit co-design purposes by a standard series resonant circuit with series resistances representing radiation and loss resistance. It should be noted that integrated antennas are not always required to have a 50 Ω input impedance since the antenna and the active circuits can be co-designed.

6.2.3 Radiation Pattern and Gain

The radiation pattern for the E-plane is shown in Figure 6.4, where angles between 0 and 180 degrees correspond to the top side of the wafer.

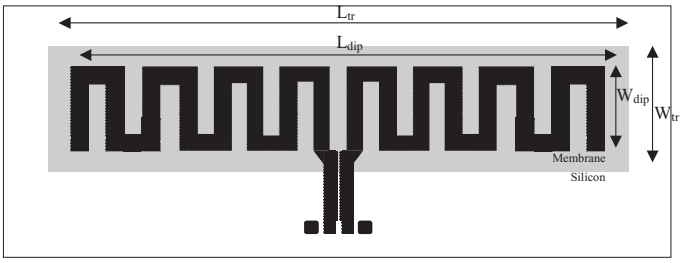

Figure 6.1: Meander dipole layout

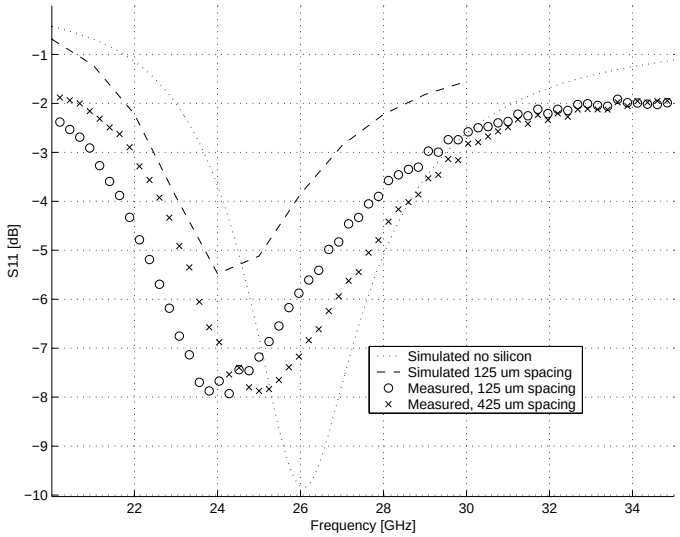

Figure 6.2: Measured and simulated meander dipole antenna return loss and input impedance

The pattern exhibits typical dipole characteristics with nulls at 0 and 180 degrees and maximums in the broadside directions.

H-plane radiation pattern is shown in Figure 6.5.

The H-plane pattern shows a constant beam strength with the exception of angles between 0 and 90 degrees where the wafer probe shadows the antenna under test.

The antenna gain was measured at 24.14 GHz and found to be -1 dBi in a 50 Ω system, which is in good agreement with the simulated gain of -0.2 dBi. Elimination of matching losses by an impedance transforming network should yield an increase in antenna gain.

6.3 Conclusions and Further Improvements

The meandered dipole antenna offers a compact solution for an integrated antenna when a balanced feed of the antenna is required for the integration with differential circuits.

The geometric shape of the meandered section can be optimized in order to maximize the radiation resistance and bandwidth of the antenna given a certain length of the dipole. The use of a bow-tie shaped meander has been

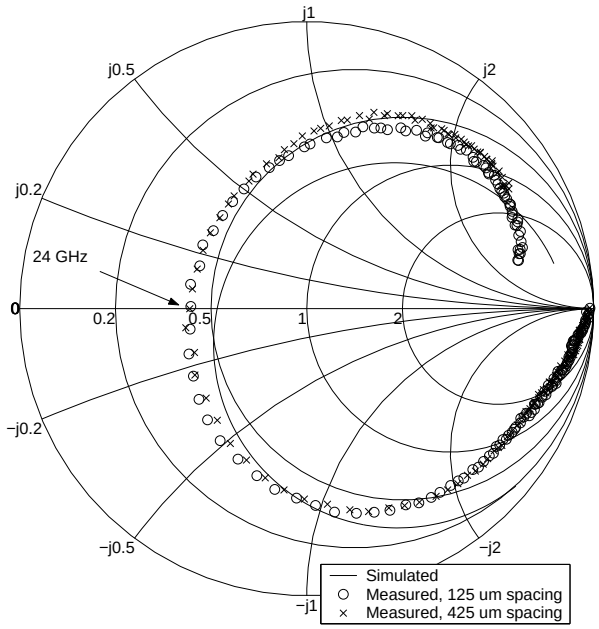

Figure 6.3: Measured and simulated (no silicon present) meander dipole antenna input impedance

suggested [28], since it minimizes the current canceling effect in the high current region in the middle of the antenna while still yielding a substantial reduction in total length.

Matching circuits, if needed in order to transform the low input impedance to a 50 Ω one, can be implemented as T-match sections [15] on the membrane.

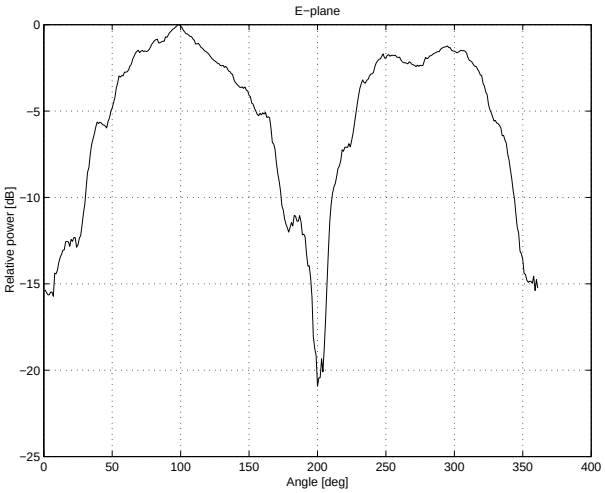

Figure 6.4: E-plane radiation pattern (0-180 deg corresponds to top side of wafer)

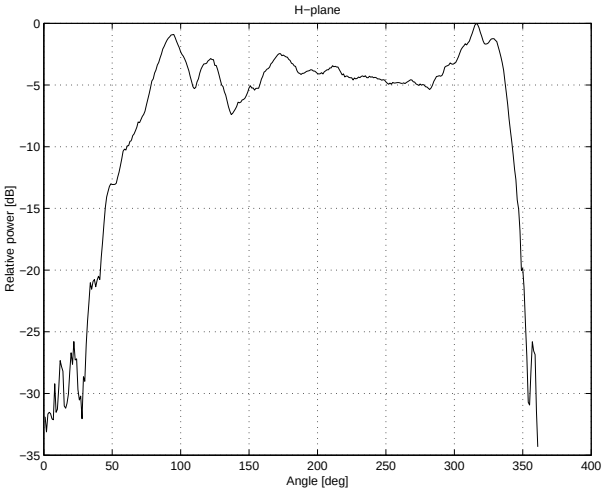

Figure 6.5: H-plane radiation pattern (0-180 deg corresponds to top side of wafer

Chapter 7

Patch Antennas

7.1 Introduction

Patch antennas have been a common choice for integrated antennas in hybrid designs, due to their low profile, high gain. The patch antenna is a popular antenna type consisting of a wide metal patch on top of a grounded dielectric substrate. By exiting a TM_{010} mode between the patch and the groundplane, radiating fringing fields will occur at two of the edges.

A patch antenna manufactured on silicon will exhibit small bandwidth and poor performance due to the high dielectric constant of the substrate. Conductive losses in the silicon will lead to poor efficiency, thus requiring the use of high resistivity silicon which is generally not compatible with standard SiGe bipolar and CMOS processes.

A solution to these problem is offered by micromachining methods. The lossy silicon can be removed by back side etching of the substrate, thereby creating a cavity under the patch or by depositing a low permittivity, low loss dielectric such as BCB to the top of the wafer and realizing the patch on top of this layer.

In this chapter two micromachined patch antennas are considered, one 60 GHz aperture fed patch antenna on a bulk micromachined high resistivity silicon substrate, suitable for a stacked wafer integration with an active transceiver module, and a differentially fed patch antenna developed on a thick BCB layer designed for wafer level integration with a 24 GHz differential SiGe oscillator.

7.2 Micromachined 60 GHz Patch Antenna

To increase the efficiency and bandwidth of such an antenna, part of the substrate beneath the patch could be removed using bulk micromachining techniques, thus reducing the effective dielectric constant of the substrate. Such an approach has been presented by Papapolymerou [29].

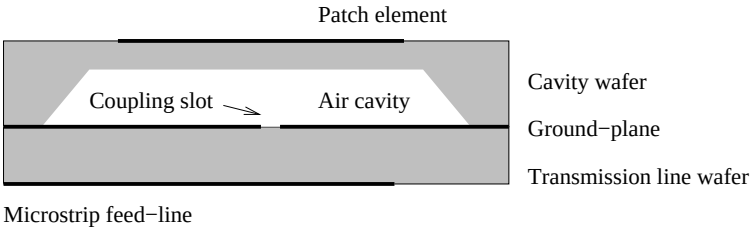

Figure 7.1: Micromachined silicon patch antenna

A well known problem in the design of wide-band patch antennas, is that the requirements on the substrate are vastly different for the radiating patch element and the feedline (typically microstrip). By using aperture coupling between the patch and the feedline, a high permittivity substrate could be chosen for the microstrip feed, while a substrate with a lower dielectric constant could be selected for the patch-antenna element. Another advantage of aperture coupling over other feed types is that the feed network is completely shielded from the radiating elements by the ground-plane.

By combining silicon micromachining techniques and aperture feed a highly efficient patch antenna can be made by stacking two silicon substrates on each other. A thick wafer is selected for the upper wafer to obtain good radiation characteristics where a cavity is opened underneath the patch. A thinner wafer is selected for the transmission lines, thus reducing the risk for substrate modes.

7.2.1 Modeling of Patch Antenna on Non-Homogenous Substrate

The effective dielectric constant of the mixed air-silicon patch substrate can be calculated using the quasi-static capacitor model presented by Papapolymerou [29]. The expression (7.1) gives accurate results as long as the cavity is large enough to accomodate the fringing fields of the patch. x_{air} is the

ratio of air to full substrate thickness.

$$\epsilon_{cavity} = \frac{\epsilon_{air}\epsilon_{Si}}{\epsilon_{air} + (\epsilon_{Si} - \epsilon_{air})x_{air}} \tag{7.1}$$

As in the case of microstrip transmission lines, an equivalent dielectric constant ϵ_{reff} needs to be calculated. This equivalent constant is used to replace the substrate and the surrounding air with a fictitious homogeneous material. It can be calculated as shown in Eq. 7.2.

$$\epsilon_{reff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}\left[1 + 12\frac{h}{W}\right] \tag{7.2}$$

Due to the fringing fields at the ends of the patch the electrical length of the element is longer than the physical length. A popular formula for computing this length ΔL has been derived by Hammerstad [30] and is presented in 7.3

$$\frac{\Delta L}{h} = 0.412\frac{(\epsilon_{reff} + 0.3)\left(\frac{W}{h} + 0.264\right)}{(\epsilon_{reff} - 0.258)\left(\frac{W}{h} + 0.8\right)} \tag{7.3}$$

The physical length L of the patch can be determined using eq. 7.4.

$$L = \frac{c}{2f_r\sqrt{\epsilon_{reff}}} - 2\Delta L \tag{7.4}$$

7.2.2 Aperture-coupling

An equivalent circuit model of the aperture-coupled patch antenna based on transmission line analysis has been presented by Himdi [31]. Figure 7.2 depicts the suggested circuit model. The coupling slot in the ground-plane can be modelled as two tranformers, transforming current between the patch antenna element and the microstrip transmission line. Y_{patch} represents the radiation resistance of the patch element and Y_{slot} the susceptance of the slot. A short-circuit at the coupling slot is obtained by terminating the microstrip with a $\lambda_g/4$ open stub, thus maximising the current in the lower transformer. The susceptance Y_{slot} will appear as a pure inductance if the length of the slot is well below its resonant length.

The coupling efficiency between the microstrip transmission line and the patch element can be increased if a H-slot is used instead of a traditional rectangular slot. This fact was demonstrated by El Yazidi *et al* in [32]. The use of an H-slot enables selection of shorter slots for the same amount of coupling, thus insuring that the slot can be operated well below its resonant frequency.

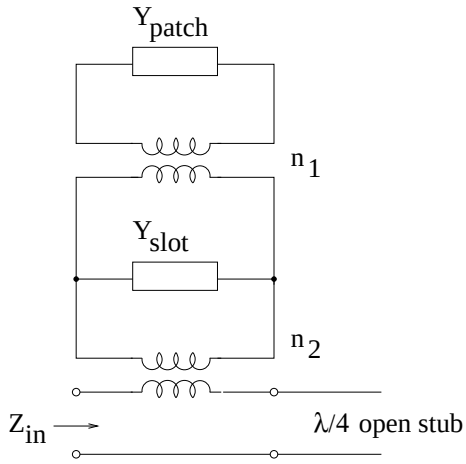

Figure 7.2: Equivalent model of aperture-coupled patch

7.2.3 Design and Simulation

The antenna structure is shown in figure 7.2.3. A square patch was selected to allow for dual-polarization use (with a suitable feed network). A 50 μm thick silicon membrane was selected as a compromise between surface mode rejection and ease of manufacturing. Using a capacitor model (7.1)

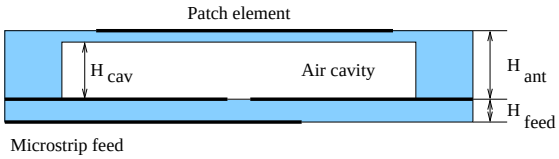

Figure 7.3: Side view of the micromachined patch antenna

the dielectric constant of 1.24 was calculated for a 254 μm thick silicon substrate with a 200 μm deep cavity. From HFSS simulations it can be seen that this model of the effective ε yields a higher resonance frequency than the simulated one.

With equation 7.4 and subsequent HFSS simulations a patch antenna size W=L=1500 μm was determined for a 60 GHz resonance frequency. By selecting a W_{cav}=L_{cav}=3 mm large cavity underneath the patch element most of the fringing fields was found to be accomodated within the cavity, thus preventing excitation of surface waves.

The microstrip line is aperture coupled to the patch with an H-shaped

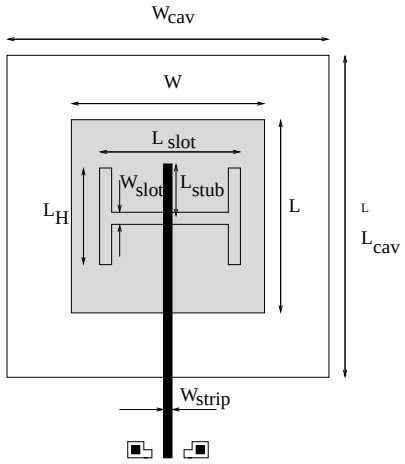

Figure 7.4: Top view of the micromachined patch antenna

slot with the dimensions L_{slot}=1100 μm, L_H=600 μm and W_{slot}=110 μm. The improved coupling of the H-slot over a rectangular one allows for a slot-length well below the resonant region of the slot.

A L_{stub}=0.45 mm long quarter-wave stub is used to give the microstrip line a short-circuit termination after the slot.

A set of identical antennas to these described above were equipped with diode detector circuits to facilitate indirect radiation pattern measurements. A GaAs flip-chip diode is used to detect the received signal at the antenna terminals. The detector setup is shown in figure 7.5.

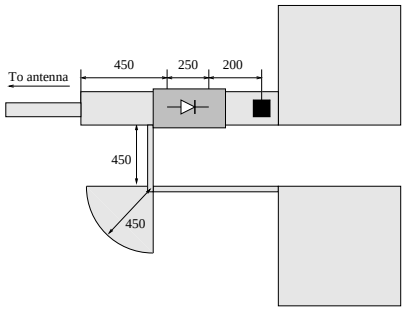

Figure 7.5: Diode detector circuit with feed line and DC-pads

The diode is provided with 0.4 mA bias current through the network shown in figure 7.5. The junction capacitance C_j and the parasitic capacitance C_p

of the diode is partly tuned out by the inductance of the ground via-hole and of the microstrip. A 450 μm long quarter-wave transformer is used to tune the residual real part of the diode impedance to 50Ω. Simulations of the the detector circuit predict an acceptable return loss in the 50-60 GHz frequency range.

7.2.4 Manufacturing

The patch antenna was manufactured on high-resistivity, double polished, (100) silicon wafers. The wafer carrying the transmission lines and the slot was thinned from 254 to 100 μm and processed using the same methods as described in Chapter 2.

The patch antenna elements were manufacured on a polished 254 μm thick wafer. The 3 x 3 mm large cavities were opened with dry etching, leaving a 50 μm thin membrane. Due to problems with the processing equipment, aluminium instead of gold had to be used for the patch-element metal layer. The aluminium metal layer was evaporated onto the surface using an electron beam evaporator to 1 μm thickness. The patch elements was patterned using standard lithography methods.

The antenna and transmission-line wafers were attached to each other with silver epoxy glue. Marks on both of the wafers were used insure proper alignment. Silver epoxy was also used to attach the the GaAs detector diodes to the gold pads on the substrate.

7.2.5 Return Loss Measurements

The return-loss measured in this setup is shown in Figure 7.6. From the

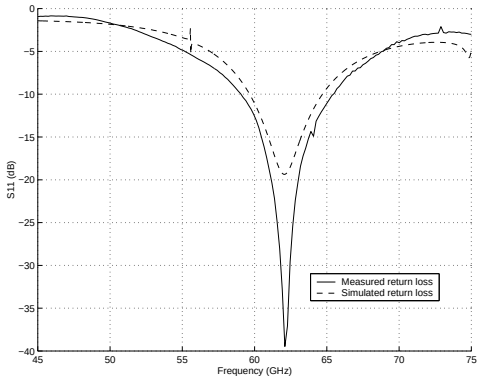

Figure 7.6: Antenna return loss

measurements it can be seen that the antenna resonates at 62 GHz. The -10 dB bandwidth of the antenna is 6 GHz.

The antenna was connected to the CPW-probe with a 2 mm long microstrip. Separate on-wafer characterization microstrip lines suggest an insertion loss less than 1 dB for this transmission line. Its impact on the return-loss measurements can therefore be expected to be small.

The attained -10 dB bandwidth of 6 GHz, centered around 62 GHz corresponds very well to the return loss simulated with HFSS. The bandwidth is comparable to published results for similar antenna structures [29]. No measurements of the radiation efficiency have been performed, but HFSS simulations indicate 77% efficiency.

7.2.6 Radiation Pattern Measurements

The radiation pattern was measured at a frequency of 64.56 GHz. This frequency was chosen because a strong readout from the diode detector was obtained for this frequency. It is also within the -10 dB tuning range of the antenna.

The radiation pattern measurements for the vertical E-plane and horizontal H-plane is shown in figure 7.7 along with a HFSS simulation of the radiation pattern. A 50 degree half-power beamwidth is obtained in the

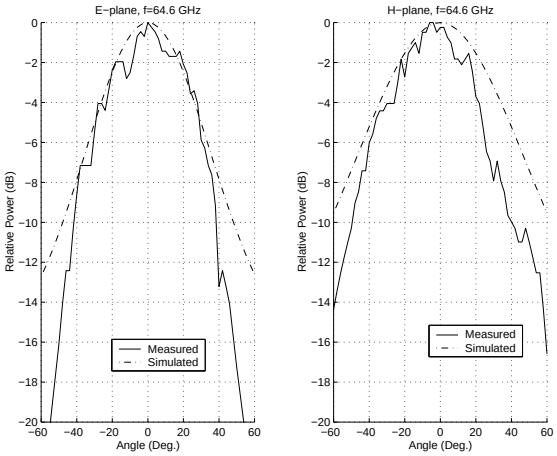

Figure 7.7: Antenna E– an H-plane radiation pattern

E-plane. In the H-plane the half-power beam-width was measured to only 45 degrees. However, a standing-wave minima accounts for a drop in the received power at an 25 degree angle from the normal of the antenna plane.

This standing-wave is caused by reflections between the antenna under test and the reference horn antenna.

The radiation pattern measured shows good agreement with the simulated results, even though the H-plane measurements indicate a premature drop-off in the radiation pattern at posivitive angles. This deviation from the simulated results is most likely caused by the extremely short distance between the antenna under test and the reference antenna. The short distance was mandated by the low sensitivity of the diode detector. The true half-power beamwidth is most likely closer to the simulated 60 degrees than the measurements suggest.

The radiation pattern measurements, as well as the HFSS simulations of the antenna, were made with the antenna backed by a very large ground-plane (in terms of wavelengths). In a practical implementation the ground-plane would have to be considerably smaller, thus increasing the beamwidth of the antenna.

7.3 Modelling of Differential 24 GHz Patch Antenna

An alternative approach to the use of stacked micromachined wafers to decouple the patch from the silicon substrate is offered by above-IC processes using BCB as a spin on dielectric layer. The maximum thickness of 20-30 μm for the BCB dielectric layer does however limit the attainable bandwidth. A differentially fed patch antenna, realized on a 30 μm thick BCB layer, is shown in Fig. 7.8. The antenna has been modelled [33] in collaboration with the designers at the University of Ulm. One advantage of the differential feed is the elimination of any connection to the patch ground-plane as well as compatibility with differential active circuits. The antenna length L_P, which governs the resonance frequency, was chosen to be 3848 μm which corresponds to slightly less than a half of a guided wavelength in the microstrip transmission line formed by the patch. The patch width W_P, which determines the patch impedance, was selected to 1928 μm. The differential feed lines were connected to the side of the patch at a distance W_f of 270 μm. The distance between the feed points determines the antenna input impedance. To predict the impact of the different antenna dimensions on the antenna impedance and return loss a transmission line model, based on standard patch antenna models [15], was developed. The modified version of the model is shown in Fig. 7.9, where the differential shunt feed is included. The combined length of the transmission lines $TL1$, $TL2$ and $TL3$ in the

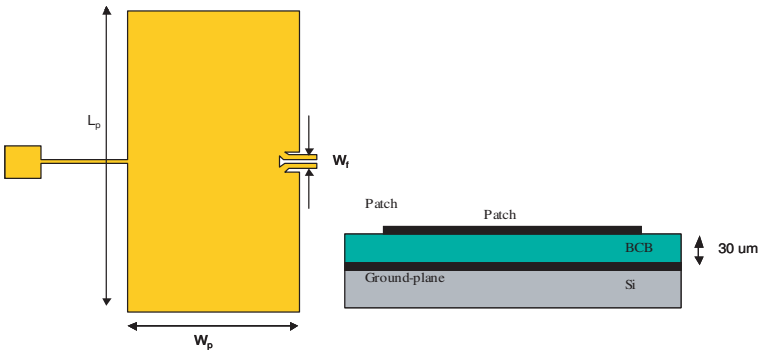

Figure 7.8: Differentially fed patch antenna on BCB layer

transmission line model corresponds to the total length L_p of the patch and the length of section $TL2$ to the distance W_f between the antenna feed points.

The measured and modeled antenna return loss is shown in Fig. 7.10. Good agreement is obtained between the transmission line model and measured results. By shortening the length L_P of the patch antenna resonance at 24 GHz can be obtained. The tuning of the patch is critical since the antenna has a small bandwidth. The simulated antenna directivity is 7 dBi.

7.4 Summary

Patch antennas offer the possibility of integrating high gain antennas with small backlobes but the antenna itself is too space consuming to be integrated directly on the semiconductor die at 24 GHz. An alternative is offered by wafer level integration where the active devices are mounted to a larger wafer, and the antennas and other passive circuit elements are implemented on the passive wafer. The problem of connecting differential active devices to patch antennas, particular if no metallic contact to the patch ground plane is available, is addressed by the presented differentially driven patch. A modified transmission line model is successfully derived for the implemented patch.

At 60 GHz the patch size is reduced to a value where integration directly on chip could be considered. The stacked wafer, aperture coupled patch demonstrated yields a high gain antenna with a bandwidth sufficient to cover the 59 to 64 GHz frequency range.

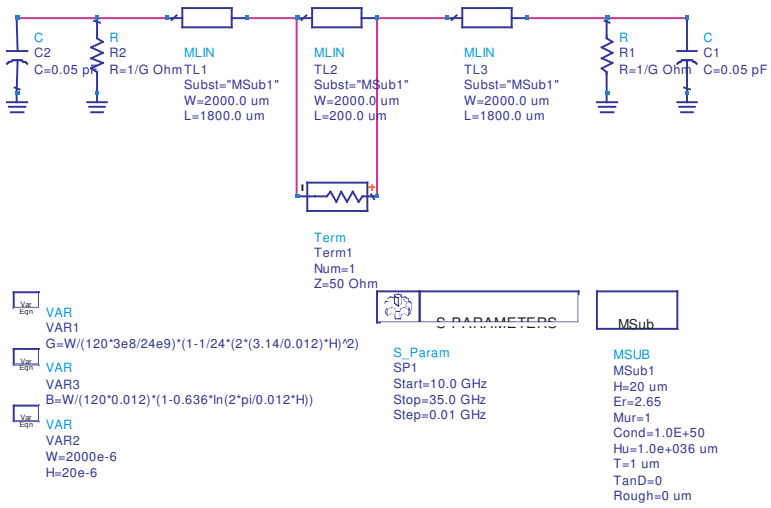

Figure 7.9: Transmission line model of differentially fed patch antenna (the substrate and antenna dimensions described in the text were used for the implemented antenna and final model)

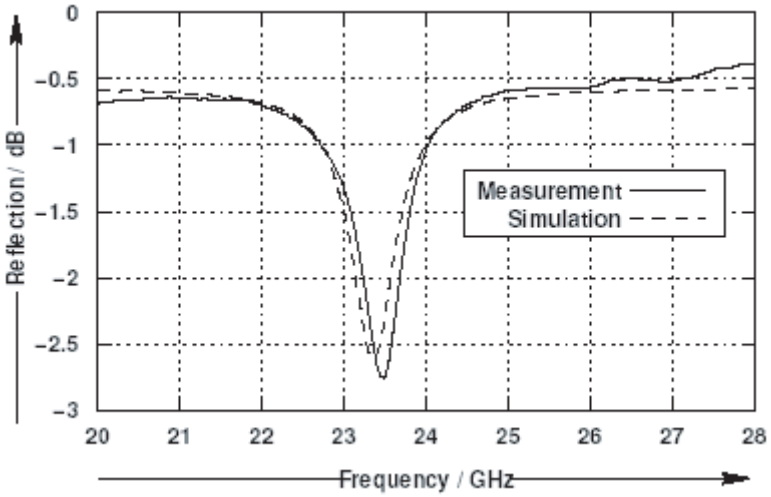

Figure 7.10: Return loss measurements and transmission line model of a differentially fed patch antenna realized on a 30 μm thick BCB layer

Chapter 8

Crosstalk

8.1 Introduction

In the suggested integration method the active transceiver circuit is to be placed close to the antenna, for instance within the perimeter of a slot loop antenna, and could therefore be subject to cross-talk. Crosstalk between the antenna and the circuits could cause instability in amplifiers and increase the phase-noise of oscillators.

Since the transceiver circuit will be placed in the near-field region of the antenna, we need to separately analyze the E- and H-fields coupling mechanisms contributing to crosstalk. In this chapter cross talk of an integrated slot-loop antenna in the Atmel SiGe process is treated, but some of the results are also applicable to other on-chip slot antennas and similar processes.

8.2 Simulation of crosstalk

Cross talk for simple on chip wire interconnects have been simulated using HFSS [23] The simulation setup is shown in Figure 8.1. The test structures consist of 200 μm long 50 Ω microstrip lines placed between a 6 μm thick oxide of the semiconductor process and the 20 μm thick post processed BCB layer. A local ground-plane is introduced under each microstrip line at the same level as the conductive p+ channel stopper layer. The test microstrip lines are terminated in each end with localized ports.

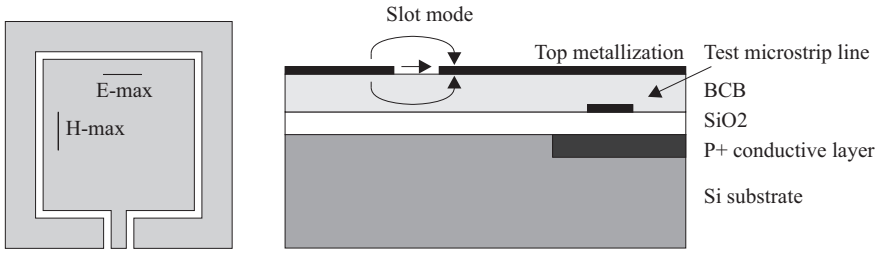

Figure 8.1: Cross-talk simulation setup

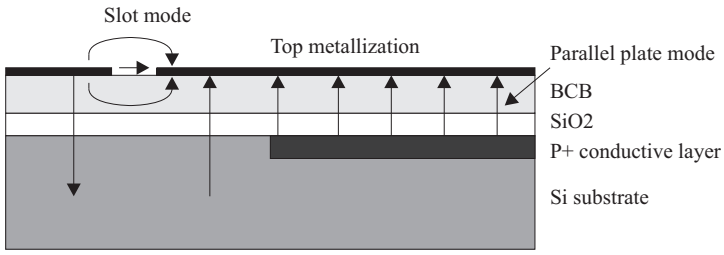

Figure 8.2: Parallel plate mode exitation

8.2.1 Solid antenna ground-plane

In the standard slot loop antenna a solid ground-plane is used in the center of the antenna. If the slot antenna is manufactured with the BCB post-processing method presented a solid ground-plane is formed above the integrated transceiver. The presence of a ground-plane would directly influence the operation of the lumped components used in the transceiver design, for example due to capacitive loading or inductive coupling to the spiral inductors. More importantly, the antenna ground-plane in conjunction with the p+-channel stopper forms a parallel-plate waveguide as shown in Figure 8.2. Leakage between the slot mode and parallel-plate mode can significantly contribute to cross-talk.

8.2.2 Finite ground-plane

To avoid the excitation of parallel plate modes, an opening can be made in the antenna ground plane metallization over the active circuit area in the center of antenna, thereby removing one of the conductors in the parallel-plate waveguide. Such a modification of the slot antenna ground-plane will

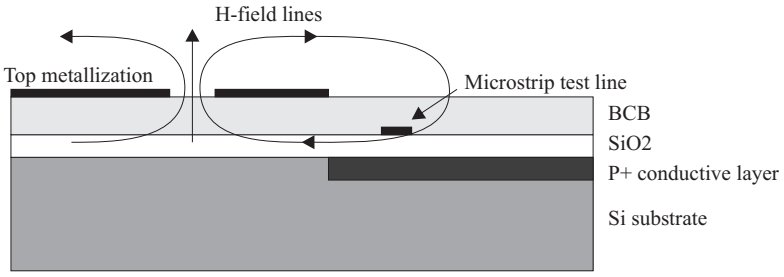

Figure 8.3: H-field near field coupling with finite groundplane

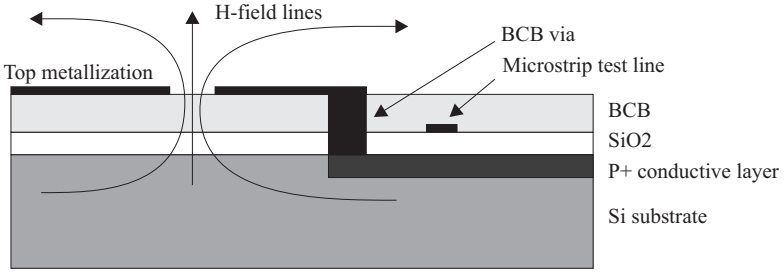

Figure 8.4: E- and H-field configuration, with the antenna ground-plane connected to p+ circuit ground.

lead to a reduced antenna radiation resistance due to the modified current distribution in the ground-plane, and also introduce new coupling mechanisms.

Close to the voltage maxima capacitive coupling from the edge of the finite ground-plane to transmission lines in transceiver circuit can occur. The magnetic coupling to the transceiver transmission lines and spiral inductors also increase, since the H-field can form closed loops around the finite ground-plane conductor as outlined in Figure 8.3.

8.2.3 Connection of the finite ground-plane to p+ channel stopper layer

The p+ channel stopper layer in the active circuit can be connected to the finite ground plane of the antenna using via holes through the BCB dielectric as shown in Figure 8.4. The connection restores a solid ground-plane in the center of the antenna and forces the normal component of the H-field at the

semiconductor surface to be zero, thus significantly reducing the coupling at the current maxima. The capacitive coupling close to the voltage maxima is eliminated as well.

8.2.4 Comparison of cross-talk with different grounding

The simulated cross-talk is plotted for test transmission lines close to electric maximums in Figure 8.5 and curent maximums in Figure 8.6.

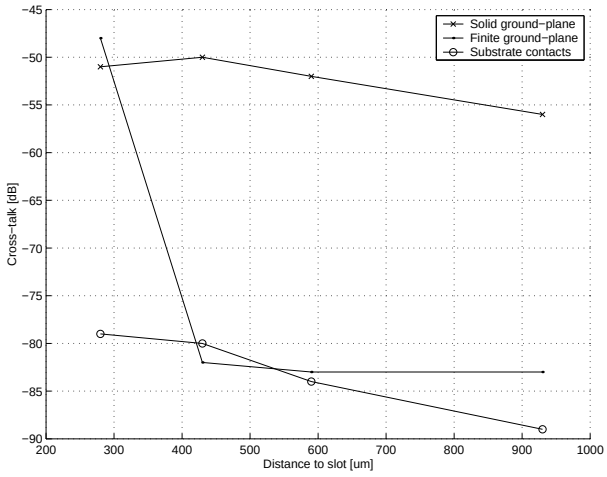

Figure 8.5: Simulated cross-talk at different distances from voltage maxima

As can be seen from the graphs, the level of crosstalk is significantly reduced if part of the solid ground-plane in the center of the slot loop is removed. Further reduction is obtained if the truncated ground-plane is connected to the channel stopper layer.

8.3 Conclusion

Crosstalk between an on-chip slot loop antenna and simple wire interconnects commonly used in the design of active SiGe circuits has been simulated. Although the simulations have not yet been verified by measurements, they suggest that active circuits can be successfully integrated close to the antenna, provided that steps are taken to reduce the crosstalk.

Elimination of potential parallel plate modes between the post processed antenna metallization and ground-planes present in the active device area

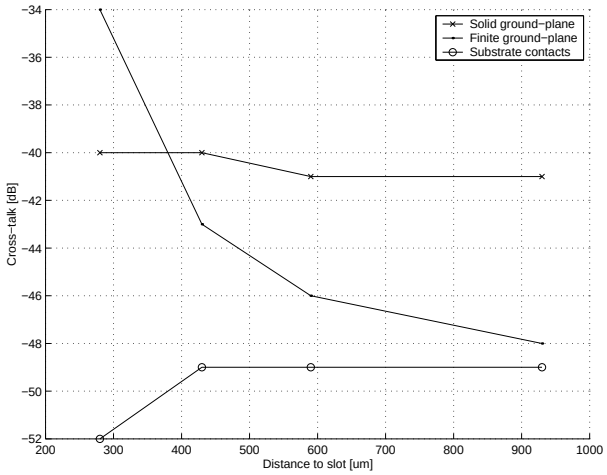

Figure 8.6: Simulated cross-talk at different distances from current maxima

yields a substantial improvement in cross-talk.

Further work is needed to verify the coupling to spiral inductors as well as bond wires. Other antenna types such as dipoles and loop antennas should also be analyzed.

Chapter 9

Packaging

9.1 Introduction

The micromachined antennas presented in this thesis are fragile and need to be protected to survive normal handling in a production environment. One way of packaging such a chip is to fully enclose it in a hermetically sealed cavity, using a standard ceramic package. The cavity and the ceramic covering of the chip would have to be designed to be transparent to the antenna and avoid any packaging resonances.

A low cost alternative to the full hermetical seal provided by a ceramic package is to only use a ceramic or organic carrier substrate and cover the chip with its integrated antenna with an organic glob-top material.

The substrate can be a LTCC (Low Temperature Co-fired Ceramic) carrier or a standard FR-4 substrate. The LTCC could be used for low-frequency interconnects to the chip with its integrated antenna as well as a carrier substrate for an independent module.

In Figure 9.1 glob-top packaging with a LTCC base substrate is illustrated. Since both the carrier substrate and the glob top material will be in close proximity or in direct contact with the antenna the dielectric properties of the packaging materials need to be evaluated.

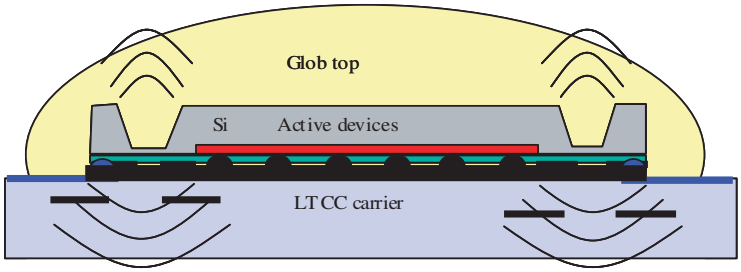

Figure 9.1: Glob top packaging

9.2 Evaluation of Ferro A6-S LTCC as a Carrier Substrate

The Ferro A6-S LTCC material has been evaluated for use at 24 GHz. Test structures consisting of microstrip ring resonators have been designed and implemented on single and dual layer LTCC, corresponding to 100 μm and 200 μm dielectric thicknesses. The test structure is shown in Figure 9.2. The mean circumference of the ring resonator was calculated by finding the effective dielectric constant ε_{eff} of the microstrip line using manufacturers supplied data ε_r=5.9 and the closed form approximation [34].

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12h/W_{ms}}} \tag{9.1}$$

The microstrip resonators were designed to have their second resonance at 24 GHz, corresponding to a total resonator length of one guided wavelength and a circumference of $l_r = 5843$ μm. The ground-plane was placed one layer down in the LTCC stack, corresponding to a microstrip dielectric thickness of 100 μm. A resonator and feed line impedance of 50 Ohm was selected and a microstrip width $W_{ms} = W_r = 141$ μm calculated. A second test structure was designed with double tape thickness, and a microstrip width of $w_{ms} = w_r = 288$ μm was chosen for 50 Ohm impedance. The ring resonators were lightly coupled to the microstrip feed lines by 100 μm wide gaps. An effective microstrip dielectric constant ε_{eff}=4.32 for the single layer resonator was calculated from the resonator dimensions and a measured resonance at 24.67 GHz. The value is in good agreement with the 4.3-4.4 range reported in literature [35] and the value 4.34 obtained using the closed form

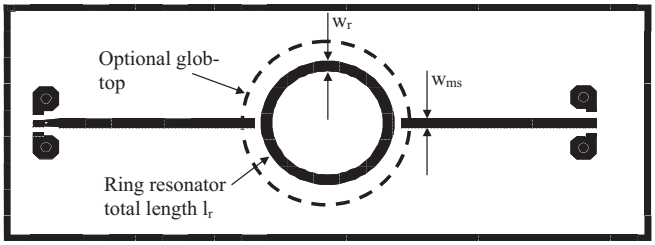

Figure 9.2: LTCC ring resonator characterization structure

microstrip approximation, thus indicating that the dielectric data provided by the manufacturer is accurate at 24 GHz.

9.3 Characterization of Glob-top Materials

The introduction of a glob top and dielectric carrier substrate will increase the effective dielectric constant seen by the on-chip antenna and thus change its tuning frequency and input impedance at resonance. Due to the introduction of a number of interfaces between different dielectric materials in the packaging, the effective dielectric surrounding the antenna cannot be easily calculated. The integrated antenna should therefore be simulated together with the selected packaging using a full-wave simulation tool to verify correct operation at the desired frequency.

Manufacturer provided dielectric data of a number of common glob-top, cavity-fill and under-fill materials are presented Table 9.1. As indicated by the frequency of characterization the data provided is however not directly applicable to high frequency applications.

Glop-top	Type	$tan\delta$	ε_r
Amicon S 7503	Silicone	0.0005 /1 kHz	3.1
Semicosil 900LT	Silicone	0.005 /50 Hz	3.0
Lord CircuitSaf ME-455	Epoxy cav. fill	0.006 /1 MHz	3.37
Lord CircuitSaf ME-430	Epoxy glob top	0.006 /1 MHz	3.77
Namics XV6841-0209	Side fill	0.008 /1 MHz	3.75

Table 9.1: Evaluated glob-top materials and manufacturers data

In order to screen the high frequency properties of the glob-top and fill

materials the ring resonators used for characterization of the Ferro-A6S material were covered with globs of the selected materials. The thickness of the glob was 0.5-1.0 mm. The change in resonance frequency and Q-value of the covered resonators is shown in Table 9.2 for resonators of single and double LTCC tape thickness.

Glop-top	f_r1	f_r2	Q1	Q2
No glob top	24.67	24.85	95	75
Amicon S 7503	23.14	23.44	75	50
Semicosil 900LT	23.41	23.98	67	65
Lord CircuitSaf ME-455	22.84	23.26	95	72
Lord CircuitSaf ME-430	22.66	22.87	95	67

Table 9.2: Measured ring resonator resonance frequencies and quality factors for single (x1) and double (x2) LTCC tape thickness

As can be seen from the tabulated data, the quality factor of the resonators is hardly affected for the epoxy based Lord CircuitSaf materials which only yield minor degradation in Q-values for the double layered resonator. The silicone based Amicon and Semicosil yield larger reduction in resonator quality factor and can thereby be expected to have higher losses also when used as antenna encapsulants.

9.4 Conclusion

Packaging solutions for monolithic circuits with integrated antennas need to consider the dielectric loading of the integrated antenna. Glob-top packaging using a ceramic carrier substrate like LTCC can be used to provide a low cost package where the dielectric properties are well defined.

The dielectric constant of a common LTCC material has been verified at 24 GHz. Microstrip ring resonators yielding Q-values close to 100 indicate low losses in the Ferro A6 dielectric as well as the silver metallization process used.

Glob tops and cavity fill materials have been screened for use at 24 GHz. Of the evaluated glob-tops epoxy based ones provide lower losses than materials based on silicone compounds.

Future work is needed to verify the electrical as well as mechanical properties of glob-top packaged micromachined antennas. The dielectric properties of the package will have to be considered during the design of the antenna.

The optimum routing of low frequency signal lines and bond wires in the package should also be determined.

Chapter 10

Discussion and future work

10.1 Discussion

This thesis has presented a number of different antenna candidates for integration with active devices on micromachined silicon substrates. Most of the antennas, except the patches, provide similar performance in terms of gain and bandwidth. In this section some of the unique properties of each antenna type will be highlighted.

The slot antenna has traditionally been the preferred antenna type for integration with active devices, since its uniplanar properties facilitate planar interconnections. The slot antenna is also compatible with the circuit ground-shield metallization commonly used in SiGe circuit designs. Slot antennas can be designed as slot-loops and U-slots in order to adapt the geometry to the typical square shaped silicon die. Another advantage of the slot antenna is the ability to implement low loss passive slot-line and CPW matching structures on micromachined membranes. Among the disadvantages of the slot antenna the difficulty of integration with differential circuits demanding an balanced antenna feed can be noted.

Dipole and loop antennas offer a balanced feed, which is inherently compatible with differential circuit designs. The full wave loop is more space consuming than the meandered dipole but yields a higher radiation resistance. Both dipoles and loop antennas are sensitive to nearby metallic objects present on the chip and should therefore be co-designed with the active circuit metallization.

The inverted-F antenna is a compact antenna type, which utilizes the ground-plane provided by the circuit metallization as a counterpoise. Both

the driven inverted F element and the small ground-plane does however contribute to the total radiation of the antenna, thus reducing the polarization purity and giving poor control over the interaction with the bond wires.

Patch antennas are useful for wafer level integration approaches since they provide high gain and small back-lobes. The main disadvantage of the patch antenna is its comparatively large size, making it unsuitable for on-chip integration with active components. The attainable bandwidth is also small if the patch is implemented on thin dielectric such as a spin-on BCB layer.

10.2 Future Work

The results presented in this thesis represents a work in progress, and there are tasks remaining in several areas.

The micromachined antennas, especially the slot antennas, need to the carefully characterized and the impact of the silicon substrate fully analyzed.

On-chip cross-talk, particulary antenna interaction with bond-wires and on-chip spiral inductors, should be experimentally verified and modeled.

Glob-top packaging of micromachined antennas should be studied and the dielectric loading of the on-chip antenna determined.

Antenna measurements techniques could be improved. Radiometric methods, allowing accurate determination of antenna efficiency, would be useful for quantifying the improvement yielded by the micromachining of the antennas. Alternative ways of feeding the antenna during radiation pattern measurements could also be devised, thereby eliminating the problem of the wafer probe interfering with the measurements.

Appendix A

Antenna Measurement Setup

The measurement of standard antenna parameters such as return loss, gain and radiation pattern for integrated antennas poses several difficulties, mainly due to the small physical size of the antennas and the requirement for wafer probing as the only means of connecting to the antenna.

A.1 Return Loss and Impedance Measurements

The return loss measurements were made with an ordinary wafer-probing system adapted as described by Roy *et al* [36] to comply with the radiating properties of an antenna. As shown in figure (A.1) this is done by letting the antenna radiate downwards into a 5 cm thick sheet of low permittivity Styrofoam. This material protects the antenna from dielectric loading and provide a region large enough for the far-field to develop. Underneath the styrofoam a 11 cm thick RF-absorber (Ecosorb AN-79) was placed to prevent waves being reflected back from the metal base plate of the probe station. The network analyzer is SOLT (Short Open Load Through) calibrated with the reference plane at the CPW probe tips using a Cascade ISS calibration substrate.

A.2 24 GHz Gain and Radiation Pattern Setup

The radiation patterns have been measured on wafer with the setup shown in Figure A.2. As in the case of the return loss measurement the antenna is placed on a ROHACELL foam sheet to allow free space radiating conditions. Diced antenna chips and antennas on wafer can be measured, but the probe

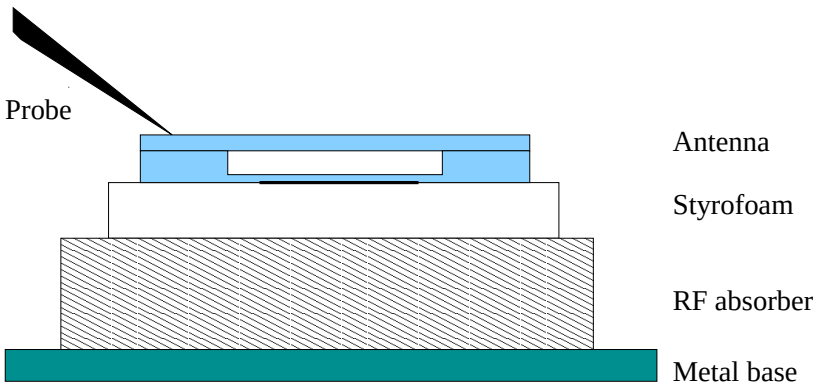

Figure A.1: Antenna return loss messurements

arm shadows the antenna at certain angles.

The antenna gain has been measured by the substitution principle. Two Flann model 20240-20 20 dBi 18-26.5 GHz standard gain horn antennas have been mounted at a distance of 55 cm and connected to an Anritsu 360B vector network analyzer (VNA). After calibration of the VNA one of the horn antennas has been replaced by the antenna under test (AUT). The AUT has been placed at the same position as the aperture of the horn antenna and the difference in insertion loss measured by the VNA has been recorded. The gain of the AUT has been calculated by subtracting the tabulated gain of the standard gain horn antenna at the frequency of measurement.

Possible error sources in the measurement include the coaxial to waveguide transition of the gain reference horn antenna used for calibration and the GSG wafer probe used to contact the AUT. The insertion loss of the transition has been checked by measuring two transitions back to back. The insertion loss was found to be less than 0.5 dB.

A.3 60 GHz Radiation Pattern Setup

The antenna is mounted on a metal fixture in an anechoic chamber as shown in figure (A.3). The antenna was positioned 20 cm from a 20 dBi reference horn antenna connected to the frequency extender. The output power of the extender is approximately 8 dBm. The output signal from the extender was pulsed with a 1 kHZ square-wave signal (100% AM-modulation or *on-off keying*).The detector diode was supplied with 0.34 mA bias current through a high impedance current source to obtain optimum sensitivity. An AC-

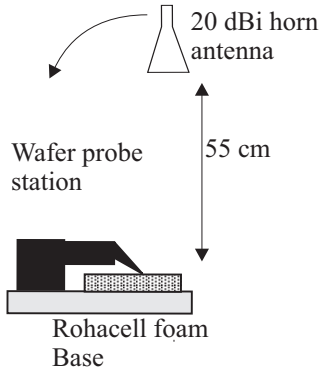

Figure A.2: Probe station pattern measurement setup

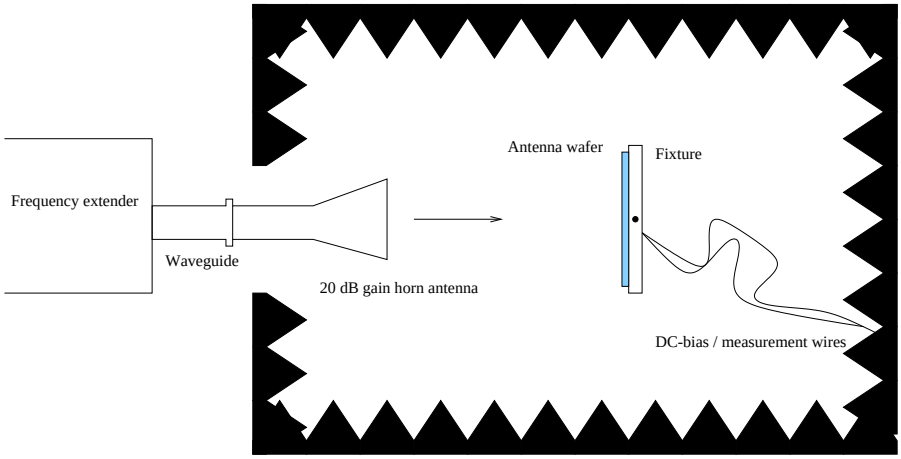

Figure A.3: Antenna in anechoic chamber

millivoltmeter was connected parallell to the diode. The detected 1 kHz signal is proportional to the power detected by the diode according to diode square-law detection.

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