UPPSALA
UNIVERSITET

Integrated Antennas

Monolithic and Hybrid Approaches

ERIK ÖJEFORS

Dissertation presented at Uppsala University to be publicly examined in Siegbahnsalen, Ångströmlaboratoriet, Uppsala, Friday, October 13, 2006 at 10:15 for the degree of Doctor of Philosophy. The examination will be conducted in English.

Abstract
Öjefors, E. 2006. Integrated Antennas. Monolithic and Hybrid Approaches. Acta Universitatis Upsaliensis. *Digital Comprehensive Summaries of Uppsala Dissertations from the Faculty of Science and Technology* 221. 69 pp. Uppsala. ISBN 91-554-6651-6.

This thesis considers integration of antennas and active electronics manufactured on the same substrate. The main topic is on-chip antennas for commercial silicon processes, but hybrid integration using printed circuit board technology is also addressed.

The possible use of micromachining techniques as a means of reducing substrate losses of antennas manufactured on low resistivity silicon wafers is investigated. Compact dipole, loop, and inverted-F antennas for the 20-40 GHz frequency range are designed, implemented, and characterized. The results show significantly improved antenna efficiency when micromachining is used as a post-processing step for on-chip antennas manufactured in silicon technology.

High resistivity wafers are used in a commercial silicon germanium technology to improve the efficiency of dipole antennas realized using the available circuit metal layers in the process. Monolithically integrated 24 GHz receivers with on-chip antennas are designed and evaluated with regard to antenna and system performance. No noticeable degradation of the receiver performance caused by cross talk between the antenna and the integrated circuit is observed.

For low frequency antenna arrays, such as base station antennas, hybrid integration of active devices within the antenna aperture is treated. A compact varactor based phase shifter for traveling wave antenna applications is proposed and evaluated. Electrically steerable traveling wave patch antenna arrays, with the phase shifters implemented in the same conductor layer as the radiating elements, are designed and manufactured in microstrip technology. It is experimentally verified that the radiation from the feed network and phase shifters in the proposed antenna configuration is small.

Keywords: antenna travelling wave arrays, antenna phased arrays, phase shifters, micromachining, silicon, monolithic microwave integrated circuits, dipole antennas, loop antennas, slot antennas

Erik Öjefors, Department of Engineering Sciences, Box 534, Uppsala University, SE-75121 Uppsala, Sweden

To my parents

List of Papers

This thesis is based on the following papers, which are referred to in the text by their Roman numerals.

I **Öjefors, E.**, Bouchriha, F., Grenier, K., Rydberg, A. (2003) 24 GHz ISM-Band Antennas on Surface Micromachined Substrates for Integration with a Commercial SiGe Process. *Proc. of the 6th European Conference on Wireless Technology,* Munich, Oct. 2003, 101-104.

II **Öjefors, E.**, Bouchriha, F., Grenier, K., Rydberg, A., Plana, R. (2004) Compact Micromachined Dipole Antenna for 24 GHz Differential SiGe Integrated Circuits. *Proc. of the 34th European Microwave Conference,* Amsterdam, Holland, Oct. 2004, 1081-1084.

III **Öjefors, E.**, Sönmez, E., Chartier, S., Lindberg, P., Rydberg, A., Schumacher, H. (2005) Monolithic Integration of an Antenna with a 24 GHz Image-Rejection Receiver in SiGe HBT Technology. *Proc. of the 35th European Microwave Conference,* Paris, France, Oct. 2005.

IV **Öjefors, E.**, Grenier, K., Mazenq, L., Rydberg, A., Plana, R. (2005) Micromachined Inverted F Antenna for Low Resistivity Silicon Substrates. *IEEE Microwave and Wireless Components Letters*, 2005, 15(10): 627 - 629.

V **Öjefors, E.**, Kratz, H., Grenier, K., Plana, R., Rydberg, A. (2005) Micromachined Loop Antennas on Low Resistivity Silicon Substrates. *Accepted for publication in IEEE Transactions on Antennas and Propagation.*

VI **Öjefors, E.**, Sönmez, E., Chartier, S., Lindberg, P., Schick, C., Rydberg, A., Schumacher., H (2005) Monolithic Integration of a Folded Dipole Antenna with a 24 GHz Receiver in SiGe HBT Technology. *Submitted to IEEE Transactions on Microwave Theory and Techniques.*

| VII | Cheng, S., **Öjefors, E.**, Hallbjörner, P., Rydberg, A. (2006) Compact Reflective Microstrip Phase Shifter for Traveling Wave Antenna Applications. *IEEE Microwave and Wireless Components Letters*, 2006, 16(7):431 - 433. |

| VIII | **Öjefors, E.**, Cheng, S., From, K., Skarin, I., Hallbjörner, P., Rydberg, A. (2005) Electrically Steerable Single-Layer Microstrip Travelling Wave Antenna With Varactor Diode Based Phase Shifters. *Submitted to IEEE Transactions on Antennas and Propagation*. |

Comments on the author's contribution to the papers

| I | Planning, design and simulation of the antenna, measurements, writing the manuscript. |

| II | Planning, design and simulation of the antenna, measurements, writing the manuscript. |

| III | Planning, design and simulation of the integrated antenna, antenna measurements, system characterization, writing the manuscript. |

| IV | Planning, design and simulation of the antenna, measurements, writing the manuscript. |

| V | Planning, design and simulation of the antenna, measurements, writing the manuscript. |

| VI | Planning, design and simulation of the integrated antenna, antenna measurements, receiver characterization, writing the manuscript. |

| VII | Major part of planning, part of design, manufacturing and measurements. |

| VIII | Major part of planning, traveling wave model, patch impedance matching method, part of manufacturing and measurements, non-linearity characterization, writing the manuscript. |

Reprints were made with permission from the publishers.

Related Papers

The following papers have not been included due to overlap or because the content is outside the scope of this thesis.

i   Rydberg, A., **Öjefors, E.** (2004) Monolithic Antennas. In *Encyclopedia of RF and Microwave Engineering, ed. Kai Chang*, John Wiley and Sons, 2004.

ii   Lindberg, P., **Öjefors, E.** (2006) A Bandwidth Enhancement Technique for Mobile Handset Antennas Using Wavetraps. *IEEE Transactions on Antennas and Propagation*, 2006, 54(8): 2226 - 2233.

iii   Kratz, H., **Öjefors, E.**, Stenmark, L. (2006) Micromachined S-Band Patch Antenna with Reduced Dielectric Constant. *Sensors and Actuators A: Physical.* 2006, 130-131: 478-484.

iv   Hallbjörner, P., Bergström, M., Boman, M., Lindberg, P., **Öjefors, E.**, Rydberg, A. (2005) Millimetre-wave Switched Beam Antenna using Multiple Travelling-wave Patch Arrays. *IEE Proceedings - Microwaves, Antennas and Propagation*, 2005, 152:551-555.

v   Lindberg, P., **Öjefors, E.**, Rydberg, A. (2006) Wideband Slot Antenna for Low-Profile Hand-held Terminal Applications. *Proc. of the European Microwave Conference 2006*, Manchester, UK, Sept. 2006.

vi   Andersson, M., Göransson, B., Skarin, I., From, K., Cheng, S., **Öjefors, E.**, Hallbjörner, P., Manholm, L., Rydberg, A. (2006) Antennas with Fast Beamsteering for High Spectral Efficiency in Broadband Cellular Systems. *Proc. of the European Conference on Wireless Technology 2006*, Manchester, UK, Sept. 2006.

vii   Cheng, S., **Öjefors, E.**, Hallbjörner, P. Rydberg, A. (2005) Varactor Diode Phase Shifters for Electrically Steerable Microstrip Travelling Wave Antennas. *Proc. of Antenna 2006,*

Linköping, Sweden, May 2006.

viii   Lindberg, P., **Öjefors, E.**, Rydberg, A. (2005) A 24 GHz On-chip Differential Wilkinson Coupler Using Lumped Components. *Proc of GigaHertz 2005,* Uppsala, Sweden, Nov. 2005.

ix   Lindberg, P., **Öjefors, E.**, Rydberg, A. (2005) A SiGe 24 GHz Monolithically Integrated Direct Conversion Receiver. *Proc of GigaHertz 2005,* Uppsala, Sweden, Nov. 2005.

x   Lindberg, P., **Öjefors, E.**, Rydberg, A. (2005) LTCC Packaging for a 26 GHz SiGe Receiver. *Proc of GigaHertz 2005,* Uppsala, Sweden, Nov. 2005.

xi   Grenier, K., Mazenq, L., Dubuc, D., Bouchriha, F., Cocetti, F., **Öjefors, E.**, Lindberg, P., Rydberg, A., Berntgen, J., Rabe, W.J., Sönmez, E., Abele, P., Schumacher, H., Plana, R., (2005) IC Compatible MEMS Technologies. *Proc. of the 35th European Microwave Conference,* Paris, France, Oct. 2005.

xii   Lenkkeri, J., Juntunen, E., Lindberg, P., **Öjefors, E.**, Rydberg, A. (2005) Packaging Issues of 24 GHz Traffic Control Radar Front End Based on SiGe and LTCC Technologies. *Proc. of IMAPS Nordic Conference*, Tönsberg, Norway, Sept. 2005.

xiii   Lindberg, P., Rydberg, A., **Öjefors, E.** (2005) Micromechanically Enhanced Integrated Radar Front-Ends. *Proc. of International Conference on Electromagnetics in Advanced Applications*, Torino, Italy, Sept. 2005.

xiv   Grenier, K., Mazenq, L., Dubuc, D., **Öjefors, E.**, Lindberg, P., Rydberg, A., Berntgen, J., Rabe, W.J., Sönmez, E., Abele, P., Schumacher H., Plana, R. (2005) MEMS Above IC Technology Applied to a Compact RF Module. *Invited paper at the SPIE Microtechnologies for the New Millennium,* Sevilla, Spain, May 2005.

xv   Stenson, J., Lindberg, P., **Öjefors, E.**, Rydberg, A., (2005) Small Conformal 3D antenna for Integration in Medical Sensor. *Proc. of the 4th European Workshop on Conformal Antennas*, Stockholm, Sweden, May 2005.

xvi   **Öjefors, E.**, Kratz, H., Rydberg, A., (2005) Membrane Antenna for Silicon Based 3D Integrated Microsystems. *MEMSWAVE 2005 Workshop*, Lausanne, Switzerland, June 2005.

xvii Lindberg, P., **Öjefors, E.**, Sönmez, E., Rydberg, A. (2004) A SiGe HBT 24 GHz Sub-harmonic Direct-Conversion IQ Demodulator. *IEEE Topical Meeting on Si Monolitic ICs in RF Systems,* Atlanta, USA, Sept. 2004.

xviii Busquere, J.P., Do, N., Bougriha, F., Pons, P., Grenier, K., Dubuc, D., Boukabache, A., Schumacher, H., Abele, P., Rydberg, A., **Öjefors, E.**, Ancey, P., Bouche G., Plana, R. (2004) MEMS SiGe Technologies for Advanced Wireless Communications. *Proc. of the IEEE Radio Frequency Integrated Circuits (RFIC) Systems,* Fort Worth, TX, USA, June 2004, 247-250.

xix **Öjefors, E.**, Rydberg, A. (2004) Micromachined On-Chip Loop Antennas for 24 GHz Short-range Communication Devices. Proc. of the *COST 273/284 Workshop,* Gothenburg, Sweden, June 2004.

xx **Öjefors, E.**, Rydberg, A. (2004) Micromachined 24 GHz Antennas on Low Resistivity Silicon. *Proc. of the 5th Workshop on MEMS for Millimeterwave Communications (MEMSWAVE),* Uppsala, Sweden, June 2004.

xxi Lindberg, P., **Öjefors, E.**, Rydberg, A. (2003) A SiGe 24 GHz Zero-IF Downconverter. *Proc. of GigaHertz 2003,* Linköping, Sweden, Nov. 2003.

xxii **Öjefors, E.**, Rydberg, A. (2003) LTCC and Glob-top Packaging for 24 GHz MMIC with Integrated Antennas. *Proc. of GigaHertz 2003*, Linköping, Sweden, Nov. 2003.

xxiii Abele, P., **Öjefors, E.**, Schad. K.B., Sönmez, E., Trasser, A., Konle, J., Schumacher, H. (2003) Wafer Level Integration of a 24 GHz Differential SiGe-MMIC Oscillator with a Patch Antenna using BCB as a Dielectric Layer. *Proc. of the 33rd European Microwave Conference,* Munich, Germany, Oct. 2003.

xxiv Lindeberg, M., **Öjefors, E.**, Rydberg, R., Hjort, K., (2003) 30 GHz LITZ Wires Defined by Ion Track Lithography. *Proc. of 12th International Conference on Transducers, Solid-State Sensors, Actuators and Microsystems,* June 2003, 887-890.

xxv Urazghildiiev, I., Ragnarsson, R., Wallin, K., Rydberg, A., Ridderström, P., **Öjefors, E.** (2002) A Vehicle Classification System based on Microwave Radar Measurements of Height

9

Profiles. *Proc. of RADAR 2002*, Edinburgh, UK, Oct. 2002.

xxvi **Öjefors, E.**, Rydberg, A., Lindeberg, M., Hjort, K., (2002) On the Integration of a Compact 24 GHz Antenna in a Commercial SiGe Process. *Proc of the 3rd Workshop on MEMS for Millimeterwave Communication (MEMSWAVE),* Heraklion, Crete, June 2002.

xxvii Kurup, D.G., Rydberg A., **Öjefors, E.** (2001) Design of Millimeterwave Micro-machined Patch Antennas for WLAN Applications using a Computationally Efficient Method. *Proc. of the 31th European Microwave Conference*, London, UK, Sept. 2001.

xxviii **Öjefors, E.**, Lindblom, J., Rydberg, A., Kurup, D.G., Bäcklund, Y., Municio, F., Ryhänen, T., Scheck, H.O. (2000) High gain Micromachined Slot-coupled Patch-antenna for 60 GHz WLAN Application. *Proc. of the 8th COST 260 Meeting on Smart Antenna Computer Aided Design & Technology*, Rennes, France, October 2000.

Contents

1. Introduction

1.1 Background

The designers of antennas for wireless communication and radar systems have traditionally taken a conservative approach to the integration and co-design of the antenna with the radio frequency front-end circuitry. Usually, the antenna has been designed separately from the electronics and manufactured in a different production technology. Standardized connectors and systems impedances have normally been used to interface the antenna to the radio electronics. However, as the operating frequency of the implemented systems increases, the complexity of the necessary packages and interconnections rises. The demand for compact low cost transceivers in short range communication and sensor applications means that the traditional design and assembly methods used in microwave and millimeter-wave technology have to be reconsidered.

Due to the progress in the field of circuit and systems design, it is feasible to fit entire receivers and transmitters on a single semiconductor chip of less than 2 mm^2 size [1], thus facilitating the design of highly compact systems utilizing several antenna elements for software beam-forming or increased system capacity. An increased number of antenna elements exacerbates the problem of finding compact, low cost solutions for the implementation of the antenna and high frequency interconnects.

Integrated antennas offer a solution for the interconnect and antenna implementation problem by placing the antenna adjacent to the radio front-end, possibly on the same semiconductor chip or printed circuit board as the electronic components. At millimeter-wave frequencies (>20 GHz) the size of simple low directivity radiators becomes comparable to typical integrated circuit sizes, thus enabling the use of on-chip antennas which completely bypass the interconnection problem as illustrated in Fig. 1.1. One application for single chip transceivers is short range communication in the licence exempt ISM (Industrial Scientific Medical) 24.05-24.25 GHz and 60 GHz frequency bands. Car radar for anti-collision and intelligent cruise control systems is another mass market application which is planned in the 24 GHz and 77-80 GHz frequency ranges.

Silicon is the dominating semiconductor material used for low frequency electronic components. However, recent advances has made silicon a viable, lost cost alternative to traditional III-V materials such as GaAs and InP also at microwave and millimeter-wave frequencies. As the silicon substrate has
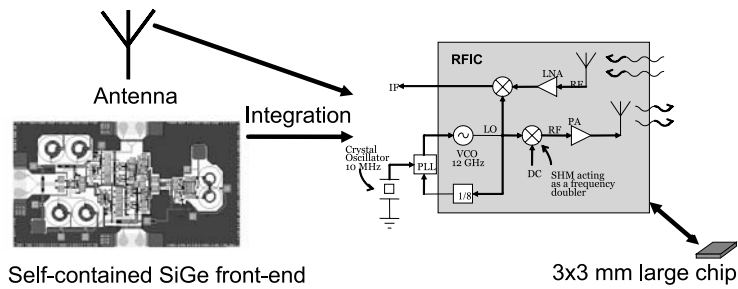
Figure 1.1: Integration of an antenna on same semiconductor die as a single chip transceiver.

higher dielectric losses than the typical III-V materials, integration of efficient on-chip antennas is difficult. For mass market applications, highly optimized space conserving designs are required as every square millimeter of wafer space increases the cost of the manufactured chip. Hence, on-chip antennas need to have a small foot-print in order to be considered practical.

In the microwave frequency range (300 MHz-20 GHz), the wavelength is normally too large to allow efficient on-chip antennas to be integrated on semiconductor substrates of reasonable sizes. However, hybrid circuits with the radiators implemented on printed circuit boards (PCB) can often be used at these frequencies since packaged discrete semiconductor components are readily available. One case where hybrid integration of antennas and electronics on the same substrate offers advantages over conventional designs is electrically steerable antennas, as shown in Fig. 1.2. Electrically steerable phased array
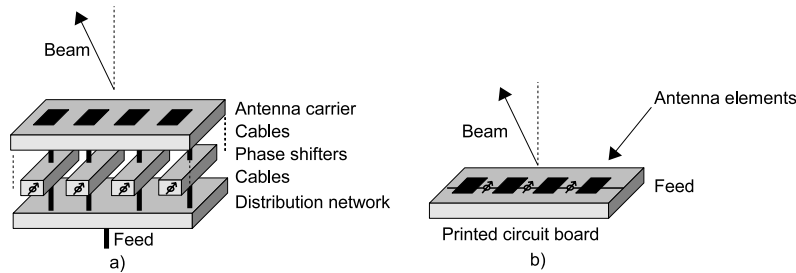
Figure 1.2: Antenna with electrically steered beam manufactured a) in conventional technology, b) with integrated electronics.

antennas are currently used in a few low volume, high value applications such as military and advanced civilian radar systems. While the benefits, such as improved capacity and range, of beam steering in wireless systems are well known the high cost and complexity of phased arrays have so far meant that the technology has not been widely used in commercial systems. By incorporating the beam steering control network on the same substrate as the radiating elements, the cost and complexity of such arrays can be reduced.

14

In the field of integrated antennas the design of radiating elements compatible with the constraints of a given environment is often the main problem which has to be considered. Restrictions of the available space are common, particular in the case of monolithic antennas. The materials used for the manufacturing of electronic components, such as semiconductor substrates, often suffer from high dielectric losses. Cross-talk between the electronic components and the radiating elements has to be minimized in order to prevent deterioration of the antenna radiation pattern or malfunctioning circuits. The aim of this thesis is to investigate methods for compact integration of antennas with active electronics such as receivers, transmitters and beam steering networks manufactured in planar technology.

1.2 Outline of the thesis

The thesis is organized as a summary, which presents the background of the work and some of the main results, and appended papers. In Chapter 2 and 3 of the summary, methods for monolithic integration of antennas in semiconductor processes are considered. Chapter 4 describes hybrid integration of electronics and radiators using planar printed circuit boards.

In Chapter 2, the use of micromachining for integration of compact antennas on low resistivity silicon substrates for the 20-40 GHz frequency band is considered. Several compact on-chip antennas, designed to be accommodated by a silicon die of typical size for integrated circuits (10 mm^2), are presented and the performance compared.

Chapter 3 describes monolithic integration of an antenna with a complete 24 GHz single chip receiver. The choice of substrate and the design of the on-chip antenna for compatibility with the receiver front-end is treated. The issue of isolation between the antenna and passive circuit elements is considered and methods of circuit design and layout for minimum crosstalk are discussed.

In Chapter 4 the design and evaluation of steerable antennas with integrated phase shifters for base station applications is treated. A novel compact phase-shifter specifically developed for traveling wave antenna applications is presented. As in the previous chapters, the active electronics is implemented in the same layer as the radiating elements.

2. Micromachined Antennas

In this chapter, compact micromachined antennas for on-chip integration with circuits manufactured in commercial Si/SiGe processes are presented. Micromachining is used to reduce the substrate losses encountered with the low resistivity silicon wafers typically used for the manufacturing of commercial Si/SiGe bipolar, BiCMOS and CMOS devices. The investigated antenna types have been designed and characterized for the 20 to 40 GHz frequency range, with 24 GHz ISM band applications primarily in mind. However, the suggested designs can be scaled to higher or lower frequencies given the limitations of practical die sizes.

2.1   On-chip antenna design considerations

In the 20 to 40 GHz frequency range, the free space wavelength of radiated signals is still relatively large compared to the typical chip sizes of integrated circuits. For short range radar sensors operating in the 24 GHz ISM-band, the free space wavelength is 12 mm, while silicon die sizes of less than 1.4 x 1.5 mm^2 have been reported [1] for complete monolithic receivers. However, considering the possibility of including additional circuit blocks such as baseband processing and transmitter functionality, die sizes up to 10 mm^2 can be expected while the use of significantly larger chips for the sole reason of monolithic antenna integration cannot be justified due to cost.

As a consequence of the limited practical die size, high directivity antennas cannot be implemented on silicon chips together with the active electronics. The critical parameters for the antennas thus become efficiency and, if required by the application, bandwidth. The radiation efficiency is defined as

$$\eta = \frac{P_{rad}}{P_{accepted}} \tag{2.1}$$

where P_{rad} is the radiated power and $P_{accepted}$ is the power accepted by the antenna. Return loss caused by impedance mismatch should thus not be included in the radiation efficiency figure of merit.

For small antennas, defined by Wheeler [2] as antennas which fit within a radiansphere with radius $a = 1/k$ where k is the wave number of the radiated field, a relation between the size of the antenna and the minimum radiation quality factor can be calculated. Original results by Chu [3] were re-examined by McLean [4] to improve the accuracy for larger antennas, arriving at the

expression

$$Q = \frac{1}{k^3 a^3} + \frac{1}{ka} \qquad (2.2)$$

for the lowest achievable radiation quality factor Q of linearly polarized antennas which fit in a sphere with radius a. The quality factor sets a limitation on the maximum achievable bandwidth assuming 100% efficiency of the radiator. Small antennas, having high radiation quality factors, often suffer from low efficiency which can lead to apparently larger bandwidths than the maximum suggested by equation 2.2.

It should be noted that the analysis in [4] is based on the assumption of a single TM_{01} spherical mode, equivalent to the fields of a linear current element. For circular polarization a modified equation is available. It is also important that the surrounding sphere encompass the entire antenna, including the commonly encountered finite groundplanes, as current on other structures than the intended radiator can contribute to the radiation and thus lower the radiation quality factor.

Antennas on thin square substrates of 10 mm^2 size, suggested above as the maximum practical size of K-band on-chip antennas, would fit in a sphere with radius 2.3 mm, which at 24 GHz is slightly larger than the 1.9 mm radius of the radiansphere. By efficient use of the available area on the semiconductor die, it should thus be possible to integrate antennas which are not "small" according to the classical definition. Hence, the severe efficiency and bandwidth limitations typically encountered with small antennas can be avoided.

In the case of antennas manufactured on silicon substrates, dielectric losses are a major contribution to low antenna efficiency. As silicon is a nonmagnetic (permeability $\mu = \mu_0$) material the relevant parameter for the characterization of the microwave properties of the material is the complex permittivity, which can be written as

$$\varepsilon = \varepsilon' - j\varepsilon'' = \varepsilon_0 \varepsilon_r (1 - j\tan\delta) \qquad (2.3)$$

where the relative permittivity ε_r ranges between 11.7-11.9 at microwave frequencies, and the permittivity of vacuum is $\varepsilon_0 = 8.85 \cdot 10^{-12}$. The high relative permittivity ε_r of silicon might be considered an advantage for on-chip antennas as it allows size reduction of resonant radiators. The factor $\tan\delta$ denotes the ratio of the conduction to displacement currents in the dielectric. High values of $\tan\delta$ causes losses due to heating in the presence of an electric field in the material. In the general case, an effective loss tangent can be defined [5] as

$$\tan\delta_e = \frac{\sigma_e}{\varepsilon'\omega} = \frac{\sigma_s + \sigma_a}{\varepsilon'\omega} = \frac{\sigma_s}{\varepsilon'\omega} + \frac{\sigma_a}{\varepsilon'\omega} \qquad (2.4)$$

where σ_s is the static conductivity of the material and σ_a the alternating current conductivity due to losses in the presence of a time-varying electric field. The time variation of the the electric field is assumed to be harmonic and represented by the angular frequency ω.

For semiconductors with low bulk resistivity, the substrate losses represented by $\tan \delta_e$ are normally dominated by the static conductivity losses and can thus be approximated by

$$\tan \delta \approx \frac{1}{\varepsilon' \omega \rho} \qquad (2.5)$$

where ρ is the resistivity of the material. Commercial silicon integrated circuit processes typically use silicon with bulk resistivity of 1-50 Ωcm, thus leading to excessive losses for antennas implemented using the conductor layers available in the process.

2.2 Micromachining of silicon for antenna applications

To mitigate the effects of substrate losses the geometry of the normally planar silicon wafer can be modified, either by addition of layers and structures to the front side of the wafer or removal of substrate material. By surface micromachining, materials such as polymers, metals and oxides are added to the top of the wafer, allowing bridges and beams to be formed. Bulk micromachining is performed by selectively removing part of the substrate, usually by backside etching. A combination of surface processing with bulk micromachining is commonly used to form membranes of dielectric materials. Such membranes have found uses for transmission lines, inductors and antennas where the substrate losses are minimized by suspending the printed metallic conductors in air.

2.2.1 Thick polymer dielectric

Adding a layer of low loss polymer dielectric between the silicon substrate and the conductor metallization, as illustrated in Fig. 2.1, is a simple way of reducing the losses of passive and distributed microwave components manufactured on low resistivity silicon wafers. Benzocyclobutane (BCB) is a polymer with a dielectric constant $\varepsilon_r = 2.65$ and low losses ($\tan \delta = 0.002$) which has been specifically developed for electronic manufacturing. With multiple applications of the polymer, thicknesses of up to 20-30 μm are readily obtained. Photosensitive allows BCB vias to be implemented, thus enabling vertical interconnects between conductor layers on top of the BCB and components residing on the substrate. Coplanar transmission lines with reduced loss have been demonstrated on top of 10-20 μm thick BCB layers [6]. The low losses of the BCB dielectric in combination with an increased distance to the silicon substrate have also been used to improve the quality factor of spiral inductors [7].
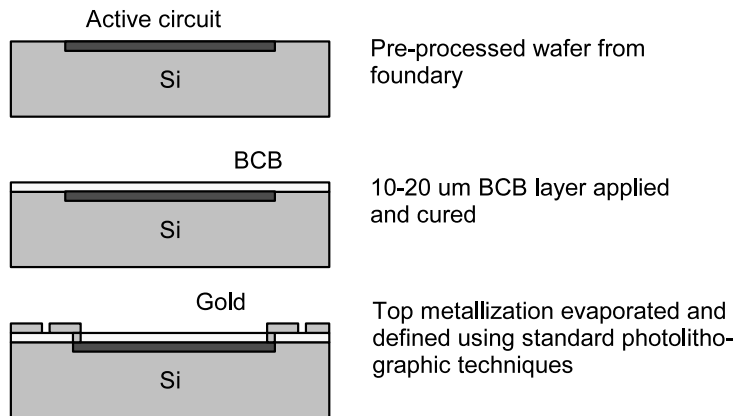
Figure 2.1: Post-processing of thick organic dielectric on pre-manufactured integrated circuit.

2.2.2   Bulk micromachining

Selective removal of the bulk semiconductor substrate is performed by dry or wet etching methods. In the wet etching process, the silicon wafers are typically submerged in a Potassium Hydroxide (*KOH*) [8] or Tetramethylammonium Hydroxide (*TMAH*) solution. The anisotropic etching of the substrate using these liquids yields slanted walls, restricted by the (111) crystal planes of the substrate, as shown in Fig. 2.2.   The slanted walls and the restriction
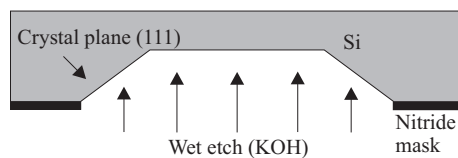

Figure 2.2: Anisotropic etching of (100) silicon, yielding slanted walls.

of having to align micromachined features with the crystal planes makes the method suitable for creating rectangular cavities and membranes, while it is difficult to implement narrow trenches, complex membrane shapes, and high aspect ratio holes. An advantage of wet etching is the batch type nature of the process, thus allowing low cost production. This advantage is however partially negated by the need for a durable mask, such as nitride, to define the areas to be etched.

Dry etching of the substrate is performed by a plasma in an evacuated chamber. For micromachining purposes the Deep Reactive Ion Etching (DRIE) based on the advanced BOSCH process [9], is commonly used, as it is capable of yielding holes and cavities with vertical walls, as shown in Fig. 2.3. High aspect ratios can be obtained, thus allowing substrate material to be selectively

removed with good precision. The method also allows complex patterns to be etched as it is not sensitive to the orientation of the crystal planes. The DRIE
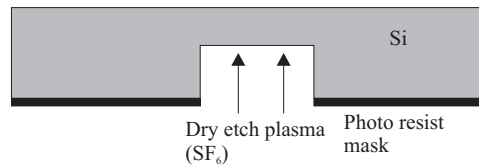

Figure 2.3: Dry etching (DRIE) of silicon.

process is generally more costly than wet etching as the equipment is expensive and usually limited to single wafer processing. Typical etch rates are in the order of 2 - 3 μm per minute [10], thus requiring lengthy processing if holes are to be etched through wafers of standard 300-500 μm thickness.

A low temperature membrane process, compatible with preprocessed semiconductor wafers, is obtained by combining the BCB dielectric process described in section 2.2.1 with bulk micromachining [11]. The BCB membrane are released by back-side etching of the wafer using DRIE or wet etching methods such as KOH.

2.2.3   A review of micromachined antennas

The vast majority of the micromachined antennas available in literature are membrane suspended patch antennas. Such antennas were originally developed at the University of Michigan, and demonstrated at 94 GHz [12] and 13 GHz [13]. Patch antennas based on similar concepts have been designed, such as a 16 GHz patch suspended on a 254 μm thick high resistivity silicon substrate backed by a micromachined low resistivity wafer [14]. As high resistivity silicon with low conductivity losses has been used as membrane material in these cases, micromachining has primarily been introduced to suppress substrate modes and to improve the bandwidth of the antennas. The advantage of the micromachined patch is mainly the high directivity, and the absence of a back lobe, which significantly facilitates packaging of the implemented device. However, a patch antenna is a space consuming radiator, particulary if implemented on a micromachined membrane with the resulting low effective permittivity of the substrate.

Large micromachined membranes have been used to implement slot radiators and arrays [15] [16]. End-fire, Yagi-Uda antennas have also been built on similar membranes [17]. Low losses were obtained, but large on-chip micromachined membranes would be costly to implement in a semiconductor process due to excessive area requirements. In addition, large membranes are prone to mechanical damage.

For on-chip antenna integration the possible use of selective micromachining of silicon in areas of high field strength is of interest, as it can minimize the required membrane areas. Selective etching has been proposed for patch and slot loop antennas [18] as a method of reducing the effective dielectric constant and preventing substrate modes, but no investigation of the reduction of substrate losses was performed as the antennas were implemented on high resistivity silicon.

It can be concluded that most of the results for micromachined antennas reported in literature rely on the use of large membranes or high resistivity silicon and are thus not directly applicable to the problem of designing compact on-chip antennas compatible with commercial IC processes. To address this problem, compact on-chip radiator designs using selective micromachining of the substrate for loss reduction are presented in the following sections. In particular, an effort is made to reduce the necessary size of the micromachined membranes in order to maximize the available space for the integrated circuit.

2.3 Full wavelength square loop antenna

As a quarter wavelength in free space at 24 GHz corresponds to 3 mm, the full wavelength square loop, having a circumference of approximately $\lambda_0 = 12$ mm in free space becomes a candidate on chip antenna for chips of 10 mm^2 size. Efficient use of the semiconductor area requires that the area inside the loop can be used for circuits, as illustrated in Fig. 2.4. Integration of active
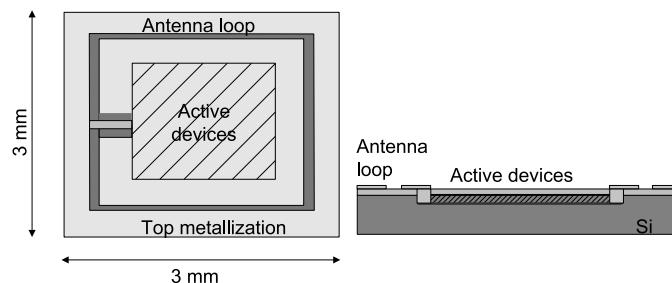

Figure 2.4: Suggested integration of a K-band square slot loop antenna at the perimeter of a 10 mm^2 large chip.

electronics within the aperture of a slot loop antenna has been demonstrated [19], utilizing the fact that the current flow on the ground-plane in the center of the slot loop is low. However, the risks of cross-talk and reduced radiation resistance due to induced currents in the circuit metallization have to be taken into account in the antenna and integrated circuit design.

The full wavelength loop antenna should not be confused with the classical loop antenna which is small compared to the wavelength and usually assumed to have a constant current in the loop. Instead, the electrical characteristics

resembles the folded dipole antenna with current maximums at the feed point and at the opposite end of the loop. If necessary, it is possible to realize a compact T-match [20] in close vicinity to the loop to adjust the impedance to a value suitable for the integrated electronics.

2.3.1 Surface micromachined slot loop

The easiest post-processing method from a manufacturing point of view for enhancement of the radiation efficiency is the addition of a thick polymer layer such as BCB or polyimide to the front-side of the semiconductor substrate, as used for the low loss CPW transmission lines reported in [21]. The use of thick dielectric to improve the efficiency of slot antennas manufactured on low resistivity silicon has been proposed [22], however no data on the measured antenna gain or efficiency were given in the reference.

In *Paper I* the design and evaluation of 24 GHz full wavelength slot loop antennas using a 10 to 20 μm thick BCB interface layer between the silicon substrate and the top metallization is presented. The implemented test structure is shown in Fig. 2.5. The slot loop was designed with a 2x2 mm loop
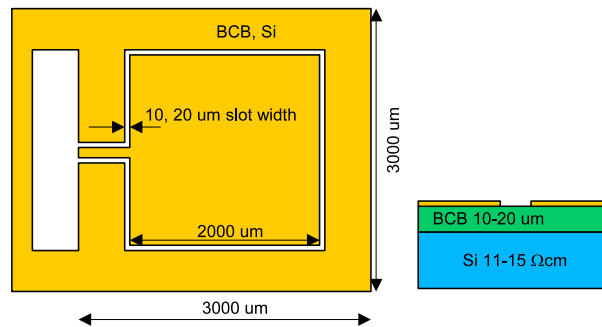

Figure 2.5: Surface micromachined slot loop antenna evaluated in *Paper I*. CPW probe pad for characterization purposes to the left.

size and slot widths of 10 μm and 20 μm. The resonance frequency of the antenna is 24 GHz and a -10 dB impedance bandwidth of 7 GHz is obtained in a 50 Ω system. The measured gain of the implemented loop is -3.6 dBi, which compared to the standard square loop directivity of 3.3 dBi indicates less than 20% efficiency.

With the proposed loop antenna integration scheme, where circuits are to be placed within the aperture of the antenna, there is a risk of cross-talk between the antenna and the integrated circuit. When adding the slot antenna metallization to the top of the substrate, care has to be taken as the integrated circuit might employ groundplanes or ground shields in the design which together with the antenna metallization could create parallel plate modes as illustrated in Fig. 2.6. As discussed in *Paper I*, such modes can be short-circuited by
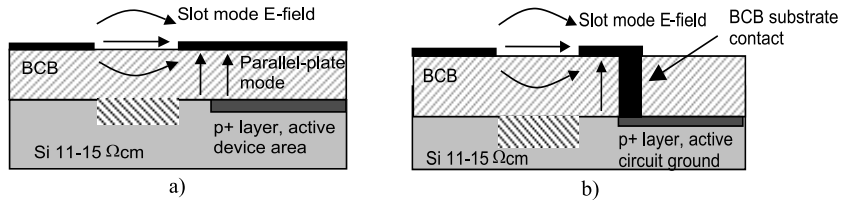
Figure 2.6: Implementation of a) solid ground-plane over the chip and b) antenna ground-plane opened up over the circuit parts of the chip.

introducing via connections between the circuit ground-planes or substrates dopings and the antenna ground-planes.

2.3.2 Bulk micromachined loop antennas

In many cases, the 20% antenna efficiency obtained for the slot loop presented in *Paper I* is insufficient. Loss reduction by bulk micromachining, where part of the substrate is etched away, could thus be considered. However, as the main point of the proposed on-chip loop antenna is to preserve the silicon area within the aperture for the integrated circuit, the classical approach of suspending the entire radiator on a large membrane is of limited interest.

Few results for micromachined loop antennas are available in literature. An annular loop antenna suspended on a BCB membrane manufactured on a silicon substrate has been demonstrated at 24 GHz [23], however the size of the 5.4x4.5 mm^2 elliptical membrane is prohibitively large for on-chip antenna applications. A more suitable technique is the use of micromachined trenches in regions of high electrical field strength as demonstrated for slot loop antennas [24], although the loss reduction aspects were not investigated in that work.

In *Paper V* practical designs for on-chip micromachined slot and wire loop on-chip antennas are proposed and evaluated. The antennas have been implemented on substrates with 10-50 Ωcm bulk resistivity to be representative of the wafers used in commercial silicon integrated circuit processes.

The micromachined slot loop antennas, shown in Fig. 2.7, are equipped with membrane covered trenches in the area of high electrical field strength present at the radiator conductor or slot transmission line. Bridges, required for mechanical support of the center section of the die, are placed at the E-field minimums in the loop. The designed slot loop radiator has been evaluated with respect to choice of membrane material, bridge width W_{br} and trench width W_{tr}. It is found that a trench width of 200 μm is sufficient to increase the gain to better than 1 dBi, compared to a simulated value of -6 dBi without trenches. A further increase of membrane size yields small improvements. The design is not sensitive to the width of the bridges. For an increase of bridge
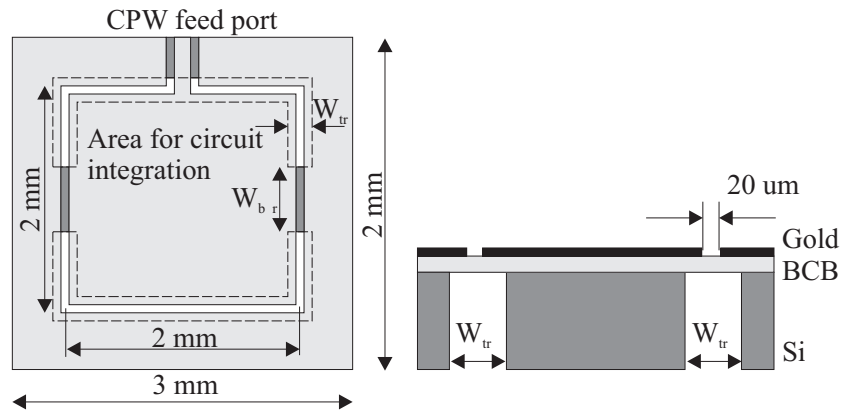
Figure 2.7: Bulk micromachined slot loop antenna with W_{tr} = 100-400 μm wide trenches investigated in *Paper V*. Two silicon bridges with W_{br} = 200 to 1100 μm cross the membrane at the two field minimums in the loop.

width from 200 to 1100 μm no noticeable gain reduction at resonance is seen in measurements.

Due to the common use of differential circuit topology in silicon RFIC designs, the balanced feed obtained by a wire loop antenna might be preferred to the unbalanced feed offered by the slot loop. A wire loop antenna design similar to the presented slot loop is obtained by replacing the slot with a wire radiator as shown in Fig. 2.8. Most of the properties of the wire loop, such
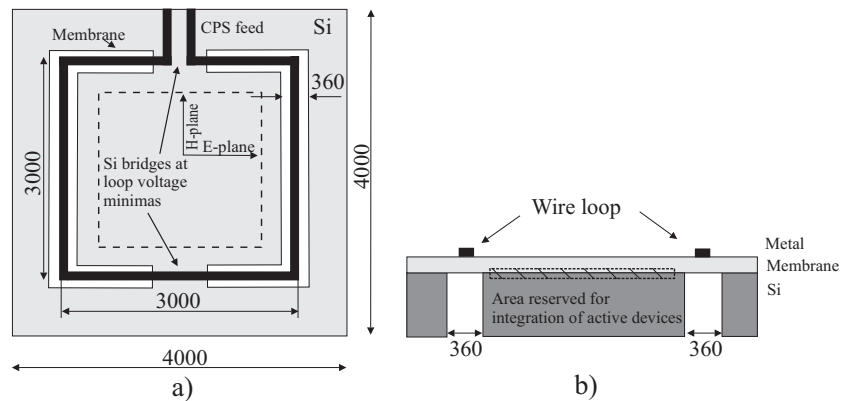
Figure 2.8: Layout a) top view b) cross section of the micromachined wire loop antenna.

as radiation pattern, are similar to the properties of the slot loop, however the position of the supporting bridges which cross the trench have been moved as the voltage minimums in the wire loop appear at the feed point and the virtual ground point at the opposite end of the loop. A 24 GHz loop of 3x3 mm size was designed with a trench width of 360 μm. The measured input impedance for a wire loop suspended with BCB membranes was 85 Ω which

is close to the 100 Ω input impedance normally obtained for a square loop in free space. The measured gain in the broadside direction is 1 dBi, which compared to the theoretical directivity of 3.3 dBi for the loop indicates relatively good efficiency.

In contrast to the slot loop, there is no ground-plane normally present in the center of the wire loop, thus raising the question of whether circuits can be placed within the aperture of the loop without disturbing the antenna. For the loop antennas reported in *Paper V*, ground-planes deliberately introduced within the center of the wire loop yielded gain reductions less than 0.5 dB. Hence, the presence of an integrated circuit within the loop is not expected to cause any significant performance reduction.

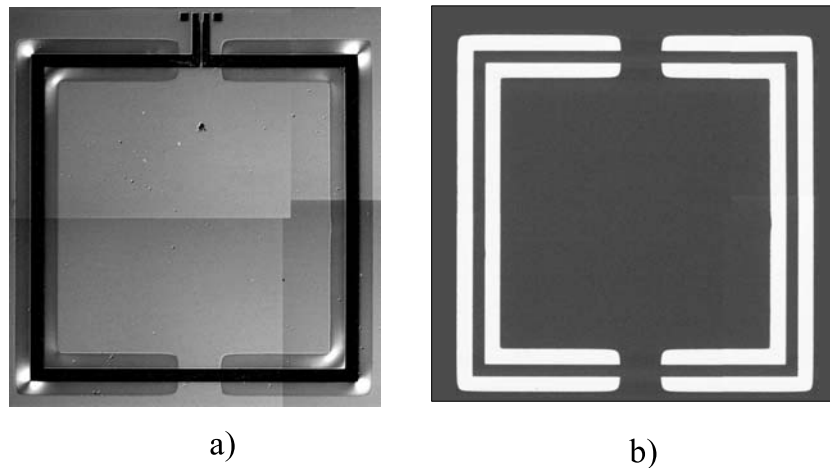The realized wire loop antenna is depicted in Fig. 2.9.

a)   b)

Figure 2.9: Optical microscope chip photo of the manufactured wire loop antenna a) front side with membrane supported loop metallization, and b) substrate side with back light, showing the dry etched trenches.

2.4   Meander dipole antenna

The half-wave dipole antenna is one of the basic antenna types and its balanced feed makes it a suitable choice for integration with active front-ends using differential circuit topology. However the length will in many cases be prohibitive when realized on a micromachined membrane as the effective dielectric constant ε_{eff} is close to one.

A common technique for reducing the length of a dipole antenna is meandering of the linear radiator. The meander dipole can be considered as a short dipole, which is periodically loaded with inductors created by short circuited coplanar strip line (CPS) stubs to obtain resonance. Since the radiation from the lengthening inductive sections cancel in the far field of the antenna, low

radiation resistance R_{rad} is obtained compared to a full length dipole. As the total wire length and conductor resistance remain approximately the same as for a half wave linear dipole, the efficiency is reduced by the meandering of the radiator. Shortening ratios and the effect on radiation resistance are available in literature [25], where $R_{rad} = 43\Omega$ is reported for a dipole with 30% length reduction. Optimum meandering techniques have been suggested such as a meander bow tie dipole[26], however the improvements compared to a radiator with equal size loading sections are relatively small.

In *Paper II* the membrane suspended, 24 GHz meander dipole antenna, shown in Fig. 2.10, is evaluated. The compact radiator has been manufac-
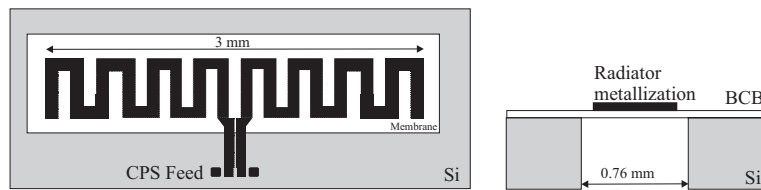

Figure 2.10: Layout of the 24 GHz meander dipole antenna described in *Paper II*.

tured on a 3.3x0.76 mm^2 large membrane. Due to the length reduction, the input impedance for the dipole is only to 20 Ω. However, the low resistance is not necessarily a problem from a matching point of view since the integrated circuit can often be tailored to directly work with lower impedance levels than the standard 50Ω. The manufactured meander antenna is depicted in Fig. 2.11.

The measured return loss for a meander dipole implemented on a BCB membrane, measured with 50 Ω system impedance, is shown in Fig 2.12. Low sensitivity of the antenna return loss with regard to the micromachined membrane size is obtained, which indicates small influence of the remaining substrate on the antenna performance. By increasing the clearance between the radiator metallization and the edge of the membrane from 125 μm to 425 μm only a minor increase in resonance frequency from 24 to 25 GHz is obtained. Compared to the simulated 26 GHz resonance frequency with the silicon substrate entirely removed, it is seen that the membrane size is not a critical parameter in the design. The measured gain, compensated for the return loss in a 50Ω system is 0.7 dBi, which compared to the maximum directivity of 2.1 dBi for a half-wave dipole indicates good efficiency.

2.5 Inverted F antenna

The inverted F antenna is a compact radiator which is commonly used in wireless communication [27]. The antenna was invented for use as a low profile antenna on missile bodies [28]. In the original analysis a transmission line
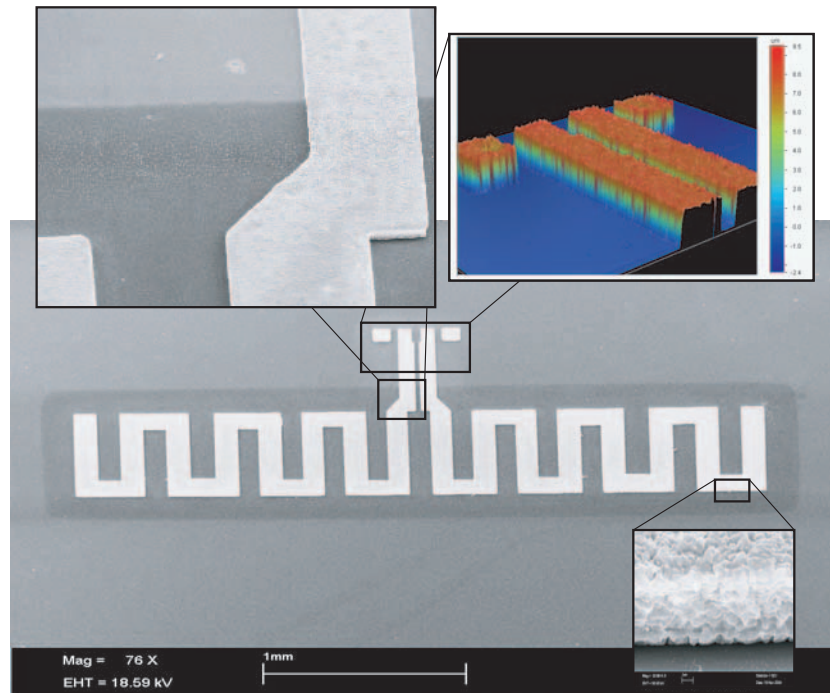
Figure 2.11: The meander dipole antenna manufactured on a 2.5 mm^2 large silicon oxide/nitride membrane.

approach was used to calculate the input impedance and radiation pattern. However, in many practical applications the inverted F can be considered as a short monopole antenna, top loaded with a transmission line and thus analysed as an inverted L antenna [29]. As illustrated in Fig. 2.13, the important design parameters of the inverted-F are the distance from ground H_F, the length of the top load L_F and the position D of the feed point relative to the ground connection of the radiator. Generally, a large distance H_F from ground is desirable to maximize the the radiation resistance and bandwidth of the radiator, while the additional length L_F is selected to obtain resonance at the operating frequency. In an on-chip antenna application, where the circuit metallization serves as antenna ground, H_F is restricted by the area the antenna is allowed to occupy. An advantage of the inverted F is the ease of which the antenna can be matched to a wide range of impedances by selection of the feed-point distance D from the short-circuit.

Inverted F antennas manufactured in silicon integrated circuit process have been reported [30]. Proton implantation was used to increase the substrate resistivity and reduce losses in the vicinity of the radiator. As an alternative to the use proton implantation, the IC compatible BCB-membrane post-processing method described in this chapter could be considered. In *Paper IV* the design and evaluation of a 24 GHz micromachined on-chip inverted F antenna, shown in Fig. 2.14, is presented. The antenna has been manufactured
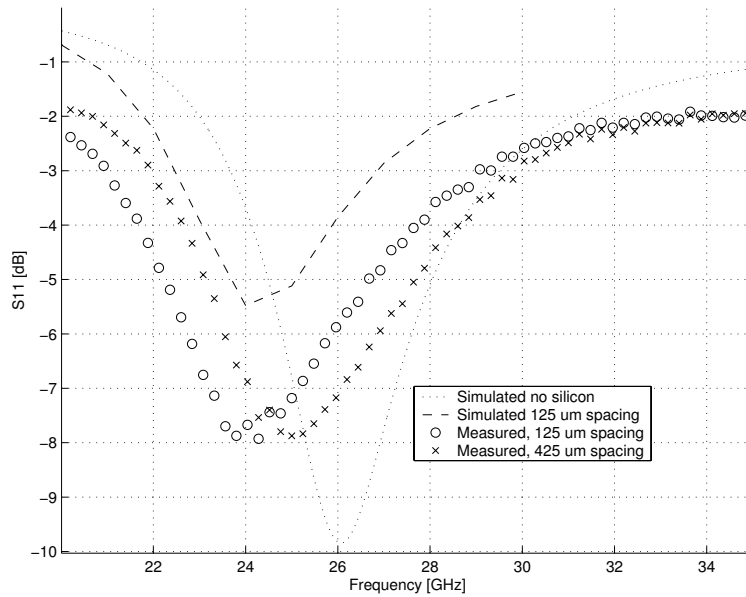
Figure 2.12: Measured and simulated return loss for meander dipole antenna with different membrane sizes.
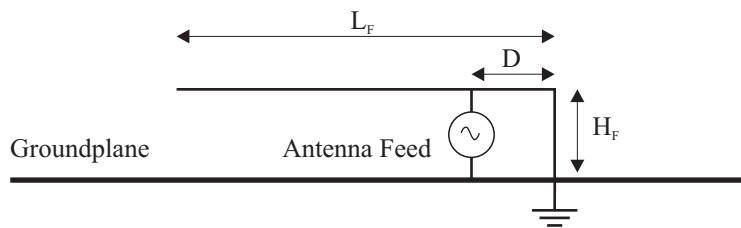
Figure 2.13: Principle of the inverted F antenna.

on a 3.8x3.8 mm^2 large, 11-15 Ωcm silicon substrate where the chip size was chosen to simulate the size of a real integrated circuit. The inverted-F radiator is suspended on a 2.4 mm^2 large BCB membrane to reduce the losses. A return loss of -16 dB is obtained at 24 GHz and the -10 dB bandwidth is 2 GHz. The measured gain is -0.7 dBi, which compared to a simulated directivity of 2.1 dBi indicates better than 50% efficiency.

The relatively low gain of the implemented inverted-F antenna can be partly explained by the low directivity, however another source of gain degradation is substrate losses in the vicinity of the ground-plane. As a small ground-plane representative of typical circuit sizes is used as a counter-poise for the radiator, significant currents will flow outside the membrane area.

29
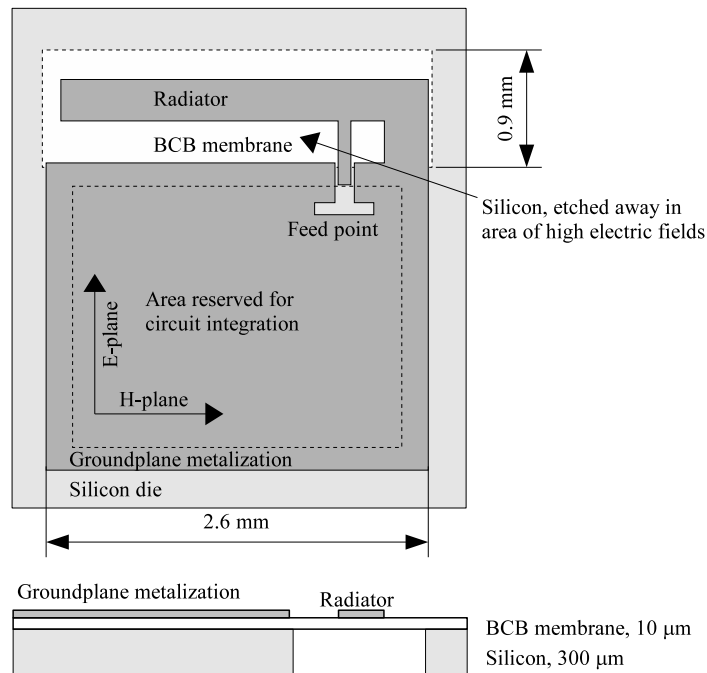
Figure 2.14: Inverted F antenna with membrane suspended radiator, presented in *Paper IV*.

2.6 Packaging of the micromachined antennas

In many applications conductor backing of the on-chip antennas is desirable to eliminate the back lobe, increase gain, or use metal heatsinks in the packaging. Conductor backing of the bulk micromachined slot loop antenna presented in Sec. 2.3.2 has been demonstrated [31]. A ground plane was introduced at a distance of $\lambda_0/4 = 2$ mm, as shown in Fig. 2.15. In the forward lobe, see Fig.
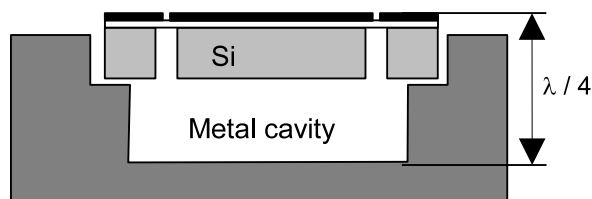
Figure 2.15: Conductor backing of a micromachined slot loop antenna.

2.16, 4 dBi was measured in the setup, thus indicating that close to 3 dB gain improvement could be obtained compared to a similar radiator in free space environment.

However, the demonstrated setup represents a simplification of the requirements in a real package. In many cases, the reflector needs to be mounted closer than the ideal $\lambda_0/4$ distance from the radiator to obtain a low profile
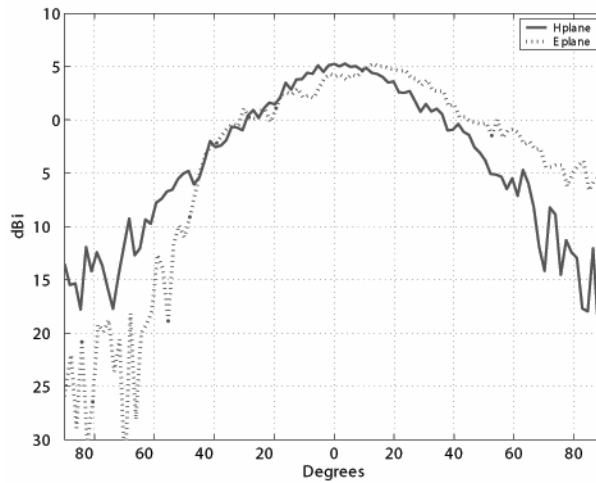
Figure 2.16: Radiation pattern of the conductor backed slot loop antenna.

package. Use of dielectric materials in the package could reduce this distance if the substrate modes in the package can be controlled.

Mechanical and environmental protection of the integrated circuit is often needed, particulary for silicon dies with micromachined membranes or circuits using bond wires for interconnections with the carrier in the package. The packaging needs to be transparent to the radiation from the on-chip antenna and free from cavity resonances. Predictable dielectric properties of the packaging materials are also needed in order to compensate the antenna for loading effects.

A simple, low cost packaging method is the use of a organic glob-top material to encapsulate the device, as proposed in Fig. 2.17. The use of glob-top
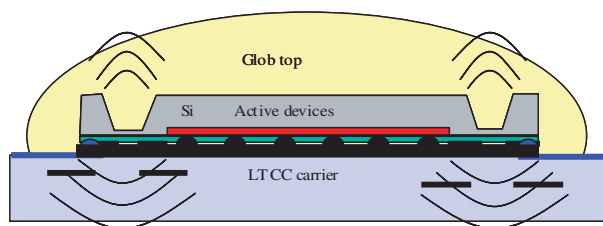
Figure 2.17: Suggested glob-top packaging of membrane antennas.

encapsulation for flip-chip mounting of microwave devices has been investigated [32] [33]. Several silicone and epoxy glob-top materials have been evaluated for 24 GHz applications [34], showing adequate performance for high frequency applications with only minor degradation of the quality factor for the implemented microstrip transmission line components. Recently, the

31

use of organic materials have been investigated for 60 GHz systems with integrated antennas [35]. The radiating element was however not covered by the encapsulant.

2.7   Summary and comparison of the micromachined radiators

The micromachined on-chip antennas investigated within the scope of this chapter have common design goals, such as high efficiency in the presence of the low resistivity silicon substrate and efficient utilization of the available on chip area. Characteristics of the individual antenna types, as summarized in Table 2.1, might make a certain radiator preferable for a specific application. If a loop antenna around the perimeter of the chip fits the circuit size it

	Slot loop	Wire loop	Meander dipole	Inverted F
Area [mm^2]	10	16	2.5	2.4
Etch type	DRIE	DRIE	DRIE / Wet	DRIE / Wet
Feed type	Unbalanced	Balanced	Balanced	Unbalanced
Gain [dBi]	1.5	1	0.7	-0.7
Impedance [Ω]	100-120	80-120	20	50

Table 2.1: *Comparison of the micromachined 24 GHz radiators for implementation on a 10 mm^2 large low resistivity silicon chip.*

yields a compact solution which utilizes the available die size to enable a full size antenna to be integrated. The selection of a wire or slot loop is primarily determined by the required feed type, balanced or unbalanced.

The meander dipole or inverted-F might be considered if a more localized antenna implementation is needed, for instance due to mounting or bond wire routing requirements. Another advantage of these antenna types is the use of simple rectangular membranes, thus allowing anisotropic wet etching to be used for the manufacturing instead of the more expensive DRIE process needed for the loop antenna trenches. Again, the use of single ended or differential circuit topology would determine whether the balanced dipole or unbalanced inverted-F antenna is the most appropriate choice.

3. Monolithically Integrated Antennas

Monolithic integration of on-chip antennas with complete self-contained receivers manufactured in a commercial IC process is treated in this chapter. In contrast to Chapter 2, where the substrate losses were reduced by micromachining, high resistivity silicon wafers are used to improve the efficiency of the on-chip antennas presented in this chapter. The implemented receivers are based on circuit designs developed by the University of Ulm, Germany.

3.1 Millimeter wave antennas in silicon active device processes

Monolithically integrated antennas have traditionally been considered in classical III-V MMIC processes. These processes use a semi-insulating gallium arsenide (GaAs) or indium phosphide (InP) substrate. Typically, a back-side ground-plane is provided to allow distributed passive elements such as transmission lines, stubs, and couplers to be implemented in microstrip technology. Due to the presence of the ground plane, patch radiators have been used for the integrated antennas implemented in these processes.

In silicon technology the SIMMWIC concept [36] was introduced more than a decade ago as it became evident that SiGe HBT technology would extend the usable frequency range of silicon transistors into the microwave and millimeter wave frequencies. The SIMMWIC:s proposed are similar to III-IV MMIC in that transmission line components and a high restivity substrate are used with relatively few active components. However, coplanar waveguides (CPW) have typically been used instead of microstrip transmission lines which removed the need for the substrates vias and backside groundplane typically used for most circuits implemented in III-IV technology. Consequently, the implemented integrated antennas have mainly been of slot type in SIMMWIC processes due to compatibility requirements with the front-side groundplane and transmission line type.

In most commercial CMOS, BiCMOS and SiGe HBT processes the only substrate available is low resistivity silicon. High frequency integrated circuits are predominantly designed using lumped passive components, such as spiral inductors, as losses and space restrictions preclude the use of distributed transmission line components. Unless backside micromachining can be used, as proposed in Chapter 2, extremely low antenna efficiency is obtained due

to excessive substrate losses. However, in certain commercial silicon bipolar processes, such as the Atmel SiGe2RF process, high resistivity silicon is available as a process option. An increased use of silicon-on-isolator (SOI) and silicon-on-sapphire (SOS) substrate in future CMOS process can also be expected which merits an investigation of the possibility of monolithic integration of antennas with circuits manufactured on high resistivity wafers.

In the work presented in this chapter the Atmel SiGe2 RF process [37] has been used. A cross section of the different layers in the process is shown in Fig. 3.1
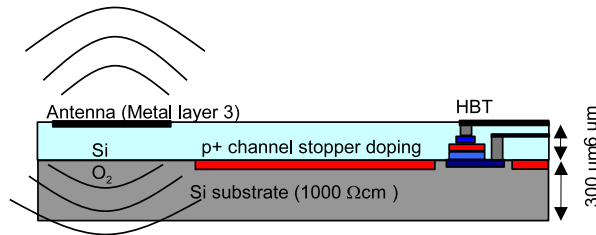

Figure 3.1: Cross-section of the semiconductor substrate in the Atmel SiGe2 RF process.

The semiconductor substrate is p-doped and has a nominal resistivity of 20 Ωcm, however high resistivity silicon substrates ($> 1500\Omega$cm) can be selected as a process option. The availability of high resistivity substrates can partly obviate the need for micromachining for implementation of high efficiency on-chip antennas.

In areas close to the transistors a highly conductive p+ doping, with a resistivity of 150 Ω/sq, is introduced at the surface of the substrate in order to suppress parasitic channels from forming between the active devices. This layer can be removed in areas of spiral inductors or on-chip antennas to minimize substrate losses.

3.2 Design of the monolithically integrated antenna

No large groundplanes are normally available in a standard silicon RFIC design as lumped passives are commonly used instead of distributed transmission line components. The implementation of a on-chip slot or patch antenna is thus difficult. As a consequence of the lack of a stable RF-ground, a differential circuit topology is preferred. Hence, the use of an antenna with a balanced feed, such as a dipole or full wave loop, is advantageous as the need for a balun is avoided. Due to the fact that the dipole does not encompass the entire circuit, off-chip connections for testing purposes are more easily arranged than in the case a loop antenna. Compact dipoles have for this reason been used for the implemented integrated antenna receivers presented in this chapter.

Monolithically integrated dipole antennas in silicon IC processes have been previously reported, however low gain has typically been obtained due to the use of low resitivity substrates. A 10 GHz dipole manufactured in a silicon process and monolihically integrated with a oscillator yielded a reported efficiency of 24% [38]. On-chip meander dipoles have also been suggested for clock distribution [39] [40] in digital circuits, but in these cases the requirements on gain are low due to the short distances between the antennas in the application.

The analysis of a printed dipole on a finite dielectric substrate usually requires 3D finite element numerical simulation as the Greens functions required for a Method of Moments (MoM) analysis cannot be easily derived for non-infinite substrates. However, a qualitative description of the resonance frequency and input impedance of the dipole in presence of the silicon substrate can be obtained by replacing the dielectric and the surrounding free space with a homogenous dielectric with an effective permittivity ε_{eff}, where $1 < \varepsilon_{eff} < \varepsilon_r$, as illustrated in Fig. 3.2. As the resonant length of the dipole
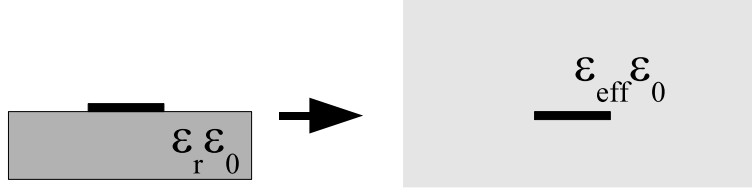

Figure 3.2: Cross section of printed dipole on substrate replaced with effective dielectric environment.

is proportional to the wavelength in the medium a length reduction

$$l_{diel} = \frac{l_{freespace}}{\sqrt{\varepsilon_{eff}}} \qquad (3.1)$$

from the free space length $l_{freespace}$ to l_{diel} is obtained.

The radiation resistance of a half wavelength dipole with negligible conductor width and a sinusoidal current distribution can be calculated from the radiated power, found by integrating the Poynting vector over the entire sphere, for a given current amplitude I_0. The result, derived in [41], yields

$$R_r = \frac{2}{|I_0|^2} P_{rad} = \frac{2}{|I_0|^2} \eta \frac{|I_0|^2}{4\pi} \int_0^\pi \frac{\cos^2(\frac{\pi}{2}\cos\theta)}{\sin\theta} d\theta \qquad (3.2)$$

where η is the intrinsic impedance of the surrounding medium, which in a dielectric can be calculated from the relative permittivity

$$\eta = \sqrt{\frac{\mu_0}{\varepsilon_0 \varepsilon_r}} \qquad (3.3)$$
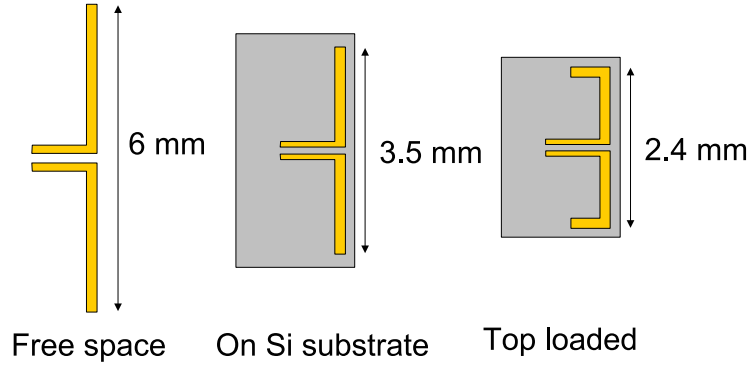
35

Figure 3.3: Size reduction of the on-chip dipole by substrate effects and top loading.

Hence, for a resonant half wavelength dipole the relation

$$R_r = \propto \frac{1}{\sqrt{\varepsilon_{eff}}} \tag{3.4}$$

is obtained, thus indicating that the reduction in radiation resistance is proportional to the length reduction of a resonant dipole caused by introduction of the dielectric. The effective dielectric constant approximation for determining the radiation resistance reduction has been validated by electromagnetical simulations for antennas on silicon substrates [38].

The size of a 24 GHz half wave dipole positioned at the edge of the chip is reduced to 3.5 mm, as shown in Fig. 3.3, by the presence of the silicon dielectric. To obtain an acceptable chip size, the radiator can be further shortened by folding back the ends along the perimeter of the die, thus effectively top loading the straight section of the dipole. The disadvantage of the length reduction is increased cross polarization and decreased radiation resistance, which in turn leads to lowered efficiency.

The reduction of radiation resistance caused by the dielectric substrate and the top loading does not only lower the efficiency of the antenna, but also complicates the matching of the antenna to the front-end circuits. The low input impedance of the dipole can however be raised by the use of a folded radiator. Printed folded dipoles were analyzed by Lampe [42] and an expression for the input impedance is given by Eq. 3.5

$$Z_{in} = \frac{2(1+a)^2 Z_d Z_x}{(1+a)^2 Z_d + 2Z_x} \tag{3.5}$$

where Z_d is the impedance of a single dipole, Z_x the impedance of the transmission line mode formed by the to parallel conductors and a the ratio of the currents on the driven and parasitic branch of the radiator. As the dipole is normally used at the half wavelength resonance, the impedance Z_x of the quarter wave long shorted stub formed by the transmission mode goes to infinity. For

equal line widths same current flows on both branches of the radiator, corresponding to $a = 1$ and an impedance step-up ratio of $(1 + a)^2 = 4$.

3.2.1 Substrate wave excitation

Printed antennas on dielectric substrates often suffer from the excitation of surface waves, as illustrated in Fig. 3.4. In the case of a non-grounded di-
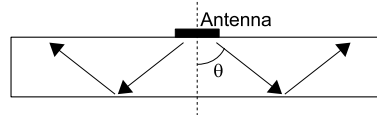

Figure 3.4: Substrate wave excitation in dielectric.

electric substrate in free space, waves launched at a critical angle larger than θ from a dipole antenna mounted at the air/dielectric interface get trapped in the substrate [43].

The excitation of substrate waves is especially a problem with grounded dielectric substrates, such as in the case of a reflector backed printed dipole antenna. For the grounded substrate case, a number of propagating substrate modes can be present. The cutoff frequencies f_c for the modes are given by

$$f_c = \frac{nc}{4d\sqrt{\varepsilon_r - 1}} \tag{3.6}$$

where d is the thickness of the substrate, ε_r the relative dielectric constant, c the speed of light, and $n = 1, 2, 3, ...$ the mode number of the propagating surface TM_0, TE_1, TM_2, ... modes. As the TM_0 has zero cutoff frequency, substrate wave losses are always present in the case of a grounded substrate, even if the amount of lost power can be considered negligible [44] for thickness $d < 0.01\lambda_0$ of the dielectric. Generally, the power lost in substrate modes increases significantly as higher order modes appear.

Silicon wafers used for the manufacturing of integrated circuits are normally thinner than 500 μm. Hence, a minimum cutoff frequency f_c of 45 GHz for the higher order modes of a grounded silicon ($\varepsilon_r = 11.9$) substrate can be calculated using Eq. 3.6. As the work presented in this chapter primarily deals with 24 GHz circuits, only the losses of the TM_0 mode have to be considered. For applications at higher frequencies, such as short range communication in the 59-64 GHz band or car radar at 77-88 GHz, the higher order modes could be suppressed by the use of a thinner substrate or micromachining as proposed in Chapter 2.

The substrate wave losses in silicon due to the TM_0 mode can be estimated using the available data [44] for printed dipole and patch antennas manufactured on grounded substrates with a similar ($\varepsilon_r = 12.8$) dielectric constant. Using the reported data, the ratio $d/\lambda_0 = 0.04$ for a 500 μm thick silicon

substrate at 24 GHz corresponds to approximately 60% antenna efficiency. However, in the case of on-chip antennas the problem of surface wave losses is normally lessened by the fact that the silicon wafer is diced into individual chips. Waves that enter the substrate are re-radiated into free space at the edges of the chip. If the extra phase shift is small, these re-radiated waves contribute to the main lobe of the antenna.

3.3 Cross talk mitigation

A major concern with on-chip antennas is the risk of cross-talk with the active on-chip circuits. The problem of cross-talk between slot antennas and integrated circuits due to unwanted parallel plate modes has been considered in Chapter II. In this section the impact of integrated circuit design and layout on cross-talk is treated.

3.3.1 Differential circuit topology

The use of differential topology in the integrated circuit reduces the coupling between the components and the antenna. Most of the capacitively coupled cross-talk in the near field of the antenna will appear as common mode components on the balanced signal lines. If the signal paths are routed in a way that the enclosed area formed by the two conductors of the balanced transmission line is small, the inductively coupled differential cross-talk will also be reduced. Furthermore, the use of a differential architecture removes the need for a stable on-chip RF ground as virtual signal ground points appear on the symmetry line of the circuit for balanced signals.

3.3.2 Subharmonic architecture

The architecture of the integrated receiver or transceiver has an influence over cross-talk. The most sensitive receiver type is the zero-IF receiver where the local oscillator (LO) of the receiver operates at the same frequency as the received signal. LO leakage picked up by the antenna causes self mixing, thus causing DC-offsets at the base band I/Q output of the receiver. In severe cases, the leakage can totally block the receiver. Similar problems can appear in transmitters as the radiated signal, including any applied modulation, might couple back to be oscillator and cause injection locking, instability and increased phase noise.

The problem of self mixing of the strong local oscillator signal can be solved with a subharmonic transceiver architecture, with the local oscillator operating at half of the frequency of the received or transmitted signal. If differential circuit topology is used throughout the system, no harmonics from the LO will appear at the receive or transmit frequency, thus largely eliminat-

ing the cross-talk problem. A block diagram of a proposed 24 GHz receiver architecture is shown in Fig. 3.5. Downconversion mixers for use in such a
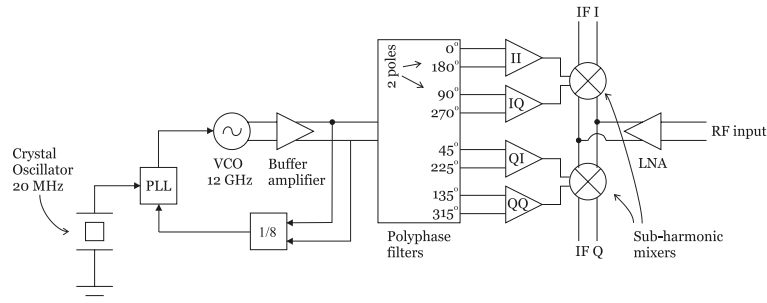

Figure 3.5: A 24 GHz subharmonic downconversion receiver based on the I/Q demodulator reported in [45].

receiver have been designed and evaluated [45]. A 24 GHz receiver equipped with such mixers is presented in [46].

3.3.3 Supply voltage filtering

The supply voltage for all the building blocks should be filtered to prevent cross-talk between individual circuit blocks such as the oscillator and the LNA. With an on-chip antenna, efficient filtering of the supply voltage becomes even more important as the long and widespread branches of the VCC rail can act as an unintended antenna. A combination of LC and RC filters in the decoupling network has been proposed [47] for highly integrated millimeter wave circuits in silicon technology. The network, shown in Fig. 3.6, employs compact low-pass RC-filters to isolate the supply of each stage within a block such as the LNA or oscillator. LC filters are used to low-pass filter the
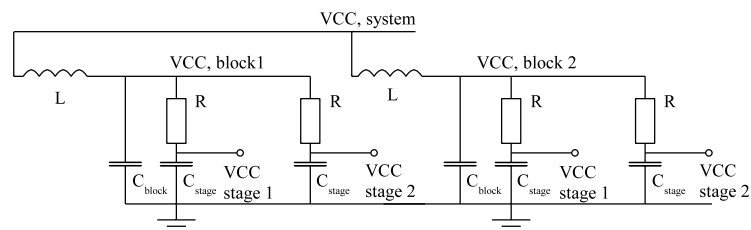

Figure 3.6: Multi-stage VCC decoupling network presented in [47].

supply current to an entire block, as RC-filters would have too large a voltage drop for the combined current consumption of multiple stages in a block.
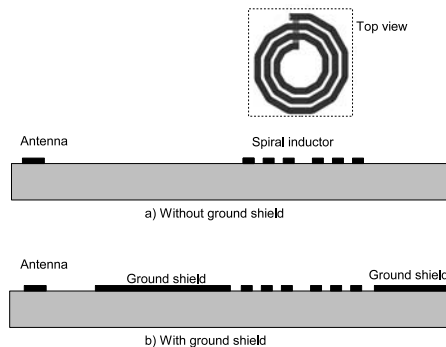
Figure 3.7: Cross-section of semiconductor substrate a) without and b) with ground shields around the spiral inductors.

3.3.4 Ground shields

The use of ground shields around spiral inductors has been shown [48] to reduce the cross-talk between adjacent inductors. A similar approach can be used to reduce the the cross-talk between the inductors and the antenna, as shown in Fig, 3.7. Currents induced in the shields will counteract the magnetic field coupling with the antenna. The grounded shields will also reduce the capacitive coupling. The main disadvantage of the ground shields is the reduced inductance and quality factor of the spiral inductors.

3.4 Implemented receivers

Integrated dipole antennas are demonstrated with a monolithic 24 GHz receiver [1] developed at the University of Ulm. Similar concepts have later been presented at higher frequencies by other groups [49].

The integrated receiver contains a low noise amplifier, local oscillator with a prescaler for locking LO to a reference signal using an external phase locked loop (PLL), quadrature down-conversion mixers and output buffers, as shown in Fig 3.8.

All circuits are fully differential, however fundamental mixing is used, thus making the design potentially susceptible to self mixing of local oscillator leakage signal picked up by the antenna. In the receiver layout ground shields are extensively used in the areas not occupied by the signal paths or components. The ground metallization is connected to substrate contacts in order to further reduce coupling between different stages and the antenna. The VCC supply voltage lines have been decoupled with the LC/RC network combination described in the previous section.

A proof of concept receiver with a simple integrated dipole, shown in Fig. 3.9, is presented in *Paper III*. Due to restrictions in the available wafer space the dipole was shortened by the addition of two top-loading extensions. An
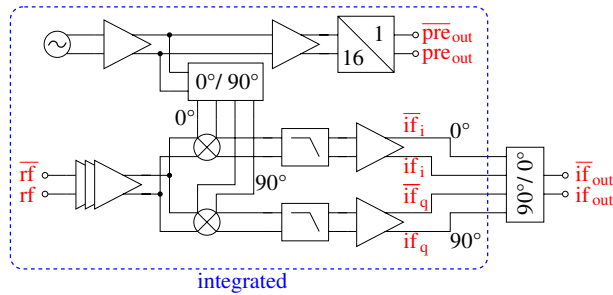
40

Figure 3.8: Block diagram of the 24 GHz receiver with integrated antenna. Picture courtesy of Ertugrul Sönmez, University of Ulm.
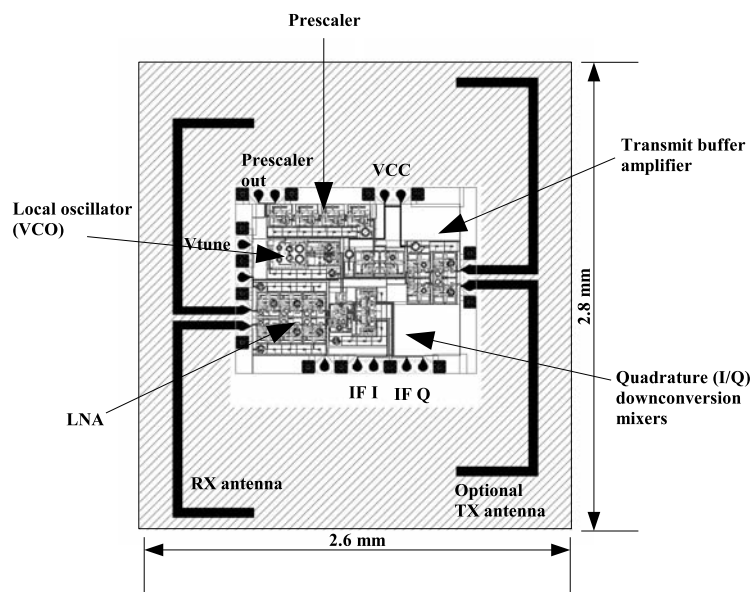
Figure 3.9: Layout of the the 24 GHz receiver with top loaded dipole presented in *Paper III.*

additional dipole was added and connected to the local oscillator through a switchable buffer to allow the circuit to be used as a simple frequency modulated transmitter. Although the shorted dipole yields a poor impedance and relatively high input return loss at 24 GHz, 33 dB conversion gain (relative to a zero gain down-converter with an isotropic antenna) has been measured for the receiver.

To improve the impedance match for minimum noise figure of the receiver and to reduce the size of the chip an improved, more compact folded dipole antenna has been developed. The full characterization of the antenna and receiver is presented in *Paper VI*. A chip photo of the receiver with the integrated folded dipoles is shown in Fig. 3.10. The input impedance of the on-chip antenna has been selected to match the required input impedance of 70+j40 Ω
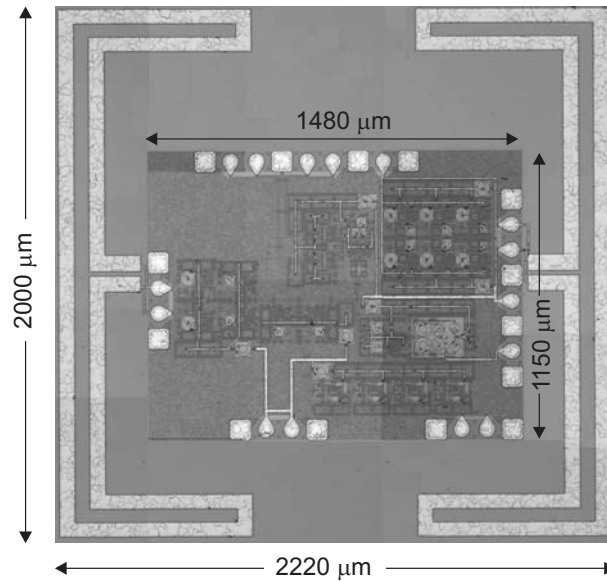
Figure 3.10: Monolithic 24 GHz receiver integrated with receive (left) and auxiliary transmit (right) folded dipole antenna.

for minimum noise of the receiver low noise amplifer (LNA). The impedance and gain were characterized with a separately manufactured antenna chip and show good agreement with simulations. The measured radiation pattern and gain of the passive antenna chip is shown in Fig. 3.11. A maximum gain of
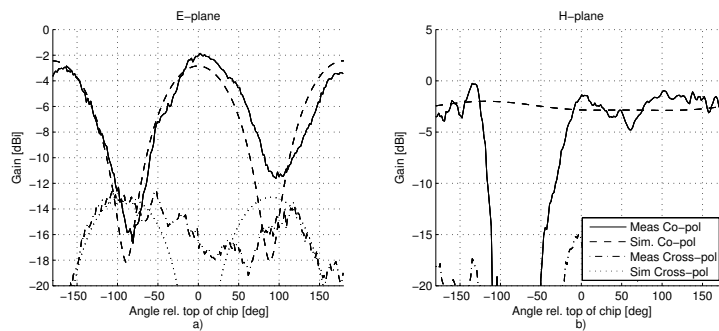
Figure 3.11: Measured and simulated a) E- and b) H-plane co- and cross-polarization radiation pattern and gain. H-plane angles between -110° and 0° shadowed by the probe setup.

-2 dBi is measured in the top side broadside direction. Despite the use of top loading sections perpendicular to the main axis of the dipole, the measured cross-polarization is lower than -12 dBi.

The conversion gain and noise performance of the implemented single chip receiver has been evaluated from the output spectrum, shown in Fig. 3.12, obtained when illuminating the chip with a 24 GHz continuous wave signal. A
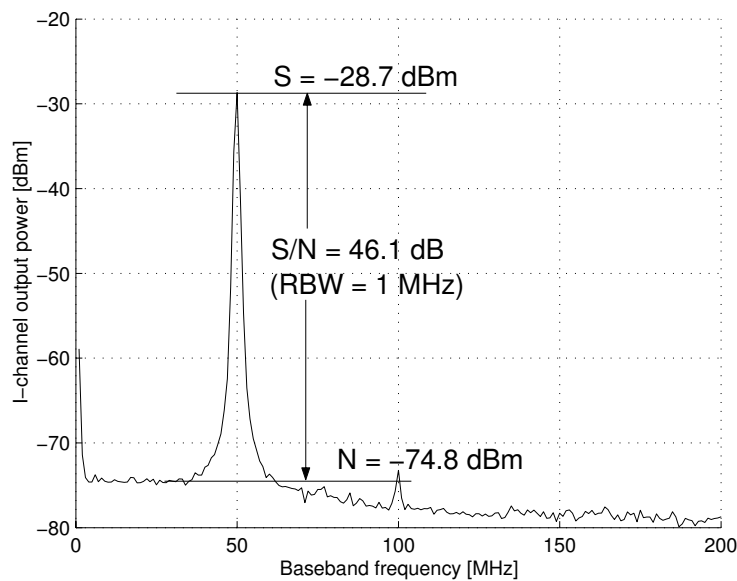
Figure 3.12: Receiver I-channel output when illuminated with a 5.9 dBm (EIRP) source at 1.25 m distance.

system noise figure of 8.8 dBi has been calculated, which is in good agreement with the separately measured noise figure 6.6 dB for the LNA and the -2 dBi gain of the antenna. It can thus be concluded that any substrate noise contribution to the total system noise figure is low.

3.5   Summary and conclusion

In this chapter, monolithic integration of dipole antennas with a single chip 24 GHz receiver has been demonstrated. The high resistivity silicon substrate option available in a commercial silicon germanium HBT process has been used to realize on-chip antennas with comparable performance to the micromachined radiators studied in Chapter 2. However, as high resistivity wafers are only available in a few commercial silicon processes, the choice of semiconductor foundries becomes limited for monolithically integrated antennas. The micromachining techniques, although more costly as additional post-processing of the manufactured circuits is needed, are in contrast applicable to almost any commercial silicon process.

4. Electrically Steerable Patch Arrays

The design of electrically steerable phased array antennas in the microwave frequency range has received considerable attention in recent years. Typical applications have been in radar where mechanically scanned antennas have been replaced by electrically steerable arrays. Many of the systems have been designed for military applications where the high cost associated with the multiple transmit/receive (T/R) modules needed have been acceptable.

Communication systems, such as cellular networks, have traditionally used fixed beam base station antennas, primarily due to cost. New concepts like MIMO (Multiple Input Multiple Output) utilize several antennas and transceivers at both the basestation and mobile terminal end to increase the capacity. However, there is also a need for simple beamsteering in basestation antennas for instance to dynamically adjust the down-tilt of the base station antenna to adapt the cell size or provide link budget enhancements.

In this chapter a base station antenna concept with beamsteering based on a traveling wave antenna is presented. By using a printed circuit board (PCB) design with microstrip phaseshifters and patch antennas closely integrated on the same layer, a low cost solution for beamsteering is proposed.

4.1 Application

One application of beamsteering in wireless networks is shown in Fig. 4.1. By adjusting the downtilt of the basestation antenna to the traffic pattern the link budget can be optimized while minimizing interference with neighboring cells. Today, the downtilt of the basestation antenna is usually mechanically set, either by physically tilting the antenna panel downwards or by using variable length transmission lines, set by a tuning screw, to electrically tilt the beam by feeding the individual elements of the array with different phases. Hence, the downtilt is seldom changed as it requires manual adjustments, although remotely controlled motors are available on the market.

Electronic phase shifters, allowing setting times less than ten nanoseconds, can be built with varactor diodes. Hence, it is feasible to change the downtilt for each time slot in a time division multiple access (TDMA) system in order to adapt the downtilt, and thus the size of the cell, depending on the distance to the user [50]. A beam steering range from $0°$ to $10°$ degrees below the horizon, is sufficient in a scenario where the basestation antenna is mounted in tower.
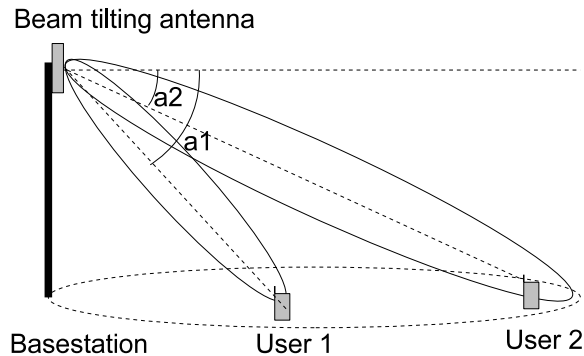
Figure 4.1: Application of electrically controlled beamtilt in a multi-user scenario for a time division multiple access (TDMA) system. The downtilt is switched for each time slot to provide maximum signal strength for the individual users.

Beamsteering can also be used in the azimuth plane to enhance the link budget and capacity with several users in a sector. In such applications, a wider steering range is needed as the sector width is usually 120°.

4.2   Traveling wave feed concept

In the classical phased array design, a corporate feed for the individual antenna elements in the array is normally used. Each element is connected through a phase shifter to a power divider which splits main feed. The traveling wave antenna is fed at one end with the signal propagating through the network, past antenna elements where part of the power is radiated. The remaining part of the signal at the end of the array is terminated in a dummy load in order to prevent reflections. The principal layout of the two feed types is shown in Fig. 4.2.   An advantage of the traveling wave feed is that all phase shifters are identical with a relatively small phase tuning range and are tuned synchronously to modify the beamtilt. The progressive phase shift needed to form the beam is generated by the array itself. In contrast, the corporate feed network needs different phase shifts for different tuning ranges which have to be calibrated to provide proper beam steering. The required phase tuning range is also larger for a given set of beam steering angles.

A characteristic behavior of traveling wave antenna is the exponential decay of the power as the signal propagates through the array due the power radiated and losses in the phase shifters and feed network. Hence, the far-end elements radiate less power than elements close to the feed. The array is normally designed so that only a small part of the power is terminated in the load. Wider patches radiate and attenuate the fed-through power more and are thus suitable for short arrays, however there is a limit on the maximum patch width which can be used before the radiators become overmoded. To reduce side lobes, the
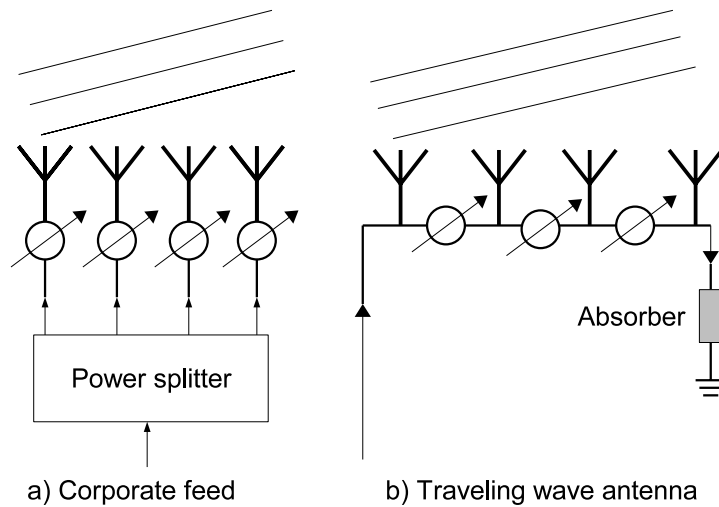
Figure 4.2: Schematic description of the a) traditional corporate feed b) Traveling wave antenna beamsteering configuration.

array can be tapered to arrange that more power is radiated by the elements in the center than elements close to the feed and terminating load. The tapering is accomplished by using patch antennas of different widths through the array.

4.3   Phase shifter design

In a series feed array a majority of the signal will pass through multiple cascaded phase shifters before it is radiated. The main requirement, along with a adequate phase tuning range, of the phase shifters such an array is therefore low insertion loss. For broadband operation of the array low group delay of the phase shifters is also desired. Excess group delays causes beam squint as the phase shift changes with frequency.

4.3.1   Transmission type phase shifter

Transmission type phase shifters (TTPS) consist of a transmission line section loaded with two variable reactances, as shown in Fig, 4.3. The TTPS can be readily adapted for use in traveling wave patch antenna arrays as the transmission line and the varactor stubs for tuning the varactor are easily implemented in microstrip technology. By using grounded stubs, the DC-control voltage can be applied to all phase shifters in the array through the signal conductor of the coaxial feed cable.

A limitation of the TTPS is the small phase tuning range. Larger phase tuning ranges increases the return loss and insertion loss of the phase shifter as the shunt loads create a missmatch at the connection point. However, due to
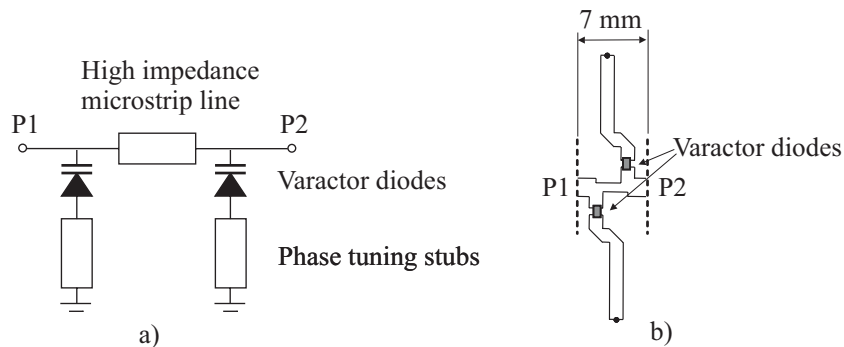
Figure 4.3: Transmission type phase shifter with varactor shunt loads a) schematic, b) layout of the 5.8 GHz microstrip typ used in *Paper VIII*.

its simplicity, the TTPS has several advantages such as low insertion loss, low group delay, and compact layout. It is thus suitable for traveling wave antenna applications where a small beam steering range is needed, such as for variable downtilt.

4.3.2 Reflective type phase shifter

The reflective type phase shifter (RTPS), shown in Fig. 4.4 uses the property of a 90° hybrid that termination of port three and four in equal reactive impedances causes all the incident power in port one to be reflected to the normally isolated port 2. In an analog phase shifter port three and four are

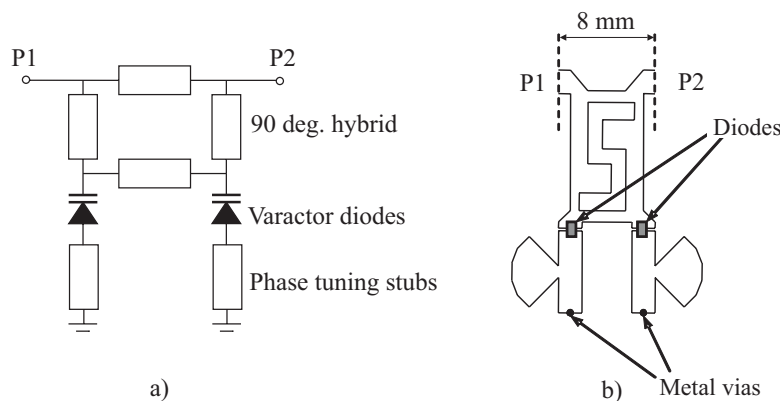*Figure 4.4:* Reflection type phase shifter with varactor diodes a) schematic, b) layout of the reduced size 5.8 GHz microstrip version reported in *Paper VII*.

terminated in varactor diodes. Ideally, no return loss is obtained over the entire phase tuning range while the insertion loss is determined by the loss of the hybrid and diodes. As in the case of the TTPS the phase tuning range can

48

be extended by adding stubs between the diodes and ground, however at the cost of lower bandwidth and increased group delay.

In a traveling wave antenna, an RTPS equipped with a standard 90° hybrid can be difficult to integrate in the same microstrip layer as the patch radiators. The 90° long transmission lines in an regular hybrid are usually too long to fit between two patches. This problem can be solved by the use of a modified, non equal length branch line coupler [51]. However, due to layout restrictions and manufacturing reasons a compact version of the unequal length branch line coupler is difficult to design. In *Paper VII* the design of a compact RTPS is presented. A modified unequal length branch line coupler is used where the low impedance branch lines have been replaced with asymmetric T-lines for compactness.

4.3.3 Non-linearities

A disadvantage of the varactor phase shifter is the inherent non-linear properties of the diode. The capacitance C of the varactor diode is modeled by

$$C(V_{tot}) = \frac{K}{(\varphi + V_{tot})^n} \tag{4.1}$$

as a function of the voltage V_{tot} over the diode where the parameters are diode dependant constants. As the total voltage over the diode consists of $V_{tot} = V_{DC} + v$, where V_{DC} is the constant DC control voltage and v the signal voltage the capacitance can be expanded in a power series

$$C(v) = C_0 + C_1 v + C_2 v^2 ... \tag{4.2}$$

where the C_2 term is the cause third order intermodulation products [52] which can appear close to the radiated or received signals. The non-linearity of the varactor diodes can be partly mitigated by using two diodes in an anti-series configuration [53], however the increased series resistance and lowered capacitance of the configuration leads to increased insertion loss of the phase shifter.

4.4 Implemented antennas

In *Paper VIII* the design and evaluation of two beamsteering antennas, implemented in hybrid technology on a standard 0.76 mm thick PTFE substrates, is described.

4.4.1 Vertical basestation antenna with adjustable downtilt

A ten-element array equipped with transmission type phase shifter between the elements is depicted in Fig. 4.5. The vertical radiation pattern, presented
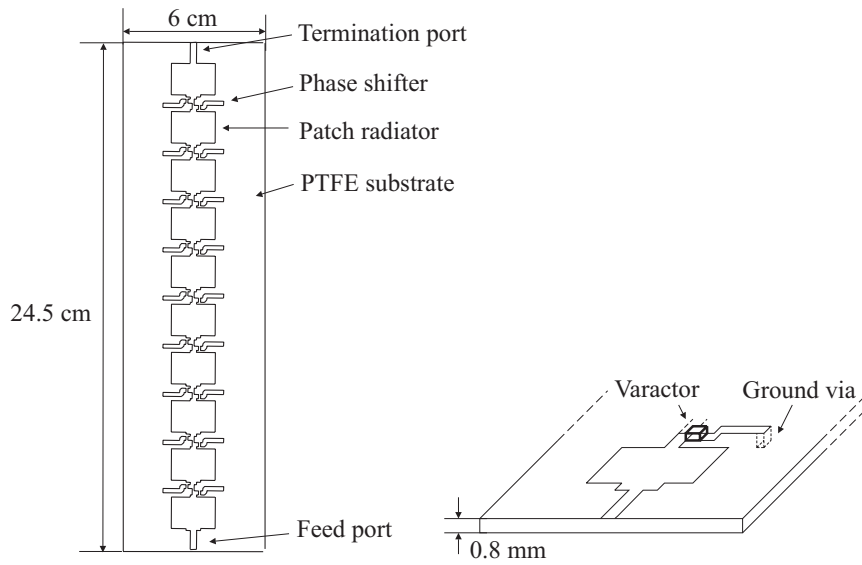
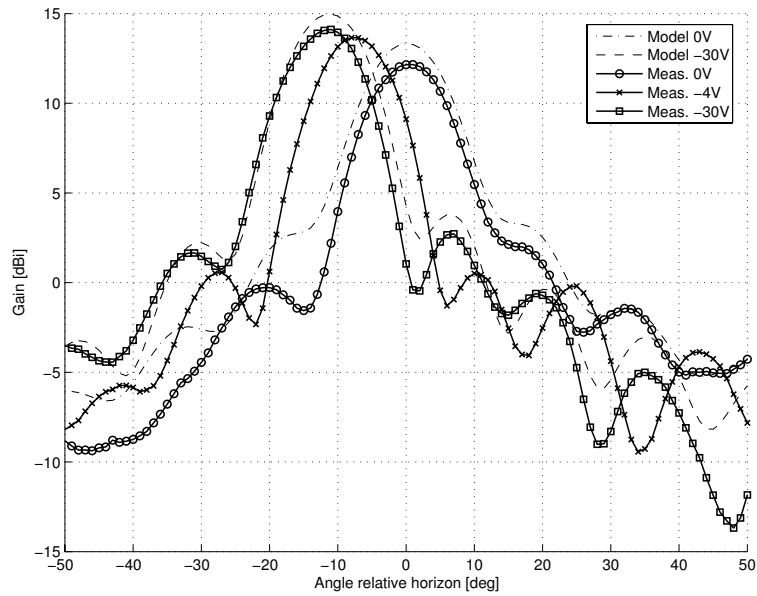*Figure 4.5:* Layout of the 5.8 GHz beam tilting antenna described in *Paper VIII*.

Figure 4.6: Measured beam tilt for different phase shifter control voltage settings. Theoretical radiation pattern obtained with a traveling wave model of the array included as reference.

in Fig. 4.6 can be controlled from 0° degree downtilt, corresponding to a beam directed towards the horizon, to a maximum downtilt of 10°. Lower gain is obtained at control voltages close to 0 V as the losses in the varactor diodes increase with lower reverse bias.

The third order non-linearity of the antenna has been measured with a standard two-tone test. For a 2x0 dBm excitation, the radiated third order products range from -42 dBc at 0V control voltage to less than -80 dBc at -4V reverse bias. The reflected non-linearity in feed port, defined as the ratio between the input power and third order products fed back to the source, range from -52 to -85 dBc. As seen from Eq. 4.1, the capacitance of the diode is a non-linear function of the total applied voltage. At the cost of a smaller beam steering range, the linearity of the antenna can be improved by avoiding low reverse bias of the varactors.

4.4.2 Wide-scanning antenna

To obtain the scan angle necessary for azimuth beamsteering within a 60° sector in a cellular system, phase shifters with large phase tuning ranges are needed, thus making the RTPS a proper choice. The tuning range requirement on the phase shifters can be relaxed by the use of a symmetric array. If the input port is switched between each of the two ends of the array, mirroring of the steerable range with respect to the broadside direction is obtained. An implemented 5.8 GHz five element array incorporating these features is shown in Fig. 4.7. The compact phase shifters presented in *Paper VII* are used to
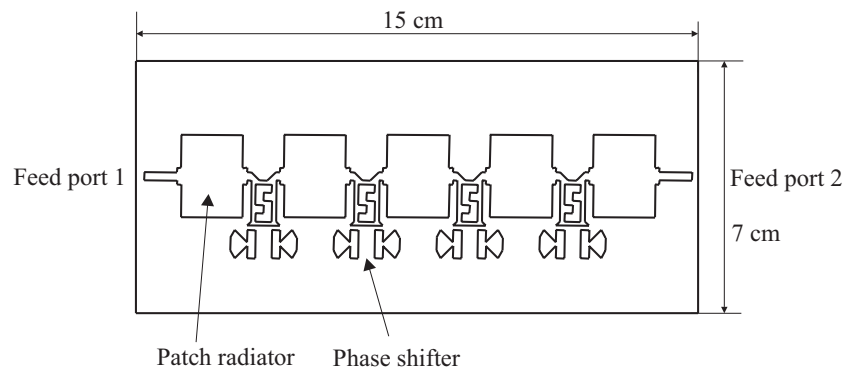
Figure 4.7: Five element wide scanning antenna equipped varactor RTPS.

allow the beam steering circuit to be fitted between the patches.

The E-plane radiation pattern for the wide-scanning antenna is shown in Fig. 4.8. For beam steering angles between -30 and -10 degrees the antenna is fed from the left side, while the 10 to 30 degree range is covered by switching the feed to the right port of the antenna. The broadside -10° to 10° range is covered by the relatively wide beam of the antenna.
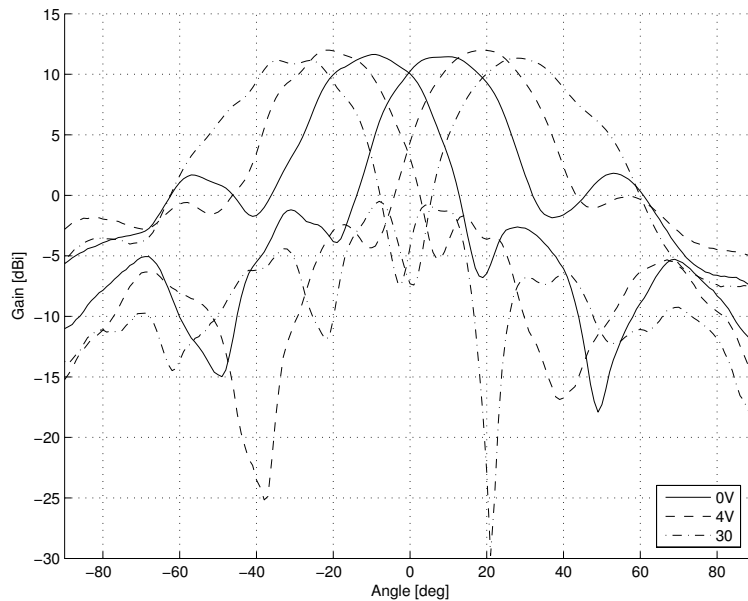
Figure 4.8: Wide scanning antenna radiation pattern for three control voltages. Symmetric mirroring of the patterns around the 0° broadside directions is obtained by switching the feed point.

4.5   Summary and suggestions for future work

In this chapter, a simple, low cost design concept for electrically steerable antenna arrays has been proposed. The main idea of using an electrically controlled progressive phase to steer the beam has been validated by the successful demonstration of two 5.8 GHz arrays. The measured radiation pattern shows good agreement with theoretical results obtained with traveling wave model of the array.

By the choice of appropriate production techniques and substrates, it should be possible to scale the demonstrated designs with frequency from the low frequency cellular bands at 800 MHz to 80 GHz vehicular radar applications. The main restriction at lower frequencies is the maximum practical size of printed circuit boards, while the high frequency limit is set by the component size and available integration techniques.

A practical limitation of the proposed designs is the low power handling capability of the varactor based phase shifters. Although the intermodulation distortion can be reduced by special diode configurations, the linearity will likely not be sufficient for high power applications. However, the traveling wave beam steering concept can be combined with integrated power amplifiers, as shown in Fig. 4.9, where a tapped transmission line is used to feed one power amplifier per array element.   In this application, the varactor phase shifters only carry a low power signal. An advantage of the active array is that
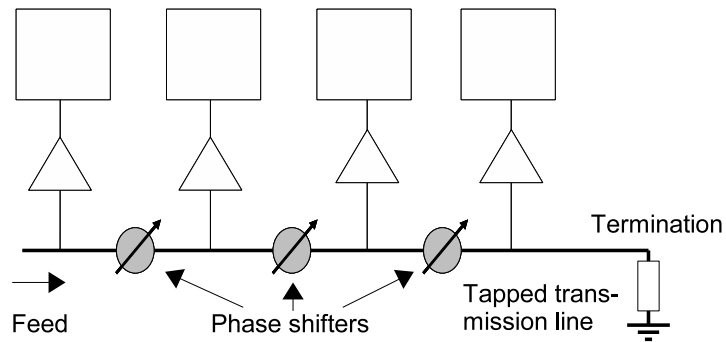
52

Figure 4.9: Proposed active transmit antenna array with electrically controlled progressive phase shift.

transmission lines with unequal length can be used for the taps to compensate for the beam squint caused by excessive group delay.

5. Conclusion and Outlook

The present work represents a higher level of integration between electronic components and radiating elements than what is common in commercial products today. Some compromises inevitably have to be made with regard to both the antenna and circuit performance when implementing both of these functions adjacent to each other on the same semiconductor substrate or printed circuit board. Hence, the use of integrated antennas has to be justified from a cost or system requirements perspective. In many cases, it is still advantageous to separate the antenna from the circuit through a specified interface, and apply optimum manufacturing technology and design methods for each of these system blocks. In these concluding remarks, the author's view of the suitability of the proposed integration techniques is given.

The on-chip antenna concept represents the most extreme form of antenna integration with active devices. Common arguments against the use of on-chip antennas are poor utilization of the expensive semiconductor substrate, low performance compared to external radiators, and cross-talk problems with the integrated circuit. The concept is however attractive for extremely compact systems or in the cases where off-chip RF-interconnects are to be avoided.

To address the size issue of on chip antennas implemented in silicon active device processes, a number of compact radiators for the 20-40 GHz frequency range has been proposed and evaluated in this thesis. The presented designs can quite easily be scaled to higher frequencies such as the 60 GHz and 77 GHz frequency bands. The lower frequency limit is primarily set by the maximum allowable die size, at least if antennas with reasonably high efficiency and bandwidth are required. For silicon circuits with a maximum die size of 10 mm^2, 20 GHz is likely the lowest reasonable frequency for integration of practical on-chip antennas.

The poor radiation efficiency of antennas manufactured on the low resistivity substrates commonly used in commercial silicon processes has been improved by the use of thick polymer layers, and selective micromachining of the silicon substrate. The necessary post-processing steps have a low temperature budget and should thus be IC-compatible. Despite the efficiency improvements, the maximum obtainable gain is however limited to 2-3 dBi due the low directivity of small on-chip radiators. While low gain antennas can find use in short range communication and sensing, gain improvements by appropriate packaging design should be further studied.

In this thesis, it has been experimentally demonstrated that cross-talk between an on-chip antenna and the integrated circuit can be managed by careful circuit design and layout. A combination of differential circuit topology and the use of ground shields and substrate contacts in the layout has reduced the cross talk to an acceptable level. A compact 24 GHz zero-IF receiver with an on-chip local oscillator and antenna, representing one of the most sensitive receiver architectures with regard to cross talk, has been successfully demonstrated with good performance. It should be possible to extend this receiver concept to a full transceiver. To further reduce the cross talk problem, a transceiver architecture based on subharmonic up- and down-conversion is proposed.

With regard to base station antennas for wireless communication, the main reasons why most commercial solutions still rely on simple, fixed beam designs are concerns regarding cost, complexity, and linearity. The printed circuit board integration of phase shifters and radiating elements in a single layer, as investigated in this thesis, addresses most of the cost and complexity issues. It has been shown that the performance of patch radiators is not significantly affected by the presence of phase shifters in the same microstrip layer as the antenna elements. Future work in this area should be directed at meeting the requirements of high linearity and power handling capability. High power transmitting applications could potentially be handled by splitting the single power amplifier in the transmitter into several smaller amplifier blocks, integrated adjacent to each of the antenna elements in the array. Another possibility of meeting the linearity requirements is the use of phase shifters with higher power handling capability. Switches and analog phase shifters based on RF-MEMS technology are particulary interesting for traveling wave antennas as such devices offer low insertion loss and improved linearity compared to the studied varactor diodes. However, the switching speed and the reliability need to be further studied.

6. Summary of Papers

Eight papers are appended to this thesis. Paper I, II, IV and V deal with micromachined antennas suitable for integration in commercial silicon active device processes. Monolithic integration of on-chip antennas is demonstrated in paper III and VI. Paper VII and VIII treat phase shifter and antenna design for electrically steerable traveling wave arrays.

6.1 Paper [I]: 24 GHz ISM-Band Antennas on Surface Micromachined Substrates for Integration with a Commercial SiGe Process

The use of thick organic polymers on top of low resistivity silicon wafers for the reduction of substrate losses in folded slot antennas has been reported in literature. In this paper the design and manufacturing of 24 GHz slot loop antennas with a 10-20 μm thick layer of BCB as an interface layer between the the antenna metallization and the substrate is described. Shallow front side etching of the silicon below the slots is also investigated. However, the main finding of the paper is that the obtainable gain and efficiency of an antenna on an on-chip antenna on low ohmic silicon without substrate micromachining is still low (20%). Cross-talk between the slot loop antenna and transmission lines of an integrated circuit within the aperture is analyzed by electromagnetical simulations. The excitation of parallel plate modes between the antenna groundplane and circuit metallization is found to be the dominant coupling mechanism. By short-circuiting the parallel-plate mode with via connections the cross-talk is reduced.

6.2 Paper [II]: Compact Micromachined Dipole Antenna for 24 GHz Differential SiGe Integrated Circuits

Transceiver circuits implemented in silicon technology benefit from the use of differential circuit topology due to the lack of a stable on-chip signal ground. Hence, a desirable property of an on-chip antenna is the balanced feed offered by a dipole antenna. As the standard half wave dipole is too space consuming, the use of a meander line for the reduction the dipole length is considered. A

24 GHz meander dipole antenna, suitable for integration on a 10 mm^2 large chip is implemented on a 2.5 mm^2 large BCB membrane. Despite the presence of a low resistivity silicon substrate, the implemented antenna yields 0.7 dBi gain. The impact of membrane size on antenna resonance frequency and impedance is shown to be small.

6.3   Paper [III]: Monolithic Integration of an Antenna with a 24 GHz Image-Rejection Receiver in SiGe HBT Technology

Two on-chip dipole antennas are integrated with a 24 GHz monolithic receiver circuit developed by the University of Ulm, forming a 7.3 mm^2 large single chip receiver module with no external high frequency interconnects. One antenna is used for the receiver input, while the other dipole is connected to a switchable local oscillator output, thus allowing the receiver to be used as as simple frequency modulated transmitter. High resistivity (1000 Ωcm) wafers are used in a Si/SiGe manufacturing process to improve the gain of the integrated antennas. For testing purposes, the implemented receiver has been mounted on a ceramic carrier. At 24 GHz, 33 dB conversion gain is observed.

6.4   Paper [IV]: Micromachined Inverted F Antenna for Low Resistivity Silicon Substrates

In this paper, a compact 24 GHz inverted-F antenna for integration with monolithic circuits manufactured on low resistivity silicon substrates is presented. To reduce the substrate losses, the silicon substrate in the vicinity of the antenna is etched away, leaving the radiator supported on a 10 μm thick BCB membrane. Two different methods, deep reactive ion etching (DRIE) and potassium hydroxide (KOH) wet etching, are used to release the membrane and the results are compared. Antenna chips of 3.8x3.8 mm^2 size are manufactured, where the radiator membrane requires 2.4 mm^2 area, leaving the rest of the substrate available for the integrated circuit. Measured in a free space environment, -0.7 dBi gain is obtained for the implemented antenna.

6.5   Paper [V]: Micromachined Loop Antennas on Low Resistivity Silicon Substrates

Slot and wire loop antennas manufactured on low resistivity silicon substrates are presented in this paper. The antennas are intended to be monolithically integrated on the same substrate as an integrated circuit, with the radiator po-

sitioned at the perimeter of the circuit die. Selective bulk micromachining is used to improve the efficiency of the implemented radiators and antennas by removing lossy silicon material in the high field regions of the chip. Radiators with better than 1 dBi gain are demonstrated at 24 GHz. An important result of the paper is that micromachined trenches of small (200 μm) width are sufficient for yielding substantial efficiency improvements compared to the non-etched substrate.

6.6 Paper [VI]: Monolithic Integration of a Folded Dipole Antenna with a 24 GHz Receiver in SiGe HBT Technology

This paper is an extension of *Paper III*. Improved folded dipole antennas are integrated with the monolithic 24 GHz receiver designed by the University of Ulm. Compared to the receiver presented in *Paper III*, the folded dipole provides a better impedance match to the low noise amplifier. Better utilization of the silicon substrate is also obtained due to smaller size of the integrated antennas. The system is characterized with regard to conversion gain, noise, baseband I/Q-balance and DC-offset. No degradation of the performance of the receiver due to substrate coupled noise is observed in the setup.

6.7 Paper [VII]: Compact Reflective Microstrip Phase Shifter for Traveling Wave Antenna Applications

Microstrip phase shifters can be integrated on the same substrate as patch antennas to form traveling wave antennas. The varactor tuned reflective type phase shifters offers a larger phase tuning range and lower return loss than comparable loaded line phase shifters. However, in order to fit between the patches on the antenna substrate the length in the signal flow direction of the phase shifter needs to be reduced. In this paper a compact reflective phase shifter using a modified non-equal length branch line coupler is described. To decrease the size of the the coupler while maintain reasonable transmission line dimensions the branch lines of the coupler are replaced with asymmetric T-line equivalents derived by ABCD-matrix analysis of cascaded transmission lines.

6.8 Paper [VIII]: Electrically Steerable Single-Layer Microstrip Travelling Wave Antenna With Varactor Diode Based Phase Shifters

The analysis and design of electrically steerable traveling wave patch antenna arrays is presented. Two 5.8 GHz arrays for basestation applications are built and characterized. A vertical array with variable downtilt, equipped with load line varactor phase shifters, yields between 0° and -10° degree beam steering range with a maximum gain of 13.9 dBi. A horizontal scanning array using the compact reflection type phase shifters presented in *Paper VIII* provides a maximum -32° to +32° beam steering range when scanned and fed from alternate ends. Non-linearity of the varactor phase shifters is discussed and the reflected and radiated third order intermodulation products of the implemented antennas are measured.

7. Swedish Summary

I denna avhandling beskrivs metoder för integration av antenner med aktiv elektronik, såsom mottagare och kretsar för lobstyrning, tillverkade på kiselsubstrat samt konventionella mönsterkort.

Inom överskådlig framtid kommer kisel att vara det helt dominerande halvledarmaterialet för produktion av aktiva elektronikkomponenter. Framsteg inom utvecklingen av transistorer i kiselgermaniumteknik (SiGe) gör att kisel även i ökad utsträckning används för integrerade kretsar i mikrovågsområdet. Ett mål med denna avhandling har därför varit att undersöka om antenner kan placeras på samma substrat (chip) som radiokretsar tillverkade i kommersiellt tillgängliga kiselprocesser. En fördel som uppnås genom att integrera antennen tillsammans med radiomottagare och sändare direkt på halvledarsubstratet är att man undviker behovet av elektriska förbindelser för de högfrekventa radiosignalerna. Därigenom kan enklare och billigare kapsling användas för kretsarna, samtidigt som förlusterna av mottagen eller utsänd signaleffekt minskar. På grund av de höga kostnaderna för kiselsubstratet krävs det dock att antennerna kan konstrueras på ett sådant sätt att de kräver liten yta.

Ett problem som måste lösas vid integration av antenner i kommersiellt tillgängliga halvledarprocesser är att de kiselskivor som normalt används vid tillverkningen ofta har hög elektrisk ledningsförmåga. Detta leder till att antenner som placeras direkt på kiselytan får låg effektivitet eftersom en stor del av de utsända eller mottagna radiovågorna absorberas av materialet. För att förbättra effektiviteten på antennerna undersöks det därför i denna avhandling om mikromekaniska tillverkningstekniker kan utnyttjas för att minska förlusterna i substratet. En kombination av polymerbaserad tunnfilmsteknik och torr- eller våtetsning föreslås användas för att efterbearbeta kiselsubstrat med aktiv elektronik. Den föreslagna processtekniken har använts för att konstruera och tillverka kompakta dipol-, loop- och inverterade-F-antenner för frekvensområdet 20 till 40 GHz. Det strålande antennelementet bäres upp av ett tunnt membran för att reducera förlusterna i halvledarsubstratet. Mätresultat för de studerade antennerna tillsammans med numeriska simuleringsresultat bekräftar att kraftigt förbättrad prestanda erhålles med den föreslagna bearbetningstekniken.

En komplett 24 GHz radiomottagare med antennen inkluderad på samma chip som övrig elektronik har konstruerats i samarbete med universitet i Ulm. Kretsen, som kräver mindre än 5 mm^2 kiselyta inklusive antenner,

har tillverkats i en SiGe-process i vilken högresistiva kiselskivor har kunnat användas. Därigenom har goda antennprestanda kunnat erhållas utan att mikromekanisk efterbearbetning har behövt utnyttjas. Ett kritiskt problem som har analyserats är överhörning mellan den integrerade kretsen och antennen. Stor överhörning kan leda till försämrade prestanda eller felfunktion då signaler från mottagaren läcker tillbaka till antennen. En viktig slutsats är att genom använda kretsar baserade på differentiell kretsteknik så kan överhörningen mellan antennen och radiokretsen hållas tillräckligt låg för att de båda komponenterna skall kunna placeras i närheten av varandra på samma chip. Dessutom är layouten av kretsen viktig, vilket har kunnat konstateras med hjälp av simuleringar. Möjliga applikationer för den utvecklade enchipsmottagaren är kortdistanskommunikation samt bilradar.

I framtida trådlösa kommunikationssystem kommer basstationsantenner med möjlighet att styra den utsända strålen mot aktiva användare vara ett betydelsefullt sätt att öka kapaciteten. Dessutom kan den totalt utstrålade effekten minskas. Styrbara antenner är idag ett område inom vilket det pågår mycket forskning samtidigt som kommersiella produkter lanseras på marknaden. Fortfarande begränsas dock användningen av stor komplexitet och höga priser på utrustning. Genom att placera komponenter för lobstyrning på samma substrat som antennelementen kan basstationsantenner med styrbarhet byggas till obetydligt högre kostnader än antenner med fasta lober. Möjligheterna till sådan integration har därför undersökts och två styrbara gruppantenner av vandringsvågstyp avsedda för framtida system i frekvensbandet kring 5.8 GHz har tillverkats och utvärderats. Konventionell mönsterkortsteknik har använts istället för monolitisk integration på kisel då den nödvändiga storleken på en gruppantenner vid lägre frekvenser gör det oekonomiskt att tillverka dessa direkt i en halvledarprocess. Genom användandet av en vandringsvågsantenn istället för den konventionella tekniken med individuell matning av varje element i gruppantennen förenklas konstruktion och kalibrering. Dessutom kan lägre krav ställas på de elektriska fasvridare som används för lobstyrningen.

Acknowledgements

First and foremost I would like to thank my supervisor, Prof. Anders Rydberg, for providing me with the opportunity to work in several highly interesting and challenging research projects, as well as giving me the freedom to develop my own ideas. I would also like acknowledge my assistant supervisor Prof. Sayan Mukherjee for his encouragement and support.

My gratitude goes to all the present and former staff members of the Signal and Systems group. In particular, I have enjoyed the help and friendship of my fellow co-worker Tekn. Lic. Peter Lindberg. I have also learnt a lot from discussions with my past colleagues Dr. Dhanesh Kurup, Dr. Mattias Wennström and Dr. Staffan Bruce, for which I am very grateful. In the last year of my studies, I have had the pleasure to work together with Dr. Henrik Kratz and M.Sc. Shi Cheng who have provided me with invaluable help.

I would like to thank the head of the Signals and Systems group Prof. Anders Ahlén for providing a pleasant working environment. I have made many friends during my years at the department, and I have truly enjoyed the numerous discussions about scientific and general topics held during coffee breaks and lunches. In particular, I would like to acknowledge the members of the Thursday club which used to consist of Ph.D. students, foreign guests and selected senior researchers meeting for dinner and a drink (or two). Among the long standing members of the group, I would specifically like to mention Dr. Tomas Olofsson and Dr. Mathias Johansson.

A large part of my work has been carried out together with people from other research group within the university, industry and other universities. During the first year of my studies, Dr. Mikael Lindeberg and Prof. Klas Hjort kindly helped me with the manufacturing of test structures in flex circuit materials.

I have had a very rewarding collaboration with Prof. Hermann Schumacher and his group at the University of Ulm, Germany. Specifically, I would like to thank M.Sc. Ertugrul Sönmez, M.Sc. Sebastièn Chartier, and M.Sc. Peter Abele, for help with layout and circuit design. Without your help, several of the integrated antenna circuits presented in this thesis would still only be device concepts. A special thanks goes to Dr. Wolfgang Schwerzel at Atmel Germany GmbH for admitting our quite space consuming designs to the SiGe2RF multi project wafer runs.

I am also very grateful for the help with the manufacturing of the micromachined antenna structures provided by Dr. Katia Grenier and other members of Prof. Robert Plana's group at CNRS/LAAS in Toulouse.

Finally, I would like to thank Dr. Paul Hallbjörner, who has tirelessly been proposing new ideas and research projects as well as provided me with good advice.

Erik Öjefors
September, 2006

Bibliography

[1] E. Sönmez, S. Chartier, C. Schick, and H. Schumacher, "Fully integrated differential 24 GHz receiver using a 0.8 μm SiGe HBT technology," in *Proc. of 35th European Microwave Conference (EuMC)*, Paris, France.

[2] H. A. Wheeler, "Small antennas," *IEEE Trans. Antennas Propagat.*, vol. AP-23, pp. 462–469, July 1975.

[3] L. J. Chu, "Physical limitations on omni-directional antennas," *J. Appl. Phys.*, vol. 19, pp. 1163–1175, December 1948.

[4] J. S. McLean, "A re-examination of the fundamental limits on the radiation of electrically small antennas," *IEEE Trans. Antennas Propagat.*, vol. 44, no. 5, pp. 672–676, May 1996.

[5] C. A. Balanis, *Advanced Engineering Electromagnetics*.   New York: Wiley, 1989.

[6] F. Bouchriha, K. Grenier, D. Dubuc, P. Pons, R. Plana, and J. Graffeuil, "Coplanar passive circuits on surface micromachined silicon and thick polymer layers for millimeter-wave applications," in *IEEE MTT-S International Microwave Symposium Digest*, vol. 2, Philadelphia, PA, United States, 2003, pp. 959 – 962.

[7] X. Huo, K. J. Chen, and P. C. Chan, "Silicon-based high-Q inductors incorporating electroplated copper and low-K BCB dielectric," *IEEE Electron Device Letters*, vol. 23, no. 9, 2002.

[8] K. E. Bean, "Anisotropic etching of silicon," *IEEE Trans. on Electron Devices*, vol. 25, no. 10, pp. 1185–1193, October 1978.

[9] F. Lärmer and P. Schilp, "Method of anisotropically etching silicon," German Patent No. DE 4,241,045.

[10] E. H. Klaassen, K. Petersen, J. M. Noworolski, J. Logan, N. I. Maluf, J. Brown, C. Storment, W. McCulley, and G. T. A. Kovacs, "Silicon fusion bonding and deep reactive ion etching; a new technology for microstructures," in *Digest of Technical Papers from Transducers'95/Eurosensors IX*, Stockholm, Sweden, 1995, pp. 556–559.

[11] K. Grenier, L. Mazenq, D. Dubuc, E. Öjefors, P. Lindberg, A. Rydberg, J. Berntgen, W.-J. Rabe, E. Sonmez, P. Abele, H. Schumacher, and R. Plana, "MEMS above IC technology applied to a compact RF module," in *Proceedings of SPIE - The International Society for Optical Engineering*, vol. 5836, Seville, Spain, 2005, pp. 504 – 515.

[12] G. P. Gauthier, A. Courtay, and G. M. Rebeiz, "Microstrip antennas on synthesized low dielectric-constant substrates," *IEEE Trans. Antennas and Propagation*, vol. 45, no. 8, pp. 1310 – 1314, 1997.

[13] I. Papapolymerou, R. F. Drayton, and L. P. Katehi, "Micromachined patch antennas," vol. 46, no. 2, pp. 295–306, February 1998.

[14] M. Zheng, Q. Chen, P. Hall, and V. Fusco, "Broadband microstrip patch antenna on micromachined silicon substrates," *Electronics Letters*, vol. 34, no. 1, pp. 3–4, January 1998.

[15] D. Neculoiu, A. Muller, P. Pons, L. Bary, M. Saadaoui, C. Buiculescu, O. Andrei, R. Enachescu, D. Dubuc, K. Grenier, D. Vasilache, I. Petrini, and R. Plana, "The design of membrane-supported millimeter-wave antennas," in *International Semiconductor Conference, CAS*, vol. 1, 2003, pp. 65–68.

[16] P. Caudrillier, A. Takacs, O. Pascal, H. Aubert, P. Pons, and R. Plana, "Compact circularly polarized radiating element for Ka-band satellite communications," in *IEEE Antennas and Propagation Society International Symposium*, vol. 1, 2002, pp. 18–21.

[17] D. Neculoiu, P. Pons, M. Saadaoui, L. Bary, D. Vasilache, K. Grenier, D. Dubuc, A. Muller, and R. Plana, "Membrane supported yagi-uda antennae for millimetre-wave applications," *IEE Proc. Microwaves, Antennas and Propagation*, vol. 151, no. 4, pp. 311 – 314, August 2004.

[18] Q. Chen, V. Fusco, M. Zheng, and P. Hall, "Micromachined silicon antennas," in *Proc. of the Int. Conf. on Microwave and Millimeter Wave Technology (ICMMT)*, Beijing, China, August 1998, pp. 289 – 292.

[19] G. Forma and J. Laheurte, "Compact oscillating slot loop antenna with conductor backing," *Electronics Letters*, vol. 32, no. 18, pp. 1633–1635, August 1997.

[20] D. Llorens, P. Otero, and C. Camancho-Peñalosa, "Dual-band, single CPW port, planar slot antenna," *IEEE Transactions on Antennas and Propagation*, vol. 51, no. 1, pp. 137–139, January 2003.

[21] F. Bouchriha, K. Grenier, D.Dubuc, P.Pons, R.Plana, and J.Graffeuil, "Minimization of passive circuits losses realized on low resistivity silicon using micromachining techniques and thick polymer layers," in *IEEE MTT-S International Microwave Symposium*, vol. 2, 2003, pp. 959–962.

66

[22] A. Bacon, G. Ponchak, J. Papapolymerou, N. Bushyager, and M. Tentzeris, "Folded coplanar waveguide slot antenna on silicon substrates with a polyimide interface layer," in *IEEE Antennas and Propagation Society International Symposium*, vol. 2, 2002, pp. 432–435.

[23] P. Abele, J. Konle, D. Behammer, E. Sonmez, K.-B. Schad, A. Trasser, and H. Schumacher, "Wafer level integration of a 24 GHz and 34 GHz differential SiGe-MMIC oscillator with a loop antenna on a BCB membrane," in *IEEE Microwave Symposium Digest*, vol. 2, 2003, pp. 1033–1036.

[24] Q. Chen, V. Fusco, M. Zheng, and P. Hall, "Silicon active slot loop antenna with micromachined trenches," in *IEE National conference on antennas and propagation, Conference Publication No. 461*, 1999, pp. 253–255.

[25] H. Nakano, H. Tagami, A. Yoshizawa, and J. Yamauchi, "Shortening ratios of modified dipole antennas," *IEEE Transactions on Antennas and Propagation*, vol. 32, no. 4, pp. 385–386, Apr 1984.

[26] M. Ali and S. S. Stuchly, "A meander-line bow-tie antenna," in *Antennas and Propagation Society International Symposium*, vol. 3, 1996, pp. 1566–1569.

[27] K. Fujimoto and J. R. James, *Mobile Antenna Systems Handbook*, 2nd ed. Artech House, 2001.

[28] R. King, C. Harrison, and D. Denton, "Transmission-line missile antennas," *IRE Trans. on Antennas and Propagation*, vol. 8, no. 1, pp. 88–90, January 1960.

[29] Z. Chen, "Note on impedance characteristics of L-shaped wire monopole antenna," *Microwave and Optical Technology Letters*, vol. 26, no. 1, pp. 22–23, July 2000.

[30] K. T. Chan, A. Chin, Y. B. Chen, T. S. D. Y.-D. Lin, and W. J. Lin, "Integrated antennas on Si, proton-implanted Si and Si-on-quartz," in *IEEE International Electron Devices Meeting*, 2001, pp. 903–906.

[31] E. Öjefors, H. Kratz, and A. Rydberg, "Membrane antenna for silicon based 3D integrated microsystems," in *Proc. MEMSWAVE Workshop*, Lausanne, Switzerland, June 2005.

[32] R. Sturdivant, C. Quan, and J. Wooldridge, "Investigation of MMIC flip chips with sealants for improved reliability without hermeticity," in *Proc. MTT-S Int. Microwave Symp.*, San Franscisco, CA.

[33] L. Li, B. Cook, and M. Veatch, "Measurement of RF properties of glob top and undercapsulant materials," in *Proceedings of Electrical Performance of Electronic Packaging*, vol. 1, 2001, pp. 121–124.

[34] E. Öjefors, "LTCC and glob-top packaging for 24 GHz MMIC with integrated antennas," in *GigaHertz 2003. Proceedings from the Seventh Symposium*, Linköping, Sweden, November 2003.

[35] U. R. Pfeiffer, J. Grzyb, D. Liu, B. Gaucher, T. Beukema, B. A. Floyd, and S. K. Reynolds, "A chip-scale packaging technology for 60 GHz wireless chipsets," *IEEE Trans. Microwave Theory Techn.*, vol. 54, no. 8, pp. 3387–3397, Aug. 2006.

[36] P. Russer, "Si and SiGe millimeter-wave ingrated circuits," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, pp. 590 – 603, May 1998.

[37] A. Schuppen, J. Berntgen, P. Maier, M. Tortschanoff, W. Kraus, and M. Averweg, "An 80 GHz SiGe production technology," *III-Vs Review*, vol. 14, no. 6, pp. 42 – 6, 2001.

[38] F. Touati and M. Pons, "On-chip integration of dipole antenna and VCO using standard BiCMOS technology for 10 Ghz applications," in *Conference on European Solid-State Circuits. ESSCIRC '03.*, 2003, pp. 493–496.

[39] B. Floyd, C. M. Hung, and K. K. O;, "Intra-chip wireless interconnect for clock distribution implemented with integrated antennas, receivers, and transmitters," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 5, pp. 543–552, May 2002.

[40] A. B. M. H. Rashid, S. Watanabe, and T. Kikkawa, "High transmission gain integrated antenna on extremely high resistivity Si for ULSI wireless interconnect," *IEEE Electron Device Letters*, vol. 23, no. 12, pp. 731 – 733, Dec 2002.

[41] C. A. Balanis, *Antenna Theory, Analysis and Design*, 2nd ed. Wiley, 1997.

[42] R. Lampe, "Design formulas for an asymmetric coplanar strip folded dipole," *Antennas and Propagation, IEEE Transactions on [legacy, pre - 1988]*, vol. 33, no. 9, pp. 1028–1031, 1985.

[43] D. B. Rutledge and M. S. Muha, "Imaging antenna arrays," *IEEE Trans. Antenna Propagation*, vol. 30, no. 4, pp. 535–540, July 1982.

[44] D. M. Pozar, "Considerations for millimeter wave printed antennas," *IEEE Trans. Antenna Propagation*, vol. 31, no. 5, pp. 740–747, Aug. 1983.

[45] P. Lindberg, E. Öjefors, E. Sönmez, and A. Rydberg, "A SiGe HBT 24 GHz sub-harmonic direct-conversion IQ-demodulator," in *Silicon Monolithic Integrated Circuits in RF Systems*, Atlanta, USA, September 2004.

[46] P. Lindberg, "Radio frequency integrated circuits for 24 GHz radar applications," Uppsala University," Licentiate Thesis, 2005.

[47] E. Sönmez, S. Chartier, A. Trasser, and H. Schumacher, "Isolation issues in multifunctional Si/SiGe ICs at 24 GHz,," in *Proc. of International Microwave Conference (IMS)*, Long Beach, CA, June 2005.

[48] J. H. Mikkelsen, O. K. Jensen, and T. Larsen, "Measurement and modeling of coupling effects of cmos on-chip co-planar inductors," in *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems Proceedings*, September 2004, pp. 37–40.

[49] A. Babakhani, X. Guan, A. Komijani, A. Natarajan, and A. Hajimiri, "A 77 GHz 4-element phased array receiver with on-chip dipole antennas in silicon," in *Proceedings of the 2006 IEEE International Solid-State Circuits Conference*.

[50] M. Andersson, B. Göransson, I. Skarin, K. From, S. Cheng, E. Öjefors, P. Hallbjörner, L. Manholm, and A. Rydberg, "Antennas with fast beam steering for high spectral efficiency in broadband cellular systems," in *Accepted by European Conference on Wireless Technology 2006*, Manchester, UK, September 2006.

[51] C. Toker, M. Saglam, M. Ozme, and N. Gunalp, "Branch-line coupler using unequal line lengths," *IEEE Trans. Microwave Theory and Techniques.*, vol. 49, no. 4, pp. 0–0, April 2001.

[52] R. Mayer and M. Stephens, "Distorsion in variable-capacitance diodes," *IEEE J. Solid State Circuits*, vol. SSC-10, no. 1, pp. 47–54, Feb 1975.

[53] A. Keerti, J. Xiang, and A.-V. Pham, "High power linearized rf phase shifter using anti-series diodes," *IEEE Microwave and Wireless Components Letters*, vol. 16, no. 4, pp. 200–202, April 2006.

[54] KMW RF & Microwave Products, "Active multi beam antenna system (amba)," http://www.kmwinc.com.

[55] L. Rexberg, N. Dib, and L. Katehi, "A microshield line loop antenna for sub-mm wavelength applications," in *IEEE Antennas and Propagation Society International Symposium*, vol. 4, 1992, pp. 1890–1893.

[56] A. Ghazinour, P. Wennekers, J. Schmidt, Y. Yin, R. Reuter, and J. Teplik, "A fully-monolithic SiGe-BiCMOS transceiver chip for 24 GHz applications," in *Proceedings of the 2003 Bipolar/BiCMOS Circuits and Technology Meeting*, Toulouse, France, 2003, pp. 181 – 4.

Acta Universitatis Upsaliensis

*Digital Comprehensive Summaries of Uppsala Dissertations
from the Faculty of Science and Technology* 221

Editor: The Dean of the Faculty of Science and Technology