Instructor's Manual
for

# ELECTRONICS

## A SYSTEMS APPROACH

## Second Edition

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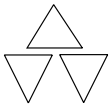

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# Preface

This instructor's guide is designed to assist lecturers and teachers using *Electronics: A Systems Approach - 2nd Edition*. The guide is divided into two parts – the first giving additional information on each chapter, and the second giving suggested solutions to the various exercises.

## Part 1 Chapter Objectives and a Guide to Presentation

This part of the guide outlines the objectives of each chapter and suggests ways in which students may be helped to gain maximum benefit from the material. The information on each chapter is divided into five sections:

**Objectives**

Sets out the major goals of the chapter. More information on this topic may be gained by reading the *Chapter Objectives* at the beginning of each chapter of the book.

**Background**

Places the material in the context of the earlier chapters and also describes how this material forms a basis for later work.

**Points to emphasize**

Stresses the most important aspects of the material in the chapter.

**Presentation of the material**

Suggests an approach to the delivery of the material in the light of the author's experience of giving courses based on this text over several years.

**The non-specialist reader**

Indicates certain sections of the chapter which may be omitted by the non-specialist without spoiling the continuity of the text or inhibiting comprehension of the remainder of the book.

## Part 2 Suggested Solutions to the Exercises

This section of the guide provides sample solutions to the various exercises in the text.

In many cases there is no *uniquely correct* answer to the problem given and thus the solutions must be taken simply as suggestions. In some cases the answer required is largely a repetition of material given in the text. In such cases the relevant section is indicated and no further discussion is given.

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*Warwick, February 1998*

# Contents

# PART 1

# Chapter Objectives and a Guide to Presentation

# Chapter 1
# ELECTRONIC SYSTEMS

## Objectives

To familiarize the reader with the basic concepts of analogue and digital systems, their applications and their limitations. Also to introduce, at the outset, a sound design methodology which will be developed later in the text.

## Background

This chapter makes few assumptions regarding prior knowledge. However, concepts introduced here will form the basis of much later work.

## Points to emphasize

- Electronic systems take inputs from sensors, process that information and produce output signals to drive actuators.
- Physical quantities are represented by electrical signals since these are easy to process, transmit and store.
- All electronic systems are susceptible to noise and distortion which ultimately limit their performance.
- Systems should be designed using a top-down approach encompassing a number of well established phases.
- A number of Electronic Computer Aided Design (ECAD) tools are available to assist the engineer. These tools complement the designer's skills, they do not replace them.
- A very important tool available to engineers is the circuit simulator. This gives an insight into the characteristics of a circuit without having to build it.

## Presentation of material

The points covered in this chapter can be most easily introduced with the use of a range of examples. Electronic systems are everywhere but are not always recognized as such. Illustrations of both analogue systems (such as televisions, radios and telephones) and digital systems (such as traffic lights, digital watches and computers) can be used to illustrate the sensors, actuators and processing used. It is also useful to point out that often analogue

quantities (for example temperature) may be sensed using digital sensors (for example a thermostat). This last point will be emphasized in the next chapter.

Noise and distortion may also be illustrated with examples from everyday life. The effects of noise and distortion are clear in such applications as radio and television, but other situations can also be used. An interesting example is the damage caused to electronic systems by lightning! Noise can be dangerous!

Design methodology is a new concept to many students at this stage of their course. Again, a top-down approach is best explained using examples (real or imaginary) and describing the various stages in turn.

One of the key themes throughout this text is the use of circuit simulation to aid the understanding of the various circuits discussed. Students should be encouraged at any early stage to start experimenting with packages such as PSpice so that they are ready to look at circuits as they are dealt with in later chapters. Students do not need a detailed understanding of simulation techniques in order to benefit from their use. The ability to simply load and run the demonstration files, and to observe the results, will allow students to increase considerably their understanding of the operation of the circuits concerned.

## The non-specialist reader

This short chapter contains many concepts which are of importance to everyone studying the subject. Experience shows that it is more often the students who do not see themselves as electronic specialists who have the most difficulty with these basics. Non-specialists should therefore not omit any of the material in this chapter. Traditionally, circuit simulation has been more widely taught to electronic students than to those of other disciplines. I would argue strongly that the use of such packages is a valuable tool for *all* students and would encourage any lecturer using this text to make use of this valuable, free, teaching aid.

# Chapter 2
# MEASUREMENT, SENSORS AND ACTUATORS

## Objectives

To give an insight into the ways in which electronic systems sense and influence the world around them, and to show how these determine the nature of the system's input and output signals.

## Background

Having introduced in Chapter 1 the concepts of sensors and actuators, this chapter looks in more detail at the processes of measuring and controlling physical quantities. By the end of this chapter the student should have an understanding of both active and passive forms of sensors and actuators, and should therefore be aware of the devices which will form the inputs and outputs of the amplifiers discussed in the next chapter. This chapter also gives a brief overview of oscilloscopes and digital multimeters.

## Points to emphasize

- Measurement involves a quantitative comparison between some quantity (the measurand) and a standard.
- All measurements are subject to errors of various forms and all are affected by noise.
- A wide range of sensors is available to measure different physical quantities.
- The achievable accuracy of measurement differs greatly from one physical quantity to another.
- Some sensors are *active* in that they generate an output voltage or current related to a change in the quantity being measured. Others are *passive* and simply change their physical attributes such as resistance, capacitance or inductance.
- Actuators of many forms are available for use in a wide range of applications. Some of these require inputs of only a fraction of a watt whilst others require many kilowatts.
- The choice of sensors and actuators has an enormous effect on the nature of the remainder of the system.

## Presentation of material

It is not proposed that students be encouraged to memorize the long lists of sensors and actuators included in this chapter. Rather, those included have been chosen to illustrate a range of techniques.

A problem experienced by many students is that they have not encountered the devices before and have difficulty visualising them and their application. Some devices are illustrated within the text but clearly the scope for including photographs is limited. In a small group environment this can be overcome by passing around examples of some of the sensors and actuators during the lecture (although this can be an expensive exercise). An alternative approach, which works well with larger groups, is to illustrate the lecture with pictures or diagrams of sample devices. Catalogues from component distributors are an excellent source of such material, which may be used to generate over-head transparencies easily using a photo-copier.

## The non-specialist reader

Engineers and scientists whose main area of interest is not electronics will often need to use electronic systems in association with their work. While it is unlikely that they will wish to perform a detailed analysis or design of an integrated circuit amplifier, they may well wish to use such a device within a monitoring or control system. In such applications a knowledge of sensors and actuators will be of great importance, and it is thought that the material in this chapter is of great importance to such readers and should not be omitted.

# Chapter 3
# AMPLIFICATION

## Objectives

To introduce the concept of amplification, and the various parameters which characterize the performance of an amplifier.

## Background

In the previous chapter is was noted that most sensors deliver little, if any, output power and are generally associated with small voltages or currents. Many actuators, on the other hand, require large input signal voltages/currents to drive them. Thus the scene has been set to discuss amplification as a means of making signals from sensors suitable for driving actuators. In this chapter amplifiers are treated largely as *black boxes* with circuit details being left until later.

## Points to emphasize

- Amplification makes thing bigger.
- Amplifiers may be of many different forms including mechanical, hydraulic, electrical and electronic.
- Amplifiers may be active or passive – most electronic amplifiers are active. Active systems take power from some external power source, such as a power supply.
- It often simplifies analysis to represent the inputs and outputs of a system by *equivalent circuits*. This allows a complete amplifier to be represented by an equivalent circuit which may be used to predict its response to external events.
- The performance of an amplifier may be characterized by a set of parameters including its gain, input and output resistances, frequency response and noise performance. If these characteristics are known the amplifier may often be used as a ‘black-box’ amplifier, without a detailed knowledge of its internal circuitry.
- Operational amplifiers are widely used as ‘black-box’ amplifiers. Such devices have a very high gain, a very high input resistance and a very low output resistance. These characteristics make them useful in a range of applications. However, the characteristics of real op-amps differ considerably from what one might term an ‘ideal’ amplifier.

- In less demanding applications much simpler circuits may be used to perform amplification. These often use single transistors or other active devices as the control element.

## Presentation of material

Surprisingly, many students find the concept of amplification quite difficult to grasp if it is presented directly in the form of a black-box amplifier. They are not confused by the fact that a voltage or a current is made bigger, but often they do not comprehend that an external power source is usually required to achieve this. I have found that the use of non-electronic examples (be they mechanical, hydraulic or other forms) greatly simplifies the task of grasping the principles of amplification. Once this has been achieved the need for a power source becomes obvious and the action of various circuits becomes clear.

This chapter highlights the desired characteristics of a general purpose amplifying device and contrasts it with those of real devices. It is important at this stage to emphasize that *all* real amplifying devices suffer from variability and have less than ideal characteristics. This illustrates the need for a means of overcoming these problems as discussed in the next chapter on feedback.

## The non-specialist reader

For many non-specialists this chapter will be one of the most useful chapters in the book since it deals with the basic building blocks of many instrumentation systems, the amplifier. Many lecturers may decide that all this material is essential for such students, though some may decide to omit much of Section 3.7. If this is done the first sub-section should be retained as an introduction to frequency response and cut-off frequencies.

# Chapter 4
# FEEDBACK

## Objectives

To introduce the concept of feedback and to illustrate its use in modifying the characteristics of amplifiers.

## Background

The last chapter looked at the various parameters which may be used to describe the performance of an amplifier, and outlined the characteristics of an 'ideal' general purpose device. These were compared with those of real operational amplifiers and it was noted that in many respects real devices fall well short of ideal behaviour. They also suffer from great variability. This chapter shows how feedback may be used to improve the performance of real amplifiers in many respects and this material forms a basis for later chapters which look in detail at circuitry used to implement amplifiers.

## Points to emphasize

- Electronic systems may be open-loop or closed-loop. In open-loop systems the goal guides the user in his choice of system inputs. In closed-loop systems the goal forms the primary system input.
- Most automatic control systems are based on closed-loop systems, be they electronic, electrical, mechanical, hydraulic or biological.
- Closed-loop control is an example of a *feedback system*. Such systems may be of two types, namely positive feedback and negative feedback.
- Negative feedback can be used to improve many aspects of the characteristics of an amplifier. In particular it may be used to reduce the variability of electronic systems by making them dependent on relatively stable passive components used in the feedback path, rather than the very variable amplifier used in the forward path.
- Negative feedback systems require a forward gain which is greater than that which would be necessary to achieve the required output in the absence of feedback.
- Using negative feedback it is possible to design a wide range of electronic systems using standard operational amplifiers. The use of feedback allows the designer to improve characteristics such as bandwidth, input resistance, output resistance and distortion performance, and also simplifies the process of design. The factor by

which the appropriate characteristic is improved is generally 1 plus the loop gain.

- The use of feedback brings with it possible problems of stability. These problems may be analysed using a number of techniques including Bode and Nyquist diagrams.
- Positive feedback is also of great importance, for example in the production of oscillators. The condition for oscillation is described by the *Baukhausen criterion*.

## Presentation of material

The use of every-day examples of closed-loop control systems (both analogue and digital) greatly simplifies comprehension of the concept of feedback systems. Examples such as the mechanical speed governor given in the text and others (such as the temperature regulatory system of the human body) are easy to understand and clearly indicate the various components and information flows.

Generation of the simple non-inverting amplifier of Section 4.4 from first principles demonstrates the use of feedback and leads into the use of standard cook-book techniques which allow a wide range of circuits to be designed and used without extensive analysis.

## The non-specialist reader

The early sections of this chapter are essential reading and the use of cook-book circuits is of great importance to the non-specialist. However, such readers could omit all but the first part of Section 4.6 – although instructors should summarize the main points of this section as it includes much useful information. Much of Section 4.7 could also be skipped without affecting the comprehension of later material although the first part of Section 4.7.1 should be covered as this discusses the criterion for oscillation. You may care to mention the problems of amplitude stabilization and should make students aware of the existence of crystal oscillators – the latter are discussed in later chapters.

# Chapter 5
# SEMICONDUCTORS AND DIODES

## Objectives

To explain the properties of semiconductor materials and to show how these may be used to make diodes and other useful devices. To outline the characteristics and uses of various forms of semiconductor diodes.

## Background

Thus far in the text we have treated amplifiers and other electronic systems as ‘black boxes’ and have said little about the circuitry inside them. In this chapter we begin to peer inside the box to look at its components. Here we look at semiconductor materials and diodes. In the following chapters we build on this material in the study of field effect and bipolar transistors.

## Points to emphasize

- Solid materials may be divided into: conductors, insulators and semiconductors. Their different electrical properties are determined by their valence electrons.
- Pure semiconductors are insulators at low temperatures but as they warm up electrons/hole pairs are formed due to thermal vibration generating mobile charge carriers and thus allowing *intrinsic* conduction.
- The addition of small amounts of impurities greatly affects the properties of semiconductor materials. *Donor* impurities give rise to an excess of free electrons and *acceptor* impurities produce an excess of holes. This produces *n*-type and *p*-type semiconductors respectively.
- The junction of *p* and *n* type materials forms a *pn* junction which has the properties of a semiconductor diode.
- Semiconductor diodes are near ideal devices but have associated turn-on and breakdown voltages.
- A number of special purpose diodes exist including: Zener diodes; light emitting diodes; laser diodes; photodiodes; Schottky diodes; tunnel diodes and varactor diodes.
- Diodes are used at the heart of a wide range of circuits including power supplies, radio detectors and wave-shaping circuits.

## Presentation of material

While students have little difficulty with the idea of electrons flowing under the influence of an electric field the idea of a current formed by holes is slightly more tricky. I like to use an analogy and here there are a number of options. One might consider a very large waiting room where people enter at the rear and take any available seat. Those at the front leave through one of a number of doors at the front as they become available. As chairs become vacant at the front people move forward filling the available spaces to be nearer the exit doors. Clearly there is a flow of people from the back to the front. The empty spaces however, move from the front to the back. There are similar analogies concerning, for example, cars in car parks.

Most students have come across semiconductor diodes in power supplies or other applications and therefore have some comprehension of the process of rectification. It should not be assumed however that they understand the properties that would be needed for an ideal diode.

## The non-specialist reader

Since the early sections are very brief I would suggest that it is worth getting students to read Sections 5.1 to 5.4 simply to give them an insight into the processing involved within semiconductor devices and to help with later chapters. Section 5.5 could be omitted, but not 5.6. Section 5.7 should be covered since Zener devices are widely used but Section 5.8 may be omitted if desired. The examples of Section 5.9 are of great benefit in establishing the characteristics of diodes in a range of situations.

# Chapter 6
# FIELD EFFECT TRANSISTORS

## Objectives

To describe the construction, operation, properties and applications of the various forms of field effect transistors.

## Background

Having looked at semiconductors in the last chapter we are now in a position to discuss simple active devices based on these materials. This chapter concentrates on analogue applications (although digital uses are mentioned) but the material in this chapter forms a vital basis for the work on digital devices in later chapters.

## Points to emphasize

- The low power consumption and small physical size of field effect transistors make them ideal for very large scale integration (VLSI). Most modern microprocessors and microcomputer memories are based on FETs.
- FETs may be divided into MOSFET and JFET types, and MOSFETs may be further divided into enhancement and depletion variants. These forms differ mainly in their biasing arrangements – their small signal characteristics are very similar.
- The relationship between drain current and gate-to-source voltage follows a square law. Over small ranges it may be acceptable to approximate this to a straight line.
- When considering small fluctuations of the input it is convenient to describe the operation of the device by a small signal equivalent circuit. In such circuits the operation of the device is normally characterized by its transconductance.
- Like all active devices FETs suffer from great device variability. This must be catered for in the design process.
- In addition to their uses within amplifiers FETs are frequently used in other applications such as: constant current sources; voltage controlled resistors; analogue switches and logical switches.

## Presentation of material

Many students are confused simply by the variety of FET devices. While the differences between MOSFETs and JFETs, and between enhancement and depletion devices should be explained, it is important to emphasize the similarities between these devices. Once the biasing differences have been covered they can be treated similarly as far as small signal considerations are concerned.

It is important to point out at an early stage the similarities between analogue and digital circuits. The operation of a simple linear amplifier and a logical inverter are similar except that in the former the input is constrained to be within certain limits and in the latter the input is constrained to be outside certain limits!

## The non-specialist reader

Sections 6.1 to 6.3 provide a general introduction to FETs and outline their characteristics and uses. These sections should not be omitted. Section 6.4 takes a more detailed look at characteristics and could be omitted if desired. Section 6.5 covers the main analysis of FET amplifiers. It can be omitted only by students who are destined to be users, rather than designers, of circuits.

Sections 6.6 and 6.7 provide an insight into the various uses of FETs and are not heavily analytical. These sections are important in that they highlight the diverse uses of FETs and also give a grounding for the digital material of later chapters. These sections should not be omitted.

# Chapter 7
# BIPOLAR JUNCTION TRANSISTORS

## Objectives

To describe the construction, operation, characteristics and applications of bipolar transistors.

## Background

Following on from the discussion of field effect transistors in the last chapter, we now turn our attention to bipolar devices. The chapter uses as its basis the material on semiconductors given in Chapter 5 and that given in Chapter 6 on equivalent circuits and amplifier design. Again, the emphasis is on analogue applications although digital circuits are also discussed as an introduction to the material on digital devices in Chapter 11.

## Points to emphasize

- Bipolar transistors, as their name implies, utilize charge carriers of both polarities. This is in contrast to FETs which are unipolar transistors.
- Bipolar transistors tend to have a higher gain and provide greater drive capabilities than FETs but generally consume more power.
- Bipolar transistors may be considered as current amplifiers. The relationship between the collector current and the base current is approximately linear.
- Alternatively they may be described by the relationship between the output current and the input voltage and be seen as transconductance amplifiers. If this latter approach is taken they may be represented in a manner similar to that used in the last chapter to describe FETs.
- Bipolar transistors may be described by a series of characteristics describing their input, output and transfer behaviour.
- A number of small signal equivalent circuits are available to model the behaviour of the device to varying levels of sophistication.These may be used to form models of complete amplifiers or other circuits.
- Bipolar transistors may be used in a number of circuit configurations and most circuits will use a number of stages cascaded together.

- In addition to their role within simple amplifiers, bipolar transistors may also be used to perform other functions in such applications as constant current sources, current mirrors, regulators and digital switches.
- A range of four-layer devices is also available. These components are of particular interest in high power applications. These are not transistors, but have many similarities with these components.

## Presentation of material

Many texts treat the bipolar transistor as a current amplifier and perform all calculations of gain on this basis. This text prefers to point out that it may be considered either as a current amplifier or as a transconductance device. The latter approach produces a much more elegant model in which the gain is of the same form as that previously derived for the field effect transistor in the last chapter.

When describing the behaviour of the simple common-emitter amplifier it is important to stress that this circuit is *not* one that we use in real applications because of its many unsatisfactory characteristics. Students have a tendency to remember this circuit when it is the one circuit we would rather they forgot! Unfortunately, it must be introduced, simply to illustrate why it is unsatisfactory.

## The non-specialist reader

Sections 7.1 to 7.4 provide a gentle introduction to bipolar transistors and should not be omitted. The bulk of the analytical material in this chapter is given in Sections 7.5 and 7.6. Some of this material could be missed by non-specialist students – the relevance of the various topics is left to the discretion of the instructor. Section 7.7 covers applications and should be of interest to non-specialists though could be left out if time were short. Section 7.8 gives a brief description of four-layer devices and Section 7.9 describes typical applications. These last two sections should not be omitted.

# Chapter 8
# ANALOGUE SIGNAL PROCESSING

## Objectives

To consider various aspects of analogue signal processing including filtering; amplifier classes; power amplifiers, noise and electromagnetic compatibility.

## Background

In earlier chapters we have considered amplification, feedback and the active components used to form amplifier circuits. We are now in a position to bring this material together to look at several aspects of more complete systems. Several topics covered in this chapter are picked up later when considering digital systems – for example the use of push-pull arrangements and considerations of noise.

## Points to emphasize

- Filters may be divided into passive and active types. Passive arrangements may be cascaded to provide arbitrarily high ultimate roll-off rates, but the transition from the pass-band to the stop-band is not sufficiently sharp for many applications.
- Active filters may be configured to provide a range of characteristics to suit particular applications. Common forms include Butterworth, Chebyshev and Bessel filters.
- Amplifiers may be divided into several classes. Typical classifications include classes A, B, AB, C and D.
- The distinction between the various classes relates to the fraction of the input cycle for which the active devices are conducting.
- Class D amplifiers are switching circuits where the output devices alternate between being turned ON and being turned OFF.
- Power amplifiers requiring low distortion, such as audio power amplifiers, usually adopt class AB.
- All electronic systems are affected by noise. Noise may be categorized into a number of classes: thermal noise; shot noise; 1/f noise and interference.
- Both bipolar transistors and FETs suffer from all these types of noise to a greater or lesser extent, but both may be used to produce high-performance, low-noise amplifiers.

- Bipolar transistors are generally superior in terms of noise performance when a low resistance source is used. FETs are superior for high values of source resistance.
- Electromagnetic compatibility (EMC) is related to the generation and affects of electromagnetic interference. There are many natural sources of such interference but perhaps the greatest problems are associated with interference that is man-made.
- EMC is affected by almost all aspects of a system's design, construction and use. Board layout and the use of screening are of particular importance.

## Presentation of material

Most power amplifiers adopt a push-pull arrangement of some form and it is useful to point out that the class in which the amplifier operates (that is class A, class B, etc.) is determined by the biasing arrangements rather than by any fundamental difference in the circuit. Normally this is determined by setting the quiescent current in the output stage to an appropriate value (either manually or automatically). Once this has been accepted the discussion can centre on the design of the output stage, without consideration of the class of the amplifier.

The use of active loads is an important concept, though it initially seems strange to students who are used to considering only discrete designs where the number of active components is usually low. It is useful to illustrate the use of active loads in real circuits such as operational amplifiers. Unfortunately, even simple operational amplifier circuits use more complex techniques then those covered thus far and so it is useful to lead students into such circuits gently. This is done in the design study which looks first at a simplified op-amp and then compares it with a real circuit.

EMC is a particularly difficult topic to cover in a useful and interesting manner. If care is not taken then presentation of this material can result in a long and tedious list of problems and design rules. Perhaps, at this level, it is more appropriate to give an overview of the problems involved and to leave detailed guidance on how to cope with the problems until later.

## The non-specialist reader

This chapter contains much material that is of use to students who do not see themselves as specialists in electronics. The first part of Section 8.2 is essential (8.2.1), as is the first part of Section 8.3 (8.3.1). Sub-section 8.4.1 provides an introduction to noise sources which should also be included. Much of the remainder of this section could be omitted without reducing the students' ability to cope with the remainder of the text. Section 8.5 on EMC contains much material that is of importance to all engineers and scientists since it relates to the interaction between real-world systems. Until recently few undergraduate courses included any material on EMC, but the introduction of various legislation in this area has focussed attention on this very important area.

# Chapter 9
# DIGITAL SYSTEMS

## Objectives

To introduce the basic ideas of digital systems and the techniques which are used to describe and design them.

## Background

Having looked in some detail at analogue systems we now turn our attention to digital matters. In Chapter 2 we looked at a series of digital sensors and actuators and in this chapter we investigate the functions necessary to take signals from the former and process them to generate outputs to control the latter. In this chapter we concentrate on combinational logic elements. In the next chapter we consider sequential systems before going on to look at the implementation of logic devices in Chapter 11. This material then forms a basis for the remaining chapters.

## Points to emphasize

- Binary variables are used to represent quantities which have two states. We often give labels to these two states such as: ON and OFF; true and false; and 1 and 0.
- Simple relationships between binary variables can often be represented using sensors and actuators such as switches and lamps. With more complex functions it is more convenient to describe such functions using Boolean algebra and to produce them using logic gates.
- Binary arrangements in which the outputs are determined only by the current states of the inputs are termed combinational logic. Any combinational logic function, no matter how complex, may be represented by a combination of simple gates.
- Logic functions may be described by a truth table which lists the outputs corresponding to each combination of the inputs. Logic functions may also be described by Boolean functions. These are not unique but may be manipulated using various identities and laws to allow expressions to be simplified. Graphical and automated, computer based methods are also available for simplifying logic functions.
- Sometimes groups of binary signals are combined to form binary words. These words may be used to represent various forms of information including both numeric and alphabetic data.

- Logic gates may be combined to form units which perform various operations concerned with binary arithmetic. Complex arithmetic calculations may be performed by suitable combinations of these simple units.

## Presentation of material

Despite the fact that most physical quantities are analogue, the world is full of binary sensors and binary actuators. It is useful to identify some of these devices to stress their binary nature.

The various laws and identities of Boolean algebra are rather impenetrable if treated simply as a set of rules. Relating them to real binary conditions, as in the text, makes their meaning clear. The use of light-hearted examples may also act as an aid to memory.

The material within this chapter covers the 'traditional' topics included within introductory courses in digital systems. One should however keep in mind the fact that the design of modern electronic systems very rarely makes use of some of these techniques! While it is (probably) advisable for electronic engineers to be aware of Karnaugh maps and Boolean simplification, we should not loose sight of the fact that *real* designs are more likely to use PLDs or microcomputers to produce logic functions. In such cases we are not interested in simplifying the logic functions but leave it to a computer pakage to fit or program the design. When was the last time *you* used a Karnaugh map in anger? Have you *ever* used a Karnaugh map in anger?

## The non-specialist reader

Sections 9.1 to 9.3 are probably essential reading for all students. Much of Section 9.4 is also necessary even for non-specialists, though some of the later material could be missed if time is short. Similarly the early parts of Section 9.5 are required to introduce number systems and binary arithmetic, although much of the material on arithmetic circuits could be omitted. Section 9.6 presents some useful examples of the use of the techniques covered earlier in the chapter and should not be omitted.

# Chapter 10
# SEQUENTIAL LOGIC

## Objectives

To introduce the principles of sequential logic and to describe a range of sequential arrangements including bistables, registers and counters.

## Background

In the last chapter we considered combinational logic circuits and the various techniques which are used in their design. Here we move on to sequential systems, initially viewing these as combinational logic with the addition of some form of memory within a feedback path. Various elements are discussed, all based on the simple gates developed in the last chapter. The next chapter will consider the implementation of these circuits. The registers and memory elements discussed within this chapter will form a basis for the discussion of microprocessors in Chapter 12.

## Points to emphasize

- Sequential systems may be divided into *synchronous* systems, which change state only at times determined by a clock signal, and *asynchronous* systems, which may change state at any time in response to changes in their inputs.
- Amongst the most common sequential building blocks are the various forms of multivibrator. These may be divided into bistables, monostables and astables.
- Bistables have two stable states. These may be of many forms including level sensitive types which are also called latches; edge-triggered types which are also called flip-flops; and pulse-triggered types which are also called master/slave flip-flops.
- A monostable has one stable and one quasi-stable state. When triggered by an appropriate input signal it will leave its stable state and enter its quasi-stable state. It will remain in this state for a period of time determined by circuit parameters and then return to its stable state. Such circuits are also called one-shots.
- An astable has two quasi-stable states and has the characteristics of a digital oscillator. The time spent in each state is determined by circuit components.
- A number of bistables may be combined to produce a register. Several forms of register are possible and circuits of this type are used as the basis of memory registers within microcomputers and other digital circuitry.

- Another form of register is the shift register which is used to perform parallel to serial and serial to parallel conversion within communications systems.
- Bistables are also used to produce various types of counter. These may be synchronous or asynchronous in nature. Large counters are usually formed by cascading smaller counters.
- Both synchronous and asynchronous sequential systems may be designed by adopting a systematic approach. The design of synchronous systems is slightly simpler since timing and stability constraints are less demanding.

## Presentation of material

When discussing the design of sequential systems it is very easy to loose sight of the relevance of the material being presented. As experienced engineers we know that the counters and registers being discussed form the basis of countless applications and it is easy to forget that students often lack this insight. Simple applications of S−R latches or shift registers are often slightly contrived but they are useful in illustrating the uses of these components. It is also important to stress the uses to which registers are put within more complex systems.

## The non-specialist reader

Sections 10.1 to 10.11 are of importance to all engineers although the relevance to non-specialists decreases as we move through these sections. Instructors must use their own judgement as to how far to progress through this material. Missing out the latter sections will not greatly impair the students' ability to cope with the remainder of the text. Section 10.12 is an advanced topic and should be omitted for those not specializing in electronics.

# Chapter 11
# DIGITAL DEVICES

## Objectives

To describe the physical implementation of the various digital elements discussed in the last two chapters. To introduce the major device families used and to outline their characteristics.

## Background

In the last two chapters we have discussed both combinational and sequential logic elements. In this chapter we look at the implementation of various digital systems and at the physical limitations which this places on their behaviour. This material is essential for the application of the techniques so far covered and is also required as a basis for the work on microcomputers in the next chapter.

## Points to emphasize

- Modern digital circuitry is invariably constructed using integrated circuits (i.c.s) rather than discrete components.
- Various levels of integration are possible from circuits containing perhaps a handful of gates (SSI) to circuits with hundreds of thousands of gates (VLSI).
- Logic gates may be constructed using either bipolar transistors or field effect transistors. When discussing digital systems it is more common to refer to the latter as MOS circuits rather than as FET circuits.
- Bipolar transistors switch quickly but suffer from *storage time* if the device saturates. This problem may be reduced by gold doping to reduce the storage time or by various means of preventing the device from entering saturation.
- MOS devices do not suffer from storage time and have high input resistances allowing one gate to drive many other gates. However they have a relatively high output resistance which reduces their speed of operation. MOS devices have a low power dissipation and require very little chip area and so are very attractive for large scale integration.
- The most popular bipolar logic families are the various forms of transistor-transistor logic (TTL). These range from the standard 7400 types through ranges optimized for speed, power consumption or other characteristics.

- The most widely used MOS family in recent years is complementary MOS (CMOS). This has the advantages of very low power consumption and high immunity to noise. Advanced versions are also capable of very high speed operation.
- In many cases it is necessary to connect TTL and CMOS circuitry. The differing characteristics of these families means that some form of *interfacing* is required to produce compatibility.
- When a design requires the use of more than a handful of logic gates it is normal to look at the use of some form of PLD. These may contain thousands of gates within a single package but allow the user to define how they are interconnected.
- A wide variety of PLDs is available. In applications that require a relatively low complexity then probably PALs are the most widely used. These are often used for replacing large numbers of conventional logic gates. If greater complexity is required then complex PLDs (CPLDs) or field programmable gate arrays (FPGAs) are used. In very high volume applications it may be feasible to design custom integrated circuits.
- All electronic circuits are susceptible to noise. Even small amounts of noise may cause problems by causing a 1 to be read as a 0, or vice versa. Large amounts of noise may cause actual physical damage to the circuits.

## Presentation of material

The operation of most MOS logic gates is straight forward and rarely causes too many problems. TTL on the other hand is slightly more complex and I believe that it is best introduced gradually. In the text the design of TTL is achieved as a result of looking at a number of simpler forms and identifying problems with each. The simpler forms of gate (DTL for example) are not important in themselves, but act as a very good introduction to TTL.

## The non-specialist reader

Sections 11.1 and 11.2 give a good introduction to digital devices and this will be sufficient for most non-specialists who may then omit Sections 11.3 and 11.4. Instructors may choose to include a brief look at Section 11.5 (array logic) but should certainly cover at least the first part of Section 11.6 (11.6.1 and 11.6.2) which looks at noise in digital systems.

# Chapter 12
# MICROCOMPUTERS

## Objectives

To describe the construction, operation and use of microcomputers.

## Background

In the last few chapters we have looked at the form of both combinational and sequential logic circuits and at their implementation using modern device technologies. In this chapter we look at a very important area of digital systems – that of microprocessors and microcomputers. This material forms a basis for that covered in the next chapter where we look at the components of typical data acquisition systems, and in the final chapter, where we compare various methods of system implementation including both programmable and non-programmable forms.

## Points to emphasize

- The development of the microprocessor allowed the great potential of very large scale integration (VLSI) to be realized.
- A microprocessor is a single chip implementation of one of the main sections of a computer – the central processing unit (CPU).
- To form a useful computer other components are also needed, these being some memory and input/output facilities.
- It is possible to get all the major components of a computer within a single VLSI component. This is termed a single chip microcomputer.
- The low cost and small size of these VLSI components have turned the computer from a scientific tool into an engineering component.
- At the heart of all computers is an array of registers. These are found in the processor, the memory and in the input/output sections. Communication between the various registers takes place over a bus system.
- Although all microprocessors have a slightly different architecture, the overall form of the devices is similar. Each obeys programs by sequentially fetching, and then executing, instructions from memory.

- All microcomputers require some form of memory. This will usually be a combination of ROM and RAM. A typical 8-bit microprocessor has an addressing range of 64 kbytes. 16-bit devices invariably have a much larger addressing range.
- The input/output section is the most application specific part of the computer. Its form will depend greatly on the nature of the sensors and actuators used within the system. Various methods of input/output control are possible including program controlled, interrupt driven and direct memory access techniques.

## Presentation of material

Some lecturers consider that the microcomputer may be considered simply as a ‘black box’. My own view is that it is much easier to understand and use components if one has at least a conceptual idea of what is going on inside. I therefore advocate a look inside the box to show that it consists of little which is more complicated than the registers and logic gates considered earlier.

The text says little about computer software and no programming examples are given. My reason for this is that as soon as programming is introduced the discussion becomes strongly processor dependent. If instructors are committed to a particular microprocessor then examples may be easily presented if desired. My own experience is that programming is usually taught separately from the hardware of microprocessors and I would suggest that there may be some advantage in covering the general principles of these devices first, before moving on to consider the detail, and programming, of specific processors.

## The non-specialist reader

A good understanding of the basics of microcomputer applications is essential for all engineers and scientists. Sections 12.1 and 12.2 are a good introduction to the subject and should not be omitted. Instructors must decide what of the material of Sections 12.3 to 12.6 is essential for their students. Some may be considered to be too detailed for the non-specialist though much of it is useful for the system integrator as well as the designer.

# Chapter 13
# DATA ACQUISITION AND CONVERSION

## Objectives

To describe the major components and operations involved in data acquisition and conversion.

## Background

Having looked at many of the characteristics of both analogue and digital systems we are now in a position to look at the problems of converting analogue signals into a digital form, and vice versa. The ability to process information in either an analogue or a digital form gives the designer a choice of implementation technique. This topic is discussed in the next chapter.

## Points to emphasize

- Signals may often be processed, transmitted and stored more easily in a digital form than in an analogue form. Noise is also less troublesome in digital systems.
- We therefore often choose to convert analogue signals into a digital form before processing/transmission/storage. It may then be necessary to convert these signals back to an analogue form.
- Conversion from analogue to digital is performed by *sampling* the signal and then digitizing the resultant data using an analogue to digital converter (ADC). Providing that sampling is performed at a sufficient rate (the Nyquist rate) no information is lost due to sampling.
- Signals may require filtering to remove high frequency components before sampling to prevent aliasing.
- Conversion from a digital form to an analogue form is achieved using a digital to analogue converter (DAC). Again filters may be needed to remove the effects of sampling.
- A wide range of both ADCs and DACs is available. These differ in resolution, speed, accuracy and cost.
- Sample and hold gates may be used to sample a number of signals simultaneously and to hold them so that they may be digitized sequentially by a single ADC. They may also be used to hold the output of a single DAC to provide multiple outputs.

- In systems with a number of inputs or outputs it is common to use some form of multiplexing to reduce the number of converters required.

## Presentation of material

It is not uncommon for students at this stage in their course to be unaware that sampling at a minimum rate is necessary to adequately describe an analogue signal. The requirement is quickly illustrated by taking an obvious example. One might, for instance, point out that while sampling the temperature of a room once every minute might give a good picture of temperature fluctuations, sampling the height of sea water once a minute would not give you a good picture of the nature of the waves present. From this it is fairly easy to illustrate the relationship between the required sampling rate and the maximum frequency component of the signal. It is important to note that students often have more difficulty with the other result of Nyquist's theorem. That is, that one gains no additional information by sampling at higher frequencies. It is tempting to think that the faster one samples the better picture one gets. This must be explained.

## The non-specialist reader

Data converters are invariably bought as standard i.c.s and so the internal construction of these devices is not of paramount importance to non-electronic specialists. However, the principles of sampling and multiplexing are important since problems will arise if these are wrongly applied. It is therefore appropriate for such students to cover Sections 13.1, 13.2 and 13.4, but to omit Section 13.3. They thus omit the bulk of the material in this chapter.

# Chapter 14
# SYSTEM DESIGN

## Objectives

To outline and justify a top-down methodology for system design; to discuss several aspects of the choice between technologies; and to describe the use of automated tools in electronic design.

## Background

In Chapter 1 we looked at the various stages of system design, mentioned briefly the choice of technology to be used and noted the existence of various automated design tools. In this final chapter we return to these topics with the benefit of the knowledge gained in the body of the text.

## Points to emphasize

- A good design is one that solves a problem in the most appropriate and efficient manner.
- The normal method of achieving a good design is to adopt a top-down approach.
- Major components of the design process include: the customer requirements; top-level specification; top-level design; detailed design; module testing and system testing.
- Top-level design is normally followed by bottom-up testing.
- At an early stage it is necessary to decide on the method of implementation to be adopted.
- Technological decisions include a choice between analogue and digital techniques, between integrated and discrete approaches and between the various device families.
- A wide range of automated tools is available to simplify the design process. Packages are available for schematic capture, circuit simulation, PCB layout, PLD layout, VLSI layout and design verification.
- Automated tools complement the designers skills, they do not replace them.

## Presentation of material

System design is generally considered to be a difficult topic to teach at any level and is usually not attempted at this early stage in a course. Indeed many students never cover some of the topics introduced within the first few pages of the text and expanded in this final chapter. While it is true that many students will not perform complete design projects in their early years of study, it is important to instill an understanding of the nature of the task and its various components. If this is not done we will perpetuate the practice, common in much student project work, of writing the specification after the design to match what has been achieved. This does little to prepare students for the realities of engineering within industry.

## The non-specialist reader

Sections 14.1, 14.2 and 14.3 are essential reading. Section 14.4 on electronic design tools could be omitted for non-specialists if required.

# PART 2

# Suggested Solutions to the Exercises

# Chapter 1
# ELECTRONIC SYSTEMS

**1.1** Often one's perception of whether a quantity is continuous or discrete will change when considering it from a microscopic, a macroscopic or even a relativistic viewpoint. Likely choices in these cases might be:

| | |
|---|---|
| *temperature* | – continuous |
| *displacement* | – continuous |
| *force* | – continuous |
| *humidity* | – continuous |
| *light intensity* | – continuous or discrete |
| *time* | – continuous |
| *mass* | – continuous or discrete |

Note that in the real world *most* physical quantities are continuous when viewed at a macroscopic level.

**1.2** There are numerous acceptable answers to this question. Quantities that are continuous include:

*strength*
*colour*
*reflectivity*

Quantities that may be considered to be discrete might include:

| | |
|---|---|
| *population* | |
| *price* | |
| *file length* | – (of a computer file) |

Quantities that could be considered to be either include:

| | |
|---|---|
| *frequency* | – depending on the situation |
| *probability* | – depending on the situation |
| *volume* | – depending on the situation |

**1.3** This question is intended to be answered at a relatively simple level and so normal responses might be that voltage or current can be used for direct current signals, and voltage, current, phase or frequency can be used for alternating (sinusoidal) signals. If one permits the use of digital/pulse techniques then one could also use the various pulse modulation techniques such as PAM (pulse amplitude modulation), PPM (pulse position modulation) and PWM (pulse width modulation) which are analogue modulation techniques, and PCM (pulse code modulation) which is a digital modulation technique.

**1.4** In practice any processing operation is acceptable since they are inevitably used in some form of signal or image processing. Possible examples include:

| | |
|---|---|
| *addition* | *differentiation* |
| *subtraction* | *multiplication* |
| *comparison* | *division* |
| *integration* | *averaging* |

**1.5** This question could be interpreted in two ways. Perhaps the most likely response is that the television antenna is the sensor and the cathode ray tube and the speaker are the actuators. In this case the physical quantity being measured is electro-magnetic field intensity which is continuous.

Alternatively, one could perhaps interpret the word television to represent the complete television network. In this case the sensor (at the television studio) is the TV camera, and the quantities being measured are light and sound intensities - which are both continuous.

**1.6** Personal computers include a number of sensors and actuators. The primary sensors are the switches that make up the keyboard, and the position sensors and push buttons in the mouse. The primary actuators are the display within the monitor and any speakers.

The quantity being detected by both the keyboard and the mouse is displacement. Movements of the hands of the operator are presumably continuous, although the sensors interpret these to produce digital outputs. For example, a key is either pressed or not. The information fed to both the display and the monitor are discrete since they are produced digitally. However, in many cases they are used to approximate a continuous signal. In many cases the sound produced is effectively continuous since the quantization levels are indiscernible.

Many computers have several other sensors and actuators within peripherals such as: scanners, printers, video cameras, graphics tablets, modems, etc. Instructors need to use their own judgement as to the relevance and correctness of answers related to such devices.

The purpose of this question (and others of this type) is not to elicit a perfect answer but to get the student to think about the issues involved.

**1.7** There are a number of valid ways of answering this question.

The actuator is the simplest to define. In a watch having hands it is the motor which drives the hands, while in a watch having a numeric display it is the display itself.

The sensor however could be defined in a number of ways. One could say that the sensor is a quartz crystal and that the physical quantity being measured is time. This would lead to the conclusion that the quantity being measured is continuous (if you accept that time is continuous!).

Alternatively, you could suggest that the sensor is a quartz crystal and that the physical quantity being measured is its own vibration (or oscillation) and is thus displacement. This would again lead to the conclusion that the physical quantity being measured is continuous.

Alternatively, it could be said that the sensor is a quartz crystal and that the physical quantity being measured is the *number* of oscillations. This would suggest that the quantity being measured is digital.

What *do* we mean by a digital watch?

**1.8** The effects of noise are determined by the relative magnitudes of the signal and the noise (that is, by the signal-to-noise ratio). Therefore, when the input signal of a system is small, a given amount of noise has a proportionally larger effect.

**1.9** Examples include:

*Hiss* from a tape player during quiet passages.

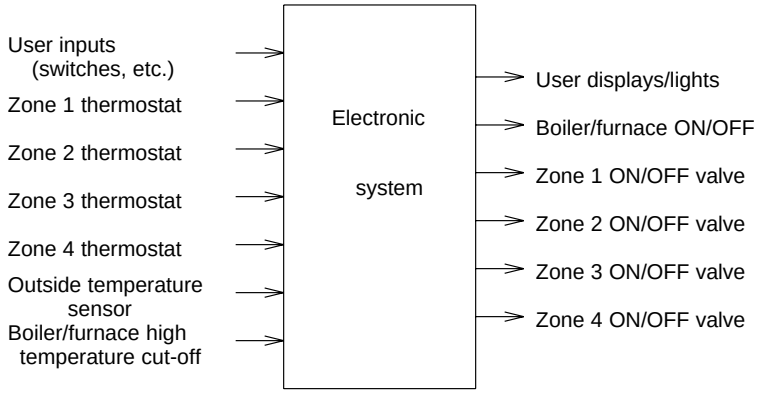
*Snow* on a television picture (worse with a weak signal).

Background *noise* on a telephone line.

**1.10** This is 'bottom-up' testing.

**1.11** The voltage across *R3* is 14 V.

**1.12** If we assume that the timing functions are performed by an internal clock, a suitable diagram for a system with four zones might be of the following form.



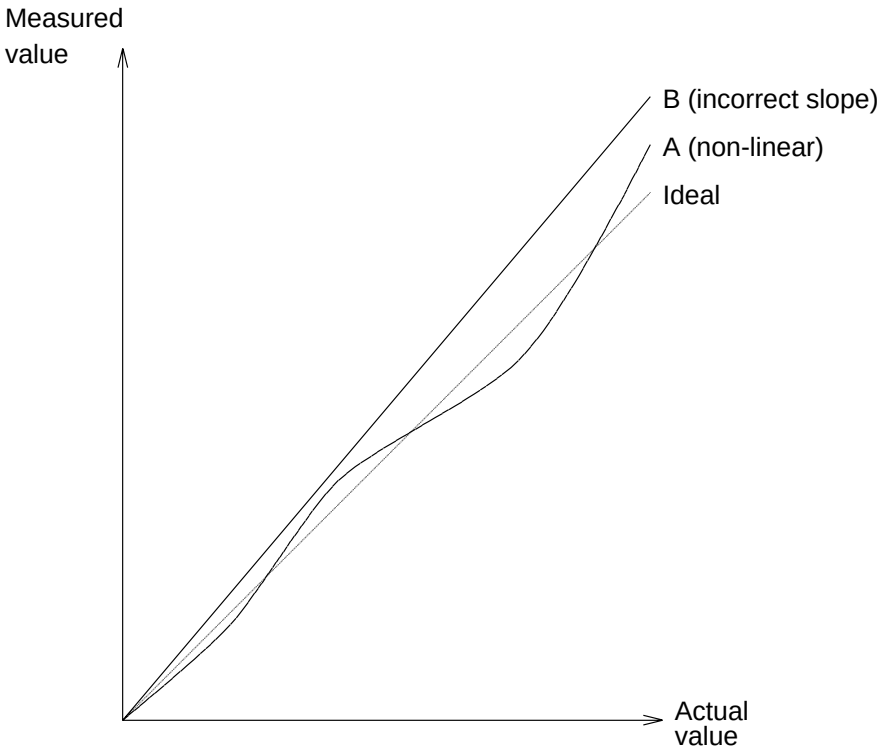
# Chapter 2
# MEASUREMENT, SENSORS AND ACTUATORS

**2.1** These terms are defined in Sections 2.1 and 2.2. The definitions, and further discussion of the terms, may be found using the index at the back of the book.

**2.2** Causes of random errors include: errors in placing or reading the tape measure; arithmetic errors in adding lengths if the tape is shorter than the room; etc.

Systematic errors include: incorrect calibration of the tape measure; stretching or shrinking of the measure; parallax errors in taking readings; etc.

**2.3** The following graph illustrates the concept of linearity.




The graph shows the characterstics of two measuring systems A and B, and compares these with those of an ideal system. If the scales of the axis are equal, an ideal transducer would produce a line at 45° as shown by the 'ideal' line in the graph. System A shows a greater accuracy that system B since it deviates less from the ideal line. However, B has better linearity since it deviates less from a straight line through the origin. In many cases B would be preferred to A, since it will often be possible to compensate for the incorrect slope by calibration.

**2.4** Traceability is the ability to trace the calibration route of a device back to the international standard, and hence to be able to predict its absolute accuracy.

**2.5** From Equation 2.2 we have that

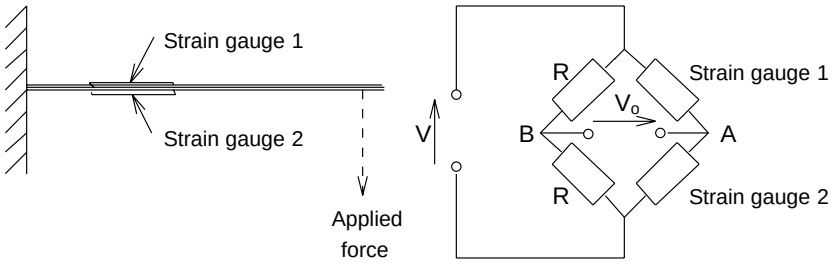
$$V_n\,(\text{r.m.s.}) = (4kTBR)^{\frac{1}{2}}.$$

Substituting the values for this examples gives

$$V_n\,(\text{r.m.s.}) = (4 \times 1.3805 \times 10^{-23} \times 300 \times 20 \times 10^3 \times 47 \times 10^3)^{\frac{1}{2}} \approx 3.9\ \mu\text{V}.$$

**2.6** See Section 2.3.3.

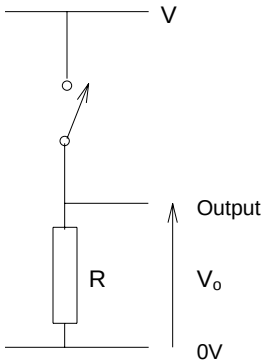
**2.7**




(a) (b)

An attractive method is to place the gauges above and below the beam as shown in (a) above and to connect them in a bridge circuit as shown in (b). A downward force on the end of the beam stretches gauge 1, increasing its resistance, and compresses gauge 2, decreasing its resistance. This decreases the voltage at the point *A* in the circuit with respect to the reference voltage at point *B*. This produces a negative output voltage $V_o$. An upward force on the beam would produce a positive output voltage.

**2.8** The following arrangement produces an output of $V$ if the switch is closed and 0V if the switch is open.




**2.9** The resistance at 100°C is given by

$$R = 100 + 100 \times 0.385\ \Omega = 138.5\ \Omega.$$

A current of 10 mA at 100°C would produce a voltage of

$$V = I \times R$$
$$= 10\text{ mA} \times 138.5\ \Omega = 1.385\text{ V}.$$

The power dissipated in the PRT is thus

$$P = I \times V$$
$$= 10\text{ mA} \times 1.385\text{ V}$$
$$= 13.85\text{ mW}.$$

This would therefore produce a rise in temperature of the sensor of

$$\Delta T = 0.2 \times 13.85 = 2.77°C.$$

In fact the calculation is slightly more complicated than that given above since this rise in temperature changes the resistance of the PRT which in turn changes the current and power dissipation. However this simple calculation is sufficient at this level.

**2.10** From the above it is clear that the temperature of the PRT is given by

$$R_T = 100 + 0.385 \times T\ \Omega.$$

Substituting this into the expression for the voltage across the potential divider gives

$$V_o = 10 \times \frac{R_T}{(100 + R_T)}$$
$$= 10 \times \frac{(100 + 0.385 \times T)}{100 + (100 + 0.385 \times T)}$$
$$= 10 \times \frac{100 + 0.385 \times T}{200 + 0.385 \times T}$$

$V_o$ is clearly not linearly related to T.

**2.11** The principal disadvantage of this method is its very high cost.

**2.12** Likely methods include ultrasonic and optical techniques.

With ultrasonic transducers it is possible to use simple time-of-flight measurements to measure distance although this gives a relatively low accuracy. For more precise measurements it is normal to use a phase sensitive detector at the receiver to compare the phase of the signal at the transmitter and at the receiver. This allows the distance to be resolved to much less than the wavelength of the signal being used.

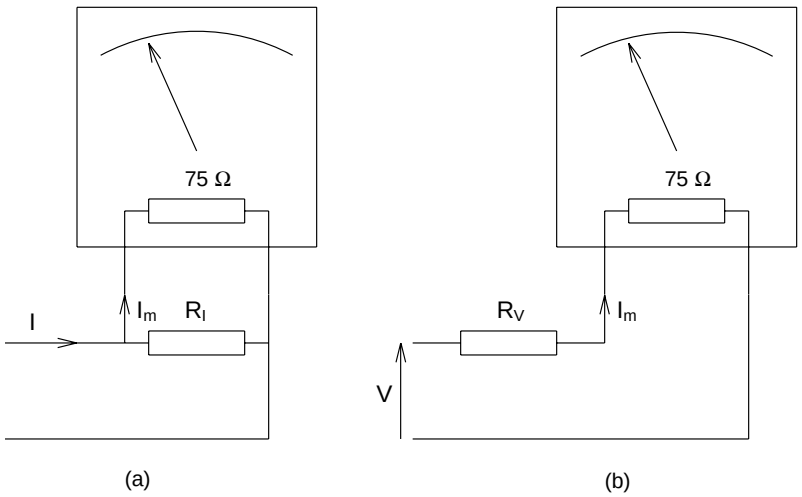
With optical systems time-of-flight measurements are often impractical except when measuring large distances and are not attractive for distances of up to 10 m (light takes only about 33 ns to travel this distance). It is common to modulate the optical signal and to again use phase measurements to resolve to a fraction of the wavelength of the modulation wavelength.

In both these examples the phase measurements give a relative position within a single wavelength rather than an absolute value. This problem may be overcome by the use of several modulation frequencies.

**2.13** Examples include:

| | |
|---|---|
| *humidity* | – used in greenhouse control |
| *altitude* | – used in autopilots |
| *mass* | – used in mass spectroscopy |
| *wavelength* | – used in colour matching |
| *density* | – used in injection molding |
| *gas concentration* | – used in mining |
| *magnetic flux* | – used in magnetic levitation |
| *resistivity* | – used in lie detectors |
| *taste sensors* | – used in the mouth |
| *radiation intensity* | – used in atomic reactors |

**2.14** The diagram below shows arrangements using the meter and a resistor.




In (a) the resistor is in a shunt configuration. Here a certain fraction of the current passes through the meter and the remainder goes through the resistor. This allows the meter to be used to measure larger currents since the current through the meter is

$$\frac{R_I}{R_I + 75\ \Omega}$$

times the current through the combination. Therefore, if the current through the meter is to be 1 mA when the total current is 1A, then

$$\frac{I_m}{I} = \frac{1\ \text{mA}}{1\ \text{A}} = \frac{R_I}{R_I + 75\ \Omega}$$

or rearranging

$$R_I = 75\ \Omega \frac{1\ \text{mA}}{1\ \text{A} - 1\ \text{mA}}$$

$$\approx 75\ \text{m}\Omega.$$

In arrangement (b) the additional resistor is placed in series with the meter such that the same current flows through the resistor and the meter. If the external resistor has a value of $R_V$, then the current flowing through the combination will be given by

$$I_m = \frac{V}{R_V + 75\ \Omega}$$

By choosing a suitable value of resistor the meter may be converted into a voltmeter with an appropriate range. To produce a full scale deflection for a voltage of 1 V, requires $R_V$ to have a value given by the expression

$$1\ \text{mA} = \frac{1\ \text{V}}{R_V + 75\ \Omega}$$

and thus

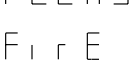
$$R_V = \frac{1\ \text{V}}{1\ \text{mA}} - 75\ \Omega$$

$$= 1\ \text{k}\Omega - 75\ \Omega = 925\ \Omega.$$

**2.15** Simulation should easilly verify the results of the above calculations.

**2.16** A stepper motor is the obvious choice. This would normally be driven from a crystal oscillator via a frequency divider. The pulse rate is reduced to one pulse per second and the motor is geared so that 60 pulses of the motor produces a movement of the second hand of 360°.

**2.17** A number of letters may be represented to a varying degree of acceptability. Examples are shown below.

| | Letter<br>A B C D E F G H I J K L M N O P Q R S T U V W X Y Z |
|---|---|
| Upper case |  |
| Lower case |  |
| Examples |  - Start<br>  - Stop<br>  - Please<br>  - Fire<br>  - Push<br>  - Pull |

# Chapter 3
# AMPLIFICATION

**3.1** Force is being amplified. The force applied to the brake drum or disc is greater than that applied at the pedal.

Distance is being attenuated. The distance travelled by the pedal is greater than that travelled by the brake drum or disc.

In a power assisted automotive braking system the source of power is the engine.

**3.2** In some cases numerous examples are possible. In others it is quite difficult to find examples other than those in the text.

Levers and pulleys are the obvious passive mechanical amplifiers and both are mentioned in the text. Other examples are usually modified versions of these, for example a lead screw (force) or a gear box (force or displacement depending on the ratio). Active examples include a slipping clutch arrangement (where the force applied to the clutch plate is amplified to produce a larger force on the driven shaft).

Passive hydraulic amplifiers include a hydraulic jack (force). Active examples include a hydraulic master/slave ram (force, power from whatever is activating the hydraulic pump).

Passive pneumatic amplifiers include a cycle pump (pressure). Active examples include a pneumatic master/slave ram (force, power from whatever is activating the pneumatic pump).

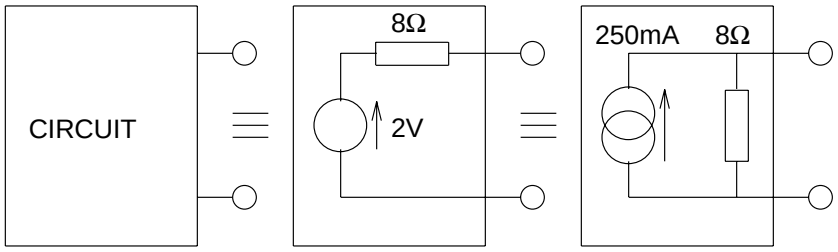
The most common examples of passive electrical amplifiers are transformers, which are mentioned in the text. Most other examples are a bit contrived – you must use your own judgement. Many examples of active electrical amplifiers are given in the text, examples not given include a photomultiplier tube (current, power comes from the high voltage supply).

Passive examples of physiological amplifiers could cover a range of mechanical, chemical and electrical phenomena. Examples include the lens in the eye (image size) and the amplification of movement caused by the lever action of the joints of the arm and leg (displacement). Active examples include the action of a synapse associated with the nerve cells (electrical energy, power comes from the stored chemical energy in the body).

**3.3** The values for the equivalent circuits can be calculated in a number of ways. In this example perhaps the easiest method is to use Thévenin equivalent circuits. First we calculate the equivalent circuit for the voltage source and R1 and R4. This is equivalent to a voltage source of 6 V in series with a resistance of 3 Ω. If we now add the effects of R2 and R5 we have a circuit which is equivalent to a voltage source of 2 V in series with a resistance of 2 Ω. Combining this with the effects of R3 gives an equivalent circuit for the complete circuit. From this the short circuit current can be

determined and hence the Norton equivalent circuit deduced.

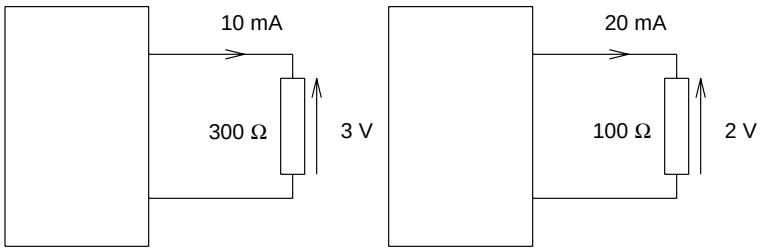
Therefore the equivalent circuits are



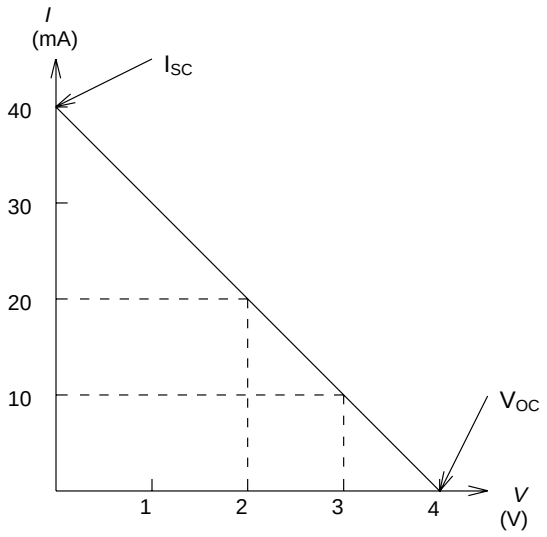

Thévenin equivalent circuit

Norton equivalent circuit

**3.4** This problem can be solved analytically or graphically as described in the text, the latter method is shown here.




When the external resistance is 300 Ω the output voltage is 3 V and hence the output current is 10 mA. When the external resistance is 100 Ω the output voltage is 2 V and hence the output current is 20 mA. Plotting $V_o$ against $I_o$ gives

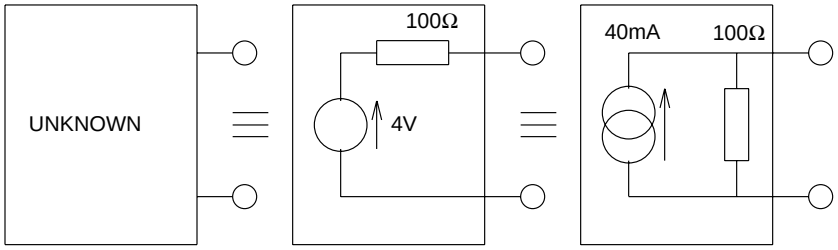


and thus the internal resistance $R$ is given by

$$R = \frac{V_{OC}}{I_{SC}}$$

$$= \frac{4\text{ V}}{40\text{ mA}} = 100\ \Omega.$$

Therefore the equivalent circuits are




Thévenin equivalent circuit

Norton equivalent circuit

**3.5** By Ohm's law the equivalent resistance of the circuit is 15 Ω.

**3.6** The output voltage may be calculated as in Example 3.1.

$$V_i = \frac{R_i}{R_s + R_i}\ V_s$$

$$= \frac{10\text{ k}\Omega}{200\ \Omega + 10\text{ k}\Omega}\ 1\text{ V r.m.s.}$$

$$V_o = A_v\ V_i \frac{R_L}{R_o + R_L}$$

$$= 20\ V_i \frac{1\text{ k}\Omega}{75\ \Omega + 1\text{ k}\Omega}\text{ V r.m.s.}$$

$$= 20\ \frac{10\text{ k}\Omega}{200\ \Omega + 10\text{ k}\Omega}\ 1\ \frac{1\text{ k}\Omega}{75\ \Omega + 1\text{ k}\Omega}\text{ V r.m.s.}$$

$$= 18.2\text{ V r.m.s.}$$

**3.7** Again, the output voltage may be calculated as in Example 3.1. If the sensor produces an output of 10 mV/cm, for an input of 1 m the output will be 1 V. Therefore

$$V_i = \frac{R_i}{R_s + R_i} V_s$$

$$= \frac{10\ \text{k}\Omega}{200\ \Omega + 10\ \text{k}\Omega}\ 1\ \text{V}$$

$$V_o = A_v\ V_i \frac{R_L}{R_o + R_L}$$

$$= 15\ V_i \frac{1\ \text{k}\Omega}{75\ \Omega + 1\ \text{k}\Omega}\ \text{V}$$

$$= 15\ \frac{10\ \text{k}\Omega}{200\ \Omega + 10\ \text{k}\Omega}\ 1\ \frac{1\ \text{k}\Omega}{75\ \Omega + 1\ \text{k}\Omega}\ \text{V}$$

$$= 13.7\ \text{V}$$

**3.8** a) A power gain of 10 is a gain of $10 \log_{10} 10 = 10$ dB.

b) A voltage gain of 1 is a gain of $20 \log_{10} 1 = 0$ dB.

c) A power gain of 0.5 is a gain of $10 \log_{10} 0.5 = -3$ dB.

d) A voltage gain of 1,000,000 is a gain of $20 \log_{10} 1{,}000{,}000 = 120$ dB.

**3.9** a) The power gain of a circuit with a gain of 20 dB = 100.

b) The voltage gain of a circuit with a gain of 20 dB = 10.

c) The power gain of a circuit with a gain of -15 dB = 0.032.

d) The voltage gain of a circuit with a gain of -15 dB = 0.18.

**3.10** a) An octave above 10 Hz is 20 Hz.

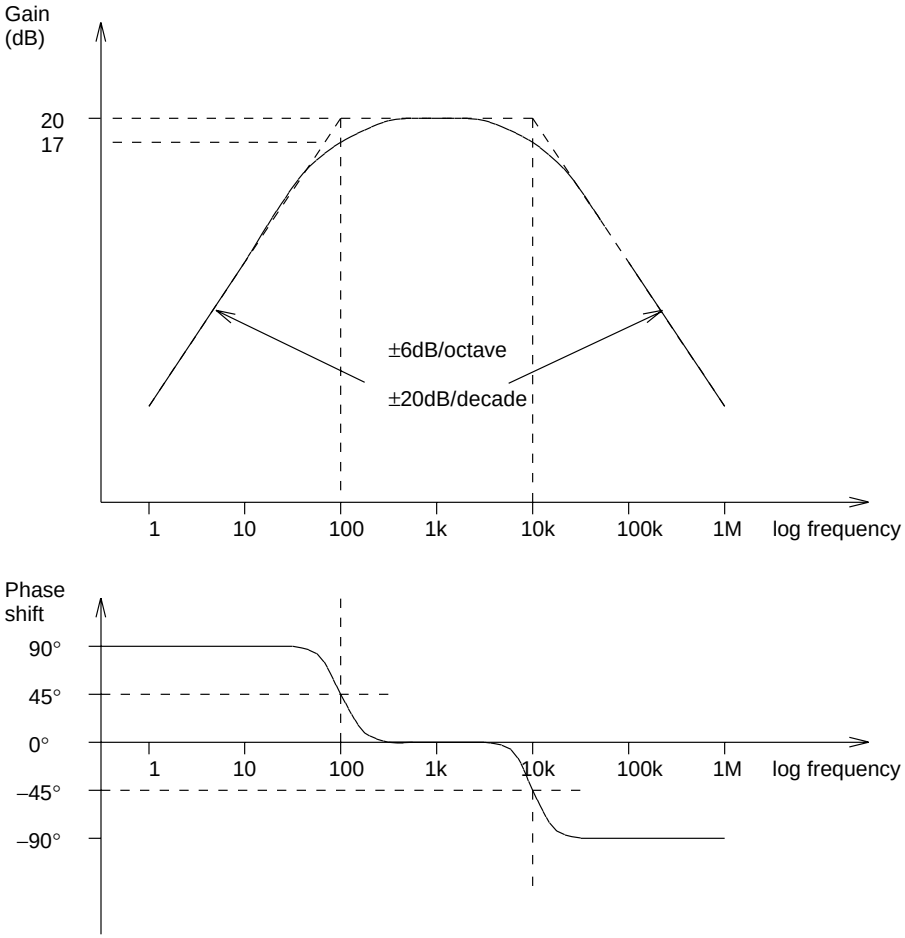
b) Three octaves above 1 Hz is 8 Hz.

c) Two octaves below 1 kHz is 250 Hz.

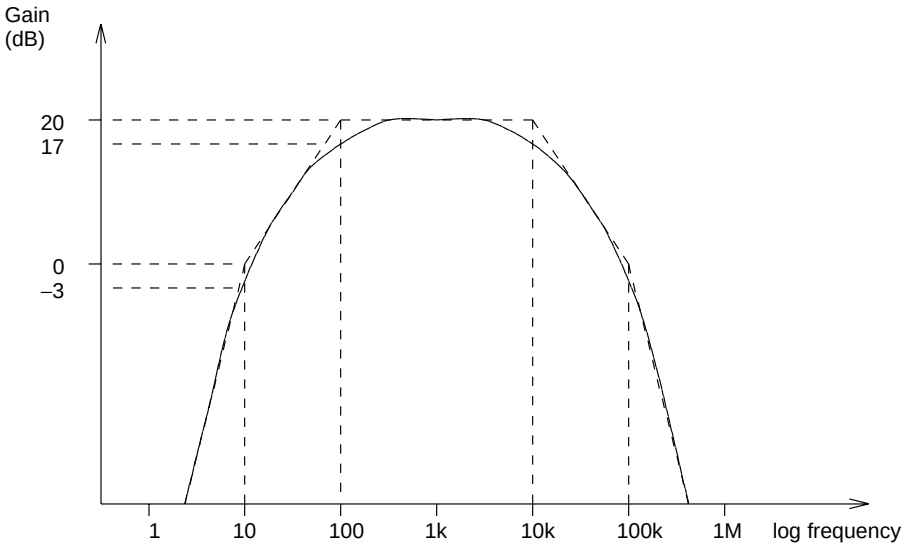
d) A decade above 100 Hz is 1 kHz.

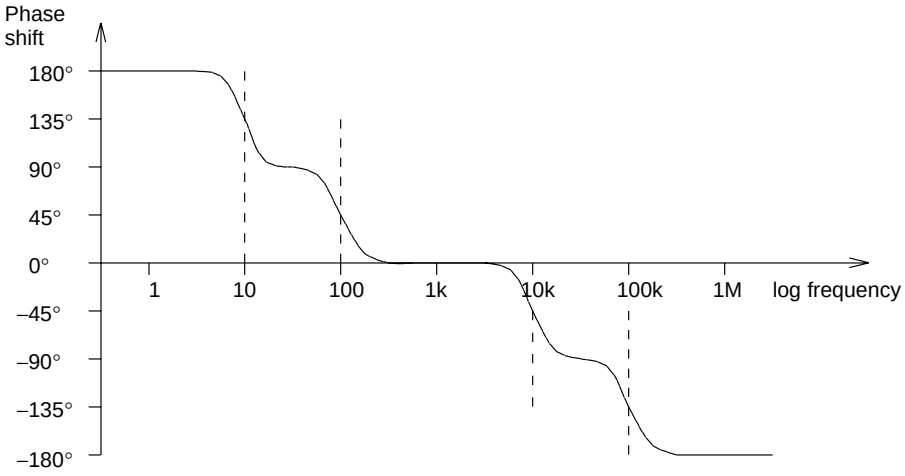
e) Two decades below 10 kHz is 100 Hz.

**3.11** The gain and phase responses are as follows



**3.12** The gain and phase responses are as follows




**3.13** From Equation 3.8 of the text

$$\text{Voltage gain } (A_v) = \frac{A'}{1 + \dfrac{\omega_L}{\mathrm{j}\omega}} = \frac{A'}{1 - \mathrm{j}\dfrac{\omega_L}{\omega}}$$

where $A' = R/(R + R_s)$ and $\omega_L = \dfrac{1}{C(R + R_s)} = \dfrac{1}{\mathrm{T}_L}$.

The cut off frequency $\omega_L$ is thus given by

$$\omega_L = \frac{1}{C(R + R_s)}$$

$$= \frac{1}{100\times10^{-9}(10\times10^3 + 1\times10^3)}$$

$$= 909 \text{ rads/s}$$

$$\approx 145 \text{ Hz.}$$

This is a lower cut-off frequency.

**3.14** If using PSpice, a suitable arrangement would use a variable voltage source (VSRC) with an AC magnitude of 1 V, and a DC magnitude of zero. Set up an AC sweep from 10 Hz to 10 kHz in decades, with 101 Pts/decade. Using Probe use the cursor to measure the frequency at which the gain falls to 0.707 of its high frequency value. This should be at about 145 Hz.

**3.15** From Equation 2.2 of the text we have

$$V_n\,(\text{r.m.s.}) = (4kTBR)^{\frac{1}{2}}.$$

where $k$ is Boltzmann's constant ($k \approx 1.3805 \times 10^{-23}$ J/K).
Substituting values for T, B and R gives

$$V_n\,(\text{r.m.s.}) = 1.2\ \mu\text{V}.$$

Therefore the signal to noise ratio is given by

$$\text{S/N ratio} = 20 \log_{10} \left(\frac{V_s}{V_n}\right) \text{dB}$$

$$= 20 \log_{10} \left(\frac{1\times10^{-3}}{1.2\times10^{-6}}\right) \text{dB}$$

$$\approx 58 \text{ dB}.$$

# Chapter 4
# FEEDBACK

**4.1** There are numerous examples of open-loop and closed-loop systems which could be called electronic systems. However, here we are mainly concerned with the parts which control the system rather than the other components. If this is accepted then electrical or other systems are easier to understand at this level. So for example a conventional electrical hand drill uses open-loop speed control (and thus the speed varies with the load) and an electronically controlled hand drill uses closed-loop control (and the speed is consequently more stable).

A steam engine can be controlled by simply varying the amount of steam applied to the piston. This is open-loop control and the speed will vary considerably with the load put on the engine. The use of a centrifugal governor, as in Section 4.2, forms a closed-loop system and produces a more consistent speed.

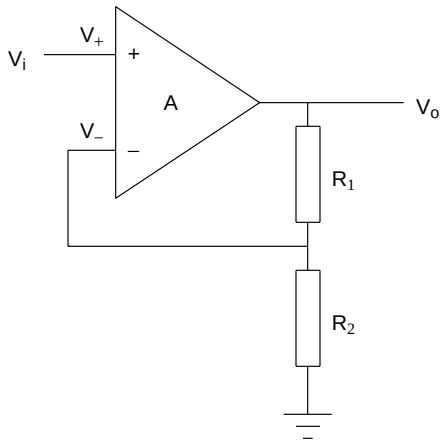
Hydraulic rams may be open-loop (when they apply a force related to the hydraulic pressure) or closed-loop (when the output position is used to vary the pressure to produce position control).

Pneumatic rams may also be used in open-loop or closed-loop systems.

Almost all biological systems are closed-loop. Examples include the maintenance of body temperature, sugar levels and many others. Most open-loop biological systems are rather contrived but can be found. An example might be the positioning of a part of the body with the eyes closed. Here the control of the individual limbs is closed-loop (using length sensors in the muscles) but the overall system is open-loop since it relies on a known relationship between the position of the joints and the resultant limb position, rather than on a measure of the final position. The fact that most biological processes are closed-loop says a great deal about their relative advantages.

**4.2** This diagram is given as Figure 4.3 in the text and the expression derived in Section 4.3 as Equation 4.1.

**4.3** The diagram below shows a suitable circuit.




From Example 4.2 we know that the overall gain $G$ is given by

$$G = \frac{V_o}{V_i} = \frac{R_1 + R_2}{R_2}$$

Based on the discussion of resistor values in Section 4.5, we might choose $R_1$ to be 100 kΩ and $R_2$ to be 1 kΩ. This gives a gain of approximately 100 (choosing a value of 99 kΩ for $R_1$ would be pointless unless very high tolerance resistors were to be used).

From Example 4.12 we know that the input resistance of this arrangement is approximately that of the op-amp (about 2 MΩ for a 741) multiplied by $1 + AB$. For a 741 $A$ is about $2\times10^5$ and $B$ is the feedback fraction which is approximately 0.01 (since the gain is $1/B$). Hence $1 + AB$ is approximately 2000 and the input resistance is about 4 GΩ (4000 MΩ).

From Example 4.12 we know that the negative feedback reduces the output resistance of the op-amp by a factor of $1 + AB$. The output resistance of a 741 is about 75 Ω and $1 + AB$ has a value of about 2000 (as above). Thus the output resistance has a value of about 75/2000 Ω or about 40 mΩ (there is little point in giving this figure to more than 1 significant figure because of the variability of the device).

**4.4** A suitable starting point for this exercise would be FILE 4H - the simulation file for computer simulation exercise 4.2. Choose component values to give a gain of 100 (for example resistors of 99 kΩ and 1 kΩ) and add an AC voltage source (VAC) as the input. Set the magnitude of the voltage source to 1 mV and configure the simulator to run Probe automatically at the end of simulation. Set up the simulation to perform an AC sweep from 1 Hz to 100 kHz with 11 points per decade.

Run the simulation and use Probe to plot the output voltage. From the graph you should see that the output magnitude at low frequencies is about 100 mV. Now modify the circuit by adding a 1 Ω resistor from the output to ground. Run the simulation once more and again note the output voltage. It will now have dropped to a magnitude of about 93 mV. By considering the output as a potential divider formed by the output resistance and the added load resistor it is now easy to compute the output resistor from the expression

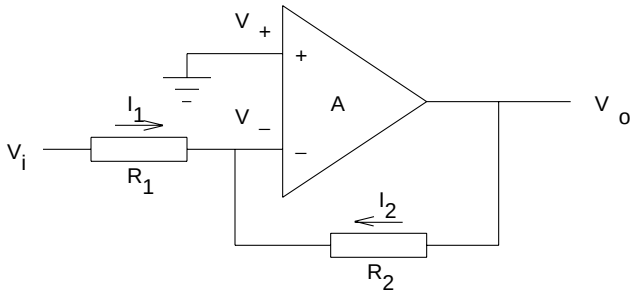
$$\frac{V_o}{V_{oc}} = -\frac{R_L}{R_o + R_L}.$$

Substituting the measured values should give a value for $R_o$ of about 75 mΩ.

The input resistance of the arrangement can be measured in a similar way. Remove the load resistor from the above circuit and add a 1 MΩ resistor ($R_s$) in series with the input. Run the simulation as above and use Probe to plot the voltage from the voltage source ($V_s$) and the voltage at the input of the op-amp ($V_i$). This will show that at low frequencies these two voltages are almost identical since the input impedance is very high compared with the 1 MΩ resistor. However, at higher frequencies the voltage at the input of the op-amp falls as the input impedance falls. This illustrates that the input impedance falls as the gain of the op-amp falls at high frequencies and the effects of the negative feedback fall off. To estimate the value of the input resistance plot the current through the input resistor. At low frequencies this will be of the order of a picoamp. Since the input voltage is about 1 mV at low frequencies this corresponds to an input resistance of about 1 GΩ. At higher frequencies the input current rises to about 1 nA which indicates an input resistance of about 1 MΩ. Here we see how *this form of negative feedback* increases the input resistance of the circuit to considerably greater than that of the op-amp itself. However, we also see that the improvement in input resistance is only gained at frequencies where the negative feedback is effective.

Note that the values produced by the simulation are not identical to those obtained using the typical figures given in the text. The PSpice models do not use the typical values given in the data sheet for the 741 op-amp. The differences between the two sets of values can be used to illustrate that both the values in the data sheets, and the parameters used by the simulation models, are *typical* values and that any real device is likely to differ from both. Where models rely on the characteristics of active components their results must be treated as estimates, not as exact values.

**4.5** A suitable circuit is shown below




From Example 4.3 we know the gain $G$ is given by

$$G = \frac{V_o}{V_i} = -\frac{R_2}{R_1}.$$

We might therefore choose $R_2$ to be 50 kΩ and $R_1$ to be 1 kΩ. Since 50 kΩ is not a standard value we might replace this with a standard value of 47 kΩ to give a gain of *approximately* 50, or make up the value using two high tolerance resistors (for example two 100 k resistors in parallel).

From Example 4.13 we know that the input resistance of this arrangement is approximately that of $R_1$ which in this case is 1 kΩ.

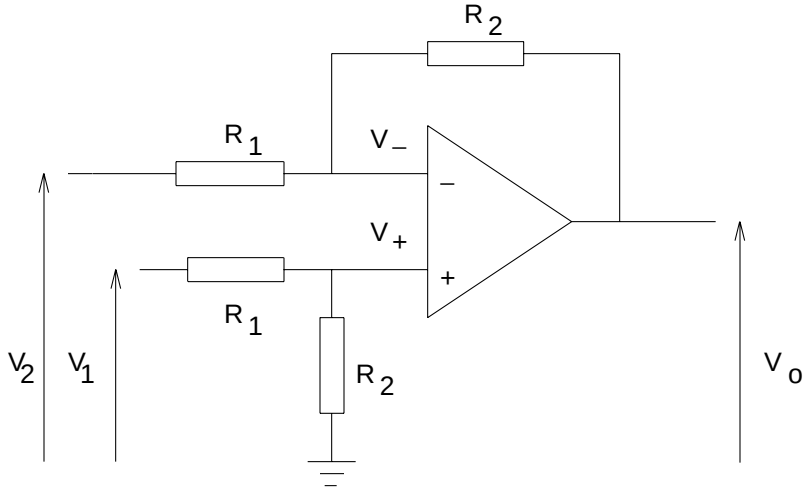
As in the last exercise the negative feedback reduces the output resistance of the op-amp by a factor of $1 + AB$. Here $B$ has a value of 1/50 or 0.02. The output resistance of a 741 is about 75 Ω and $1 + AB$ has a value of about 4000. Thus the output resistance has a value of about 75/4000 Ω or about 20 mΩ.

**4.6** A suitable starting point for this exercise would be FILE 4J for computer simulation exercise 4.3. The circuit should be modified to produce a gain of -50 and then similar techniques to those described for Exercise 4.4 above may be used.

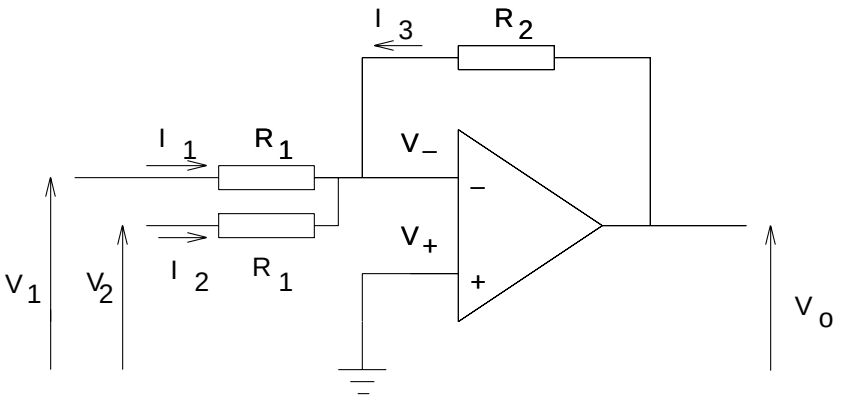
The measured value for the output resistance should be about 40 mΩ. This value is lower than that obtained for the non-inverting amplifier of Example 4.4 simply because the gain of the circuit is lower and therefore (1 + AB) is higher, giving a greater improvement in output resistance. If the magnitude of the gain is changed to 100 (as in Example 4.4) a higher value of output resistance is obtained - similar to that in the earlier exercise. As discussed in Example 4.4 above, the value obtained for the output impedance is slightly different from that predicted by the calculations in the last exercise.

When measuring input resistance remember that we are looking at the input resistance of the complete circuit, not that of the op-amp itself. We need to add a source resistor in series with the input resistor of the amplifier and measure the current through this resistance and the voltage at the input of the amplifier (or the ratio of the voltage across this resistor to the input voltage). A suitable value for the added resistor might be 1 kΩ. At low frequencies the measured value of the input resistance should be equal to the value of the input resistor in the circuit (not the added source resistor). Unlike the non-inverting amplifier, the input resistance of this circuit *increases* at higher frequencies as the feedback falls off.

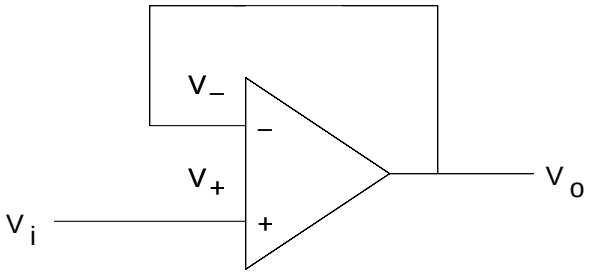
**4.7** A suitable circuit is as shown below with $R_1$ = 10 kΩ and $R_2$ = 100 kΩ.



**4.8** A suitable circuit would be as shown below with $R_1 = R_2 = 100\ \text{k}\Omega$.




**4.9**




The circuit is a special case of the non-inverting amplifier of Example 4.2 with $R_1$ equal to zero and $R_2$ equal to infinity. The overall gain $G$ is given by

$$G = \frac{R_1 + R_2}{R_2}$$

This may be rearranged to give

$$G = \frac{R_1}{R_2} + 1$$

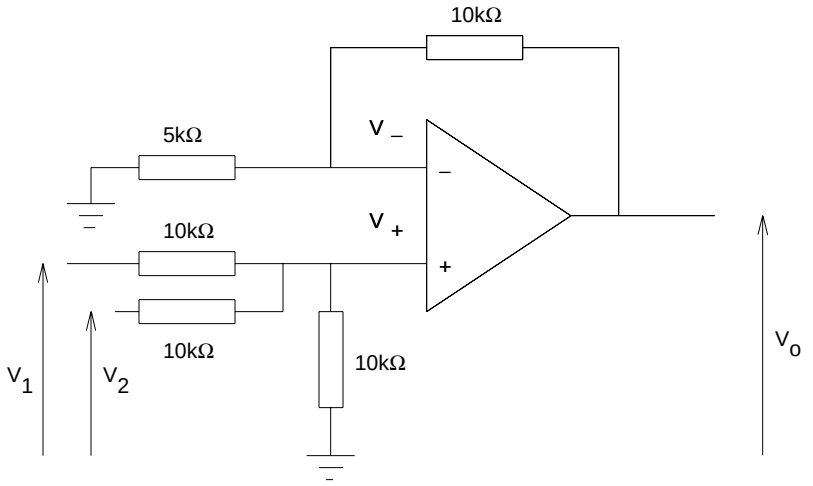
If we substitute appropriate values for $R_1$ and $R_2$ we get

$$G = \frac{0}{\infty} + 1 = 1$$

We thus have a unity gain amplifier.

Following the analysis given above for Exercise 4.3 we see that the input resistance of the circuit is approximately that of the op-amp multiplied by $1 + AB$. Here $B$ is unity and thus $1 + AB \approx A \approx 2\times10^5$. The input resistance is thus about 2 M$\Omega$ $\times$ $2\times10^5$ which is about $4\times10^{11}$ $\Omega$. The output resistance is about 75 $\Omega/A$ which is about 400 $\mu\Omega$. The circuit thus gives a very high input resistance, a very low output resistance and approximately unity gain. It is used as a unity gain buffer.

**4.10**




Since negligible current flows into the inputs of the op-amp, the voltages on the two inputs are determined simply by the external voltages and resistors.

Thus

$$V_- = V_o \frac{5\ \text{k}\Omega}{5\ \text{k}\Omega + 10\ \text{k}\Omega} = V_o \times \frac{1}{3}$$

and by superposition

$$V_+ = V_1 \frac{10\ \text{k}\Omega // 10\ \text{k}\Omega}{10\ \text{k}\Omega + 10\ \text{k}\Omega // 10\ \text{k}\Omega} + V_2 \frac{10\ \text{k}\Omega // 10\ \text{k}\Omega}{10\ \text{k}\Omega + 10\ \text{k}\Omega // 10\ \text{k}\Omega}$$

$$= (V_1 + V_2) \frac{5\ \text{k}\Omega}{10\ \text{k}\Omega + 5\ \text{k}\ \Omega} = (V_1 + V_2) \times \frac{1}{3}$$

The negative feedback forces $V_-$ to equal $V_+$ and therefore

$$V_o \times \frac{1}{3} = (V_1 + V_2) \times \frac{1}{3}$$

and thus

$$V_o = V_1 + V_2$$

**4.11** The use of negative feedback reduces the distortion by a factor of $1 + AB$. The reduction in distortion required is 15, so

$$1 + AB = 15$$

Since $A$ =1000, it follows that

$$1 + 1000B = 15$$

and thus, the feedback gain is

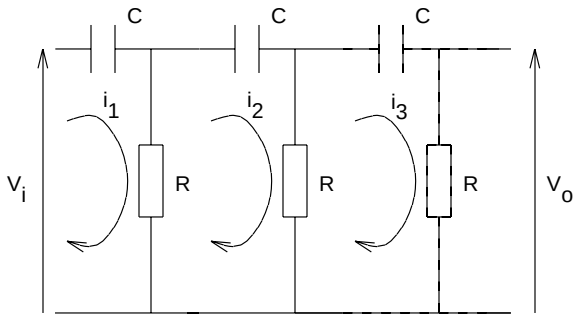
$$B = 0.014$$

A reduction in distortion by a factor of 15 is achieved along with a reduction in gain of the same amount. Therefore the input must be increased by a factor of 15 to maintain the output level at its original value.

**4.12** This topic is covered in Section 4.6.6 of the text in the sub-section headed ‘Gain and Phase Margins’.

**4.13** This topic is discussed in Section 4.6.6 of the text in the sub-section headed ‘Nyquist diagrams’. The significance of the point (−1,0) is that a line drawn from this point to a point on the locus of $P$ represents the term $1 + AB$. If the magnitude of this line is always greater than 1, the magnitude of the term $1 + AB$ is always greater than 1, and the circuit is stable. If a unit circle is drawn about this point the stability of the circuit may be readily seen. If the locus of P is outside the circle the circuit is stable; if the locus of P enters the circle the circuit is unstable, and if the locus of P passes through the point (−1,0) this represents a point where the gain is infinite and oscillation will occur.

**4.14**




For each of the circuit loops we may deduce a circuit equation.

$$v_i = i_1(R + \frac{1}{j\omega C}) - i_2R \tag{1}$$

$$0 = i_2(2R + \frac{1}{j\omega C}) - i_1R - i_3R \tag{2}$$

$$0 = i_3(2R + \frac{1}{j\omega C}) - i_2R \tag{3}$$

$$v_o = i_3R \tag{4}$$

From these equations we may progressively eliminate $i_3$ to $i_1$ to leave an expression for $v_i$ in terms of $v_o$.

From (4)

$$i_3 = \frac{v_o}{R}$$

Substituting for $i_3$ in (3) gives

$$i_2 = \frac{v_o}{R^2}(2R + \frac{1}{j\omega C})$$

Substituting for $i_2$ and $i_3$ in (2) gives

$$i_1 = \frac{v_o}{R^3}(2R + \frac{1}{j\omega C})^2 - \frac{v_o}{R}$$

and substituting for $i_1$ and $i_2$ in (1) gives

$$v_i = (\frac{v_o}{R^3}(2R + \frac{1}{j\omega C})^2 - \frac{v_o}{R})(R + \frac{1}{j\omega C}) - \frac{v_o}{R}(2R + \frac{1}{j\omega C})$$

This may be expanded and simplified to give

$$v_i = v_o\left(1 + \frac{6}{j\,\omega CR} + \frac{5}{(j\,\omega CR)^2} + \frac{1}{(j\,\omega CR)^3}\right)$$

which may be rearranged to give the required expression.

$$\frac{v_o}{v_i} = \frac{1}{1 - \frac{5}{(\omega CR)^2} - j\left(\frac{6}{\omega CR} - \frac{1}{(\omega CR)^3}\right)}$$

It should be noted that phase-shift oscillators may also be formed using a low-pass filter arrangement by simply interchanging the capacitors and resistors in the above circuit. This produces an expression for the voltage ratio of the form

$$\frac{v_o}{v_i} = \frac{1}{1 - 5(\omega CR)^2 + j\,(6\omega CR - (\omega CR)^3)}$$

and in this case the frequency of oscillation is given by

$$f = \frac{\sqrt{6}}{2\pi CR}.$$

**4.15** From Section 4.7.1 of the text we have

$$f = \frac{1}{2\pi CR\sqrt{6}}.$$

therefore

$$f = \frac{1}{2\pi\ 1\times10^{-6}\ 1\times10^{3}\sqrt{6}} = 65 \text{ Hz}.$$

**4.16** A similar analysis to that given in Exercise 4.14 above produces the following expression for the gain of the network

$$\frac{v_o}{v_i} = \frac{1}{1 - \frac{15}{(\omega CR)^2} + \frac{1}{(\omega CR)^4} - j\left(\frac{10}{\omega CR} - \frac{7}{(\omega CR)^3}\right)}$$

The frequency of oscillation corresponds to the condition that the imaginary part of the expression is zero. That is when

$$\frac{10}{\omega CR} = \frac{7}{(\omega CR)^3}$$

which may be simplified to give

$$f = \frac{1}{2\pi CR\sqrt{\frac{10}{7}}}.$$

Substituting this value back into the above expression gives an expression for the gain of the network at this frequency. This is approximately 1/18.4. Thus the required gain of the forward path is 18.4.

**4.17** By inspection, and following an analysis similar to that given in Exercises 4.3 and 4.5 we have:

a) Gain = 215, input resistance ≈ $1\times10^9$ Ω and output resistance ≈ 80 mΩ.

b) Gain = –33, input resistance ≈ 10 kΩ and output resistance ≈ 10 mΩ.

c) Gain = 11, input resistance ≈ $2\times10^{10}$ Ω and output resistance ≈ 4 mΩ.

d) Gain = –67, input resistance ≈ 1.5 kΩ and output resistance ≈ 20 mΩ.

**4.18**

$$\frac{v_o}{v_i} = \frac{Z_2}{Z_1 + Z_2}$$

$$= \frac{\frac{1}{\frac{1}{R} + j\omega C}}{\frac{1}{\frac{1}{R} + j\omega C} + R + \frac{1}{j\omega C}}$$

$$= \frac{1}{1 + (R + \frac{1}{j\omega C})(\frac{1}{R} + j\omega C)}$$

$$= \frac{1}{1 + (1 + \frac{1}{j\omega CR} + j\omega CR + 1)}$$

$$= \frac{1}{3 + \frac{1}{j\omega CR} + j\omega CR}$$

$$= \frac{1}{3 - j(\frac{1 - \omega^2 C^2 R^2}{\omega CR})}$$

as required.

**4.19** From Section 4.7.1 see have that

$$\omega = \frac{1}{CR}$$

and hence

$$f = \frac{1}{2\pi CR}.$$

Substituting for the component values gives

$$f = \frac{1}{2\pi\ 1\times10^{-8}\ 1\times10^{5}} \approx 160 \text{ Hz}.$$

**4.20** A PTC thermister could be used in a manner similar to that described in the text except that it would be used in place of $R_2$ rather than $R_1$.

**4.21** An accuracy of 1 second in a month represents an accuracy of 1 part in 2 592 000 (assuming a 30 day month). This is an accuracy of about 0.00004%.

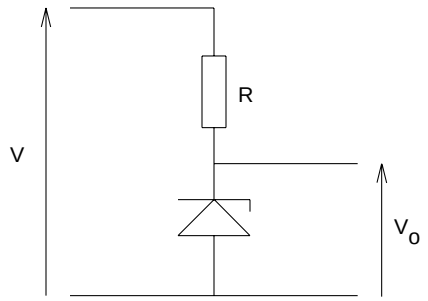
# Chapter 5
# SEMICONDUCTORS AND DIODES

**5.1** These topics are discussed in Sections 5.1 to 5.4 of the text. The index may be used to pin-point many of the terms.

**5.2** Commonly used materials include silicon, germanium and gallium arsenide. Silicon is currently the most widely used material for making electronic devices.

**5.3** The potential barrier formed at a *pn* junction cannot be measured externally because connecting external components to the device produces extra 'contacts' with contact potentials that cancel that of the junction.

**5.4** The following circuit is suitable.




$R$ should be as large as possible to minimize power dissipation. The maximum value is determined by the output current and the minimum input voltage.

The current taken by the load is given by

$$I_L = \frac{V_o}{R_L} = \frac{5.6\text{V}}{1\ \text{k}\Omega} = 5.6\ \text{mA}.$$

When the input voltage is at its minimum value (10.5 V), the voltage drop across $R$ must not be so great that the output voltage drops below $V_o$ (5.6 volts). Therefore,

$$V_{\text{min}} - I_L \times R > V_o$$

or substituting for actual values

$$10.5 - 5.6\times10^{-3}\, R > 5.6$$

Re-arranging gives

$$R < 875\ \Omega$$

We would therefore choose $R$ as the standard value 820 Ω.

The maximum power dissipated in the circuit is determined by the maximum input voltage. When $V$ equals 12.5 V, the voltage across $R$ is given by

$$V_R = 12.5 - 5.6 = 6.9\ \text{V}$$

and hence the power dissipated in $R$ is

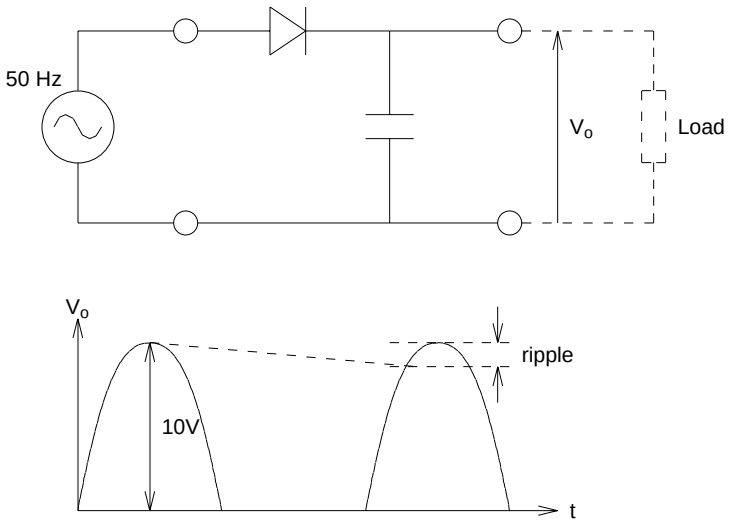
$$P_R = \frac{(V_R)^2}{R} = \frac{6.9^2}{820} \approx 60\ \text{mW}.$$

The power dissipated in the Zener diode is

$$P_Z = V_Z I_Z = V_Z (I_R - I_L) = 5.6 \times (8.4\times10^{-3} - 5.6\times10^{-3}) = 16\ \text{mW}.$$

**5.5** A similar analysis to that given for the last Exercise determines that $R$ must be less than 437 Ω. Therefore choose $R$ = 390 Ω. The maximum power dissipated in $R$ is then approximately 120 mW, and that in the Zener diode about 83 mW.

**5.6**




The voltage ($V$) across a capacitor is related to its charge ($q$) and its capacitance ($C$) by the expression

$$V = \frac{q}{C}$$

Differentiating this expression with respect to time gives

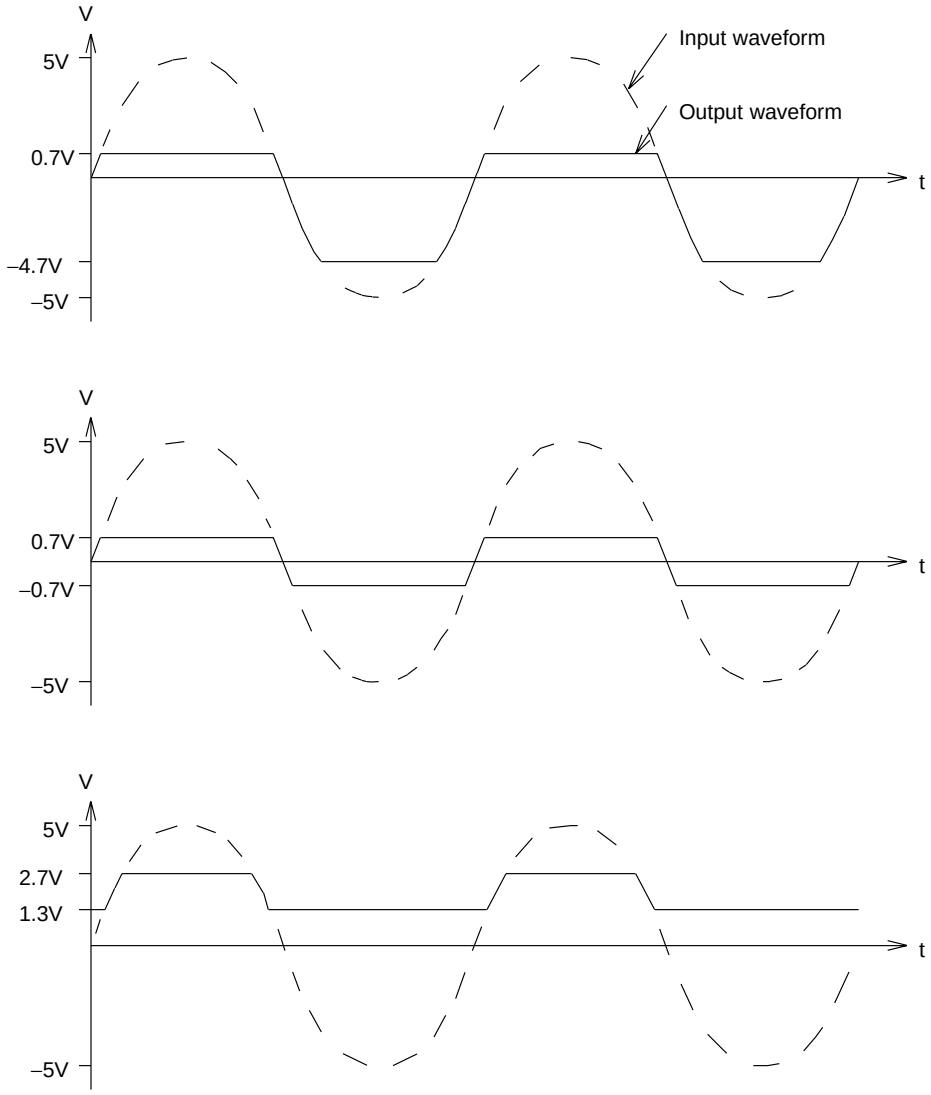
$$\frac{\mathrm{d}V}{\mathrm{d}t} = \frac{i}{C}$$

where $i$ is the current into, or out of, the capacitor. Thus the rate of change of voltage

with time is simply the ratio of the current to the capacitance. In our example the current $i$ is 200 mA and the capacitance $C$ is 10 mF. Thus the rate of change of voltage with time is 20 V/s. The time between peaks in the input waveform is equal to the period (20 ms) and during this time the voltage will drop by $20 \times 20 \times 10^{-3}$ which is about 0.4 V. Thus the peak ripple voltage is about 0.4 V.

**5.7** The ripple voltage would be approximately halved since the time for which the capacitor is discharged is halved.

**5.8** The output waveforms are as follows.



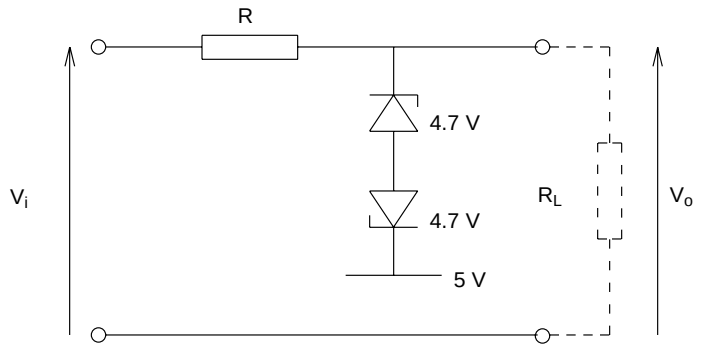

**5.9** If using PSpice the circuits can be easily simulated. A suitable arrangement might use a VSIN voltage source with Freq = 1k, VAMP = 5V, VOFF = 0, AC = 0 and DC = 0. The voltage source is simply connected in series with a resistor and the appropriate diode arrangement. A value of 1 kΩ is suitable for the resistor. $R_L$ is not essential for the operation of the circuits and may be omitted. If it is included it must be large compared with the series resistor to prevent its current from producing a large voltage

drop across the series resistor. The simulator should be configured to perform a transient analysis and set to print in steps of 20 ns with a final time of 2 ms. If Probe is set to run immediately after simulation then the output trace can be easily viewed by displaying the output voltage. This can be superimposed on the input trace if desired.

For circuit (a) a D1N750 zener diode can be used. This is one of the standard parts contained within the PSPice library. Circuits (b) and (c) can use any small signal diodes such as D1N914 devices. In (c) the 2 V supply can be produced using a VDC voltage source.

$R_L$ affects the circuit since its current flows through the series resistor and produces a voltage drop. If $R_L$ is not large compared with the series resistor then this voltage drop will distort the output waveforms.

**5.10** A suitable circuit is as follows.




**5.11** This exercise may be simulated as for Exercise 5.8(c) above. The diodes are replaced by two 4.7 V zener diodes (e.g. D1N750) in series and the voltage of the AC source is increased (perhaps to 15 V pk). The voltage of the DC source is also increased to 5 V.

# Chapter 6
# FIELD EFFECT TRANSISTORS

**6.1** Holes.

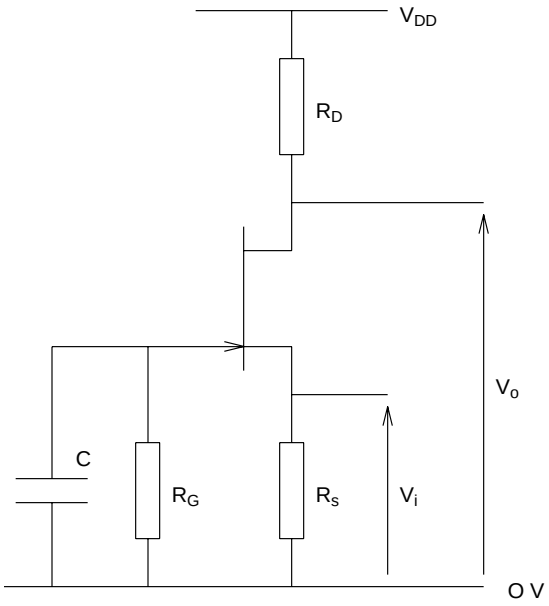
**6.2** To place the device within an appropriate region of its operating range.

**6.3** The polarity of a typical gate bias voltage would be:

| | |
|---|---|
| *n*-channel DE MOSFET | zero |
| *p*-channel JFET | positive |
| *p*-channel enhancement MOSFET | negative |
| *n*-channel JFET | negative |

**6.4** *C* is a coupling (or blocking) capacitor. Its function is to *couple* the input alternating signal to the amplifier while *blocking* any direct component which might otherwise upset the biasing arrangement of the amplifier. The presence of the capacitor will introduce a low-frequency break point which will reduce the gain of the amplifier at low frequencies as discussed in Section 3.7.1.

**6.5** The circuit below is an example of a common gate amplifier.




**6.6** The analysis shows that the gain of the resulting amplifier is approximately −8. The small signal input resistance is unchanged at 1 MΩ and the small signal output resistance is approximately 3.2 kΩ.

**6.7** From Equation 6.3 of the text we have

$$g_m = -2\frac{\sqrt{I_{DSS}}}{V_p} \times \sqrt{I_D}$$

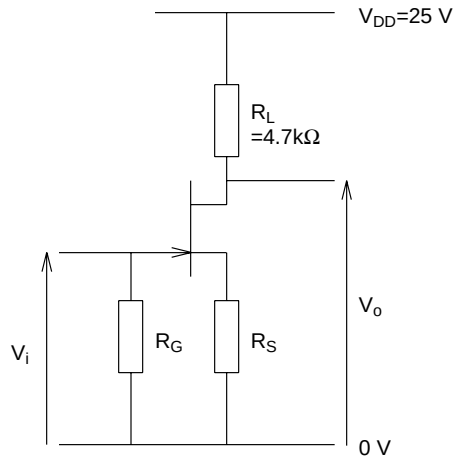
In this case $I_{DSS}$ is 6 mA and $V_p$ is −4 V. Substituting these values into the equations gives

$$g_m = 0.0387 \times \sqrt{I_D}$$

Thus the values of $g_m$ corresponding to drain currents of 1 mA, 2 mA and 4 mA, are 1.2 mS, 1.7 mS and 2.4 mS respectively.

**6.8** The JFET has $V_P$ = −4 V and $I_{DSS}$ = 6 mA. The amplifier is to be used with a supply voltage of 25 V and a load resistance of 4.7 kΩ, the amplifier is to have a quiescent output voltage of 15 V.

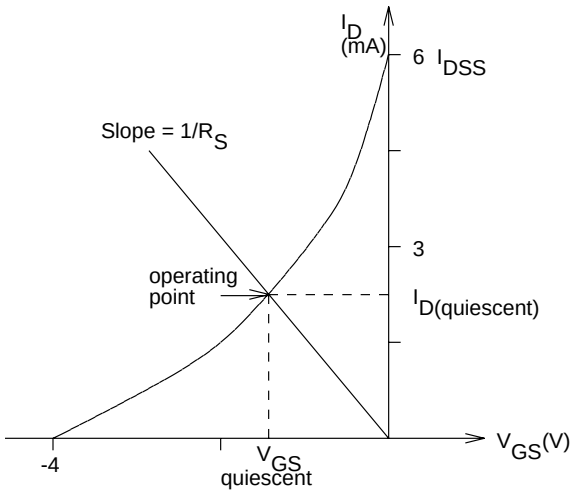
A suitable circuit is given below




From Equation 6.2 we know that

$$I_D = I_{DSS}(1 - \frac{V_{GS}}{V_p})^2$$

which, using the figures given for $V_P$ and $I_{DSS}$ may be plotted to give




The quiescent output voltage $V_{o\,(quiescent)}$ is given by

$$V_{o\,(quiescent)} = V_{DD} - V_L$$

where $V_L$ is the voltage drop across the load resistor $R_L$. Therefore the required value of $V_L$ is given by

$$V_L = V_{DD} - V_{o\,(quiescent)} = 25 - 15 = 10\ V,$$

and the required quiescent drain current $I_{D\,(quiescent)}$ is

$$I_{D\,(quiescent)} = \frac{V_L}{R_L} = \frac{10\text{V}}{4.7}\ \text{k}\Omega = 2.13\ \text{mA}.$$

From the transfer characteristic, this value of drain current corresponds to a gate to source voltage of −1.62 V. Since the gate is at ground potential this gate to source voltage must be obtained by a voltage drop across $R_S$ of +1.62 V. Thus the value of

$R_S$ is given by

$$R_S = \frac{V_{GS}}{I_D} = \frac{1.62\text{ V}}{2.13\text{ mA}} = 760\ \Omega.$$

The value of $R_G$ is not critical as it is simply required to bias the gate to zero volts. It would normally be chosen to give a high input resistance, but must not be so high that the voltage drop caused by the effects of the gate current (a few nanoamps) becomes significant. A value of 470 kΩ would be suitable.

**6.9** The circuits of Figures 6.30(a) and 6.31(a) are equivalent other than in respect of where the output is sensed. From the circuit is clear that the source current is related to the source voltage by the expression

$$i_s = \frac{v_s}{R_S}$$

and similarly

$$i_d = -\frac{v_d}{R_D}$$

Since the gate current is negligible it follows that the drain current is equal to the source current, and thus

$$\frac{v_s}{R_S} = -\frac{v_d}{R_D}$$

The analysis of Figure 6.31(a) shows that the small signal voltage on the source of the amplifier is effectively equal to the small signal input voltages, and thus $v_s = v_i$. In the circuit of Figure 6.30(a) the output is taken from the drain and thus $v_o = v_D$.

Substituting these into the above expression gives

$$\frac{v_i}{R_S} = -\frac{v_o}{R_D}$$

and rearranging gives

$$\frac{v_o}{v_i} = -\frac{R_D}{R_S}.$$

Thus the small signal voltage gain is equal to the ratio of the drain and source resistors. You might like to point out to students the similarity between this result and that obtained for equivalent bipolar circuits.

**6.10** The orientation of the diode and the polarity of $V_S$ are reversed.

**6.11** The operation of these circuits relies on the fact that when the input voltage is high (normally close to $V_{DD}$) the switching transistor is turned ON, but when the input voltage is low (close to 0 V) the switching transistor is turned OFF. The second of these conditions is only satisfied if the transistor used is an enhancement FET. A DE MOSFET would require the input voltage to be taken negative (for an *n*-channel device) in order for it to be turned OFF.

**6.12** Because of the symmetry of the circuit, if the circuit's output is taken as the difference between the two drain voltages ($V_4$ - $V_3$ in Figure 6.32) then the output for a common-mode signal will always be zero and the CMRR will appear to be infinite. In fact, although the circuit produces two complementary outputs, *each* output should represent the difference between the inputs. We therefore look at a single output and measure the difference between the output for a differential input and that for a common-mode input.

Start with the circuit of computer simulation exercise 6.3 as given in FILE 6C. Set the input magnitude to 50 mV peak at 1 kHz and use transient analysis to observe the behaviour of the system. Suitable setting for the analysis would be a step size of 30 us and a final time of 3 ms. Perform the analysis and use Probe to look at the output waveform on V4. Measure the peak to peak voltage of the output and divide this by the peak to peak voltage applied to the input (100 mV) to give the differential voltage gain. The gain will be about 3.4.

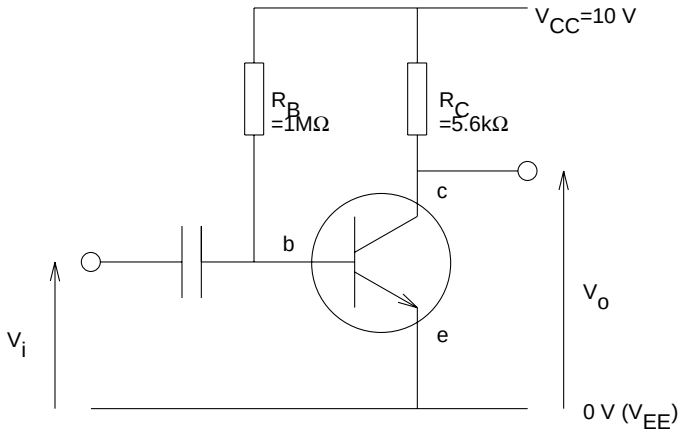
Next modify the circuit by removing the fixed voltage connected to V2 and connecting this input to V1 so that the same input is applied to both gates. Again measure the ratio of the peak to peak output voltage to the peak to peak input voltage. This is the common-mode gain which will be about 0.31.

The ratio of the differential voltage gain to the common-mode voltage gain gives the CMMR which will be about 3.4/0.31 = 11.

**6.13** Measuring the current in R sub S in the circuit of the last exercise will give a value of about 4.1 mA. A similar current can be achieved using a 2N3819 JFET and a 300 Ω resistor in a circuit as in Figure 6.35. The differential and common-mode gains may then be measured as in Exercise 6.12. This will produce values for the differential gain of about 3.5 and for the common-mode gain of about 0.004. This gives a value for the CMRR of about 3.5/0.004 = 880.

# Chapter 7
# BIPOLAR JUNCTION TRANSISTORS

**7.1**




The voltage across $R_B$ is equal to the supply voltage less the voltage across the base to emitter junction of the transistor (about 0.7 V). Thus the voltage across $R_B$ is about 9.3 V. Therefore the base current is given by

$$I_B = \frac{9.3}{R_B} = \frac{9.3}{1\ \text{M}\Omega} = 9.3\ \mu A$$

Therefore, the quiescent collector current is given by

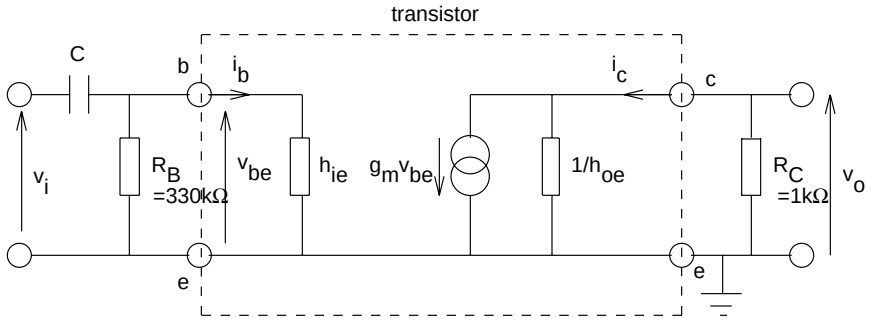
$$I_C = h_{FE} I_B = 100 \times 9.3 \times 10^{-6} = 930\ \mu A$$

and the quiescent output voltage is given by

$$V_C = V_{CC} - I_C R_C = 10 - 930 \times 10^{-6} \times 5.6 \times 10^3 \approx 4.8\ \text{V}.$$

**7.2** A similar analysis to that given above shows that the base current is again 9.3 μA. With a current gain of 200 the collector current would be about 1.9 mA. This would give a voltage drop across $R_C$ of 10.4 V which is greater than the supply voltage and is therefore impossible. This shows that the transistor is saturated (with a resultant drop in current gain). The output voltage will be equal to the saturation voltage of the transistor (about 0.1 – 0.2 V) and the circuit is not usable as a linear amplifier.

**7.3** The following equivalent circuit is appropriate.




**Bias conditions**

Before we can investigate the small signal behaviour of the circuit we need to look at its biasing conditions. By an analysis similar to that given in the answer to Exercise 7.1 above we see that the quiescent base current is 34 μA, the quiescent collector current is 6.0 mA and the quiescent output voltage is 6 V.

**Voltage gain**

In order to determine the behaviour of the circuit we need to establish the values of $g_m$ and $h_{ie}$. From Equation 7.5 of the text

$$g_m \approx 40I_E \approx 40I_C \approx 240 \text{ mS}$$

and

$$h_{ie} \approx \frac{h_{fe}}{40I_E} \approx \frac{175}{40\times 6.0\times 10^{-3}} \approx 730\ \Omega.$$

From Equation 7.12 of the text we have

$$\text{voltage gain} = \frac{v_o}{v_i} = -g_m \frac{R_C}{h_{oe}R_C + 1}.$$

and substituting for the component values gives

$$\text{voltage gain} = -240\times 10^{-3}\frac{1000}{15\times 10^{-6}\times 1000 + 1} \approx -236$$

If we consider that $1/h_{oe}$ is large compared with $R_C$ and assume that the voltage gain is equal to $g_m R_C$, this gives a value of −240. Given the inaccuracies in our calculations this is probably a reasonable approximation.

**Input resistance**

From the equivalent circuit it is clear that the small signal input resistance is simply $R_B // h_{ie}$. Since $R_B >> h_{ie}$ it is reasonable to say

$$r_i = R_B // h_{ie} \approx h_{ie} \approx 730\ \Omega.$$

**Output resistance**

The small signal output resistance is the resistance seen 'looking into' the output terminal of the circuit. Since the idealized current generator has an infinite internal resistance, the output resistance is simply the parallel combination of $R_C$ and $1/h_{oe}$. Thus

$$r_o = R_C // \frac{1}{h_{oe}} = 1000 // 66{,}667 \approx 985\ \Omega$$

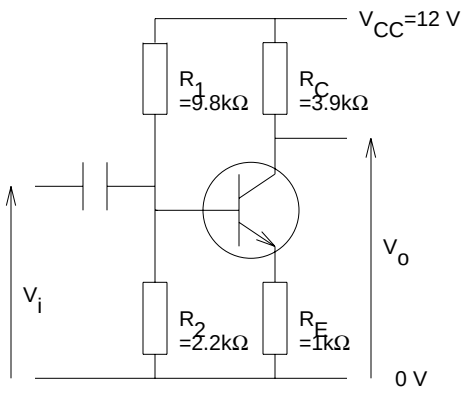
Again it is reasonable to use the approximation that $r_o \approx R_C$.

The voltage gain is related to the quiescent voltage across $R_C$ by the expression

$$\text{voltage gain} \approx -40 V_{RC} \approx -40 \times 6.0 = -240$$

**7.4** A similar analysis to that given in the last Exercise shows that in this case it is not appropriate to make the assumption that the gain is equal to $-g_m R_C$. Taking into account the effects of $h_{oe}$ gives a value for the gain of approximately -180. The input resistance is unchanged but the output resistance is reduced to about 750 Ω.

**7.5**




If we assume that the gain of the transistor is high so that the base current may be ignored, then the base to emitter voltage is determined simply by the supply voltage and the two base resistors. Thus

$$V_B = V_{CC} \frac{R_2}{R_1 + R_2} = 12 \times \frac{2.2 \times 10^3}{9.8 \times 10^3 + 2.2 \times 10^3} = 2.2\ \text{V}$$

Therefore, the emitter voltage is given by

$$V_E = V_B - V_{BE} = 2.2 - 0.7 = 1.5\ \text{V}$$

and the emitter current by

$$I_E = \frac{V_E}{R_E} = \frac{1.5}{1000} = 1.5\ \text{mA}.$$

If the base current is negligible then $I_C \approx I_E$, and therefore

$$I_C = I_E = 1.5\ \text{mA}$$

The quiescent output voltage is now simply given by

$$V_{o\,(quiescent)} = V_{CC} - I_C R_C = 12 - 1.5 \times 10^{-3} \times 3.9 \times 10^3 = 6.15\ \text{V}.$$

Since there is an approximately constant voltage drop across the base to emitter junction of the transistor, there is no small signal voltage drop across this junction. Thus the small signal voltage on the emitter is equal to the small signal input voltage

$$v_e \simeq v_b \simeq v_i$$

Now from Ohm's law

$$i_e = \frac{v_e}{R_E}$$

and since

$$i_c \simeq i_e$$

it follows that

$$v_o = -i_c R_C \simeq -i_e R_C = -\frac{v_e}{R_E} R_C$$

where the '–' sign reflects the fact that the output voltage goes down when the current increases. $V_{CC}$ does not appear within this expression because the supply rail has no small signal voltages on it (see Section 6.5.1).

Substituting for $v_e$ we have

$$v_o = -v_e \frac{R_C}{R_E} \simeq -v_i \frac{R_C}{R_E}$$

and therefore the voltage gain of the circuit is given by

$$\text{voltage gain} = \frac{v_o}{v_i} \simeq -\frac{R_C}{R_E}.$$

For the component values used this gives

$$\text{voltage gain} \simeq -\frac{3.9\ \text{k}\Omega}{1.0\ \text{k}\Omega} \simeq -3.9.$$

**7.6** From Equation 7.17 of the text we have

$$R_i = R_1 // R_2 // r_b$$

where

$$r_b \simeq h_{fe} R_E$$

which in this case means that

$$r_b \simeq h_{fe} \times 3.9\ \text{k}\Omega$$

Taking a reasonable value for $h_{fe}$ means that $r_b$ is likely to be much larger than $R_1$ and $R_2$ and therefore its effects may be ignored. If this assumption is made then

$$R_i \simeq R_1 // R_2 = 9.8\ \text{k}\Omega // 2.2\ \text{k}\Omega \simeq 1.8\ \text{k}\Omega.$$

From the discussion of Example 7.5 in the text we have that

$$r_o = R_C // \frac{1}{h_{oe}} \simeq R_C$$

Thus in this case

$$r_o \simeq R_C = 3.9\ \text{k}\Omega.$$

**7.7** From the discussion of Section 7.6.6 we see that the coupling capacitor produces a low-frequency cut-off at a frequency $f_{co}$ given by

$$f_{co} = \frac{1}{2\pi CR}$$

where $C$ is the value of the coupling capacitor and $R$ is the input resistance of the amplifier.

Substituting actual component values gives

$$f_{co} = \frac{1}{2\pi\ 10^{-6}\ 1.8\times10^{3}} \approx 88 \text{ Hz}.$$

**7.8** From Section 7.6.7 of the text it is clear that the bias conditions of the circuit are unaffected by the addition of a decoupling capacitor and thus the quiescent output voltage is as in Exercise 7.5 (6.15 V).

This section also gives expressions for the gain and input and output resistances. Thus, for mid-band frequencies,

$$\text{voltage gain} \approx -\frac{R_C}{r_e} \approx -R_C\, 40 I_E \approx -3.9\times10^{3}\ 40\ 1.5\times10^{-3} \approx -234$$

and

$$r_i = R_1 // R_2 // h_{ie}$$

The value of $h_{ie}$ depends on $h_{fe}$ which is not specified in this Exercise. If we take a typical value of 100, this gives

$$h_{ie} \approx \frac{h_{fe}}{40 I_E} = \frac{100}{40 \times 1.5\times10^{-3}} \approx 1.7 \text{ k}\Omega$$

and therefore

$$r_i = R_1 // R_2 // r_e = 9.8 \text{ k}\Omega // 2.2 \text{ k}\Omega // 1.7 \text{ k}\Omega \approx 870\ \Omega$$

At low frequencies the circuit would have a gain of approximately $-R_C/R_E \approx -3.9$. This gain would remain fairly constant from very low frequencies up to a frequency $f_1$ given by

$$f_1 = \frac{1}{2\pi C_E R_E} = \frac{1}{2\pi\ 10^{-6}\ 10^{3}} \approx 160 \text{ Hz}$$

as described in Section 7.6.7 of the text.

The value of the decoupling capacitor determines the frequency at which the gain falls from its mid-band gain, down to its low frequency gain (as shown in Figure 7.22 of the text). The cut-off frequency $f_{co}$ is given by

$$f_{co} = \frac{1}{2\pi C_E r_e}$$

where $r_e \approx 1/40 I_E \approx 17\ \Omega$.

When $C_E$ = 1μF this gives

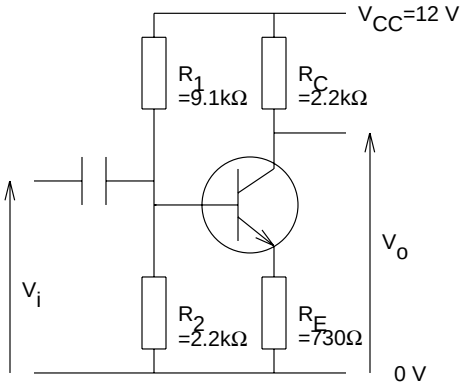
$$f_{co} = \frac{1}{2\pi\ 10^{-6}\ 17} \approx 9.4\ \text{kHz}$$

If the amplifier is to be used with signals down to about 100 Hz, we might choose the cut-off frequency to be perhaps 10 Hz. This would give a value for $C_E$ of

$$C_E = \frac{1}{2\pi f_{co}\, r_e} = \frac{1}{2\ \pi\ 10\ 17} \approx 940\ \mu F$$

and we would therefore choose a 1000 μF (1 mF) capacitor.

**7.9** The circuit below would be suitable, but is not a unique solution.




The value of 730 Ω for $R_E$ is not a standard value. If a precise value for the gain is required this value could be produced using a combination of resistors. Alternatively the nearest standard value could be used and a slightly different gain accepted. The values shown produce a theoretical gain of −3.01 and a quiescent output voltage of 7.07 V. Because of the tolerance of the components used there is little point in calculating values to any greater accuracy.

**7.10** Enter the circuit of the design (for example that given above) into PSpice using a suitable transistor (e.g. a Q2N2222) and add a VSIN voltage source. Suitable settings for the VSIN parameters might be VAMPL = 50mV, FREQ = 1k, VOFF = 0, AC = 0 and DC = 0. With a frequency of 1 kHz a suitable value for the capacitor is 10 uF. Add a viewpoint to the output to display the quiescent output voltage and set up the analysis to evaluate bias point details and to perform a transient analysis. Suitable values for the transient analysis would be a step size of 20us and a final time of 2 ms.

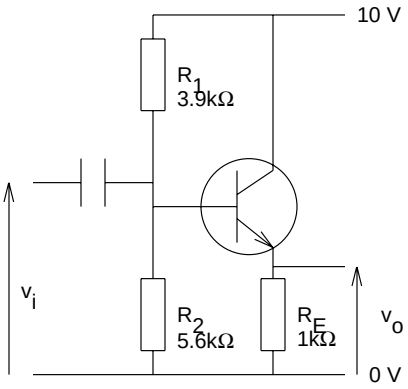
Run the analysis and look at the input and output voltages. This should show that the quiescent output voltage and the voltage gain are as predicted.

**7.11** The input resistance is approximately $R_1 // R_2$. For the circuit given above this is about 1.8 kΩ. For operation down to 50 Hz we might choose a low-frequency cut-off of about 5 Hz, and thus

$$C = \frac{1}{2\pi f_{co}\, r_i} = \frac{1}{2\pi\ 5\ 1.8\times 10^3} \approx 18\ \mu F$$

We would therefore probably choose a standard value of 22 μF.

**7.12**




The quiescent base voltage is given by

$$V_B = V_{CC}\frac{R_2}{R_1 + R_1} = 10\frac{5.6\times10^3}{3.9\times10^3 + 5.6\times10^3} \approx 5.9 \text{ V}$$

The quiescent output voltage is equal to the emitter voltage which is given by

$$V_{o\,(quiescent)} = V_E = V_B - V_{BE} = 5.9 - 0.7 = 5.2 \text{ V}.$$

The quiescent collector current is approximately equal to the emitter current which is given by the ratio of the emitter voltage to the emitter resistor. Thus

$$I_{C\,(quiescent)} = I_E = \frac{V_E}{R_E} = \frac{5.2 \text{ V}}{1 \text{ k}\Omega} = 5.2 \text{ mA}.$$

The small signal voltage gain is approximately 1 (see Section 7.6.8).

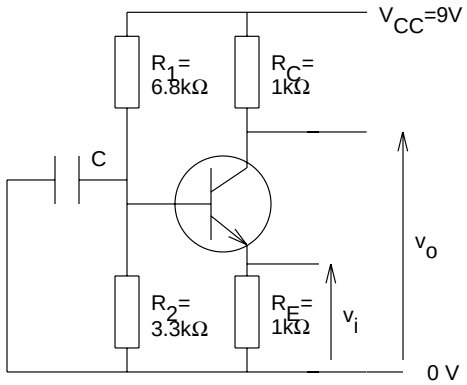
The input resistance is given by

$$r_i \approx R_1 // R_2 // r_b \approx R_1 // R_2 \approx 2.3 \text{ k}\Omega.$$

The output resistance is given by

$$r_{out} \approx r_e \approx \frac{1}{40I_E} \approx \frac{1}{40I_C} \approx \frac{1}{40 \times 5.2\times10^{-3}} \approx 4.8 \ \Omega.$$

**7.13** The circuit may be rearranged as follows




The circuit represents a common-base amplifier as described in Section 7.6.8 of the text. By an analysis similar to that given for Exercise 7.5 above we may determine that the quiescent output voltage is approximately 6.76 V and the quiescent collector/emitter current is about 2.24 mA.

The discussion of Section 7.6.8 shows that the input resistance of the circuit is given by

$$r_i \approx r_e \approx \frac{1}{40 I_E} \approx \frac{1}{40 \times 2.24\ \text{mA}} \approx 11\ \Omega$$

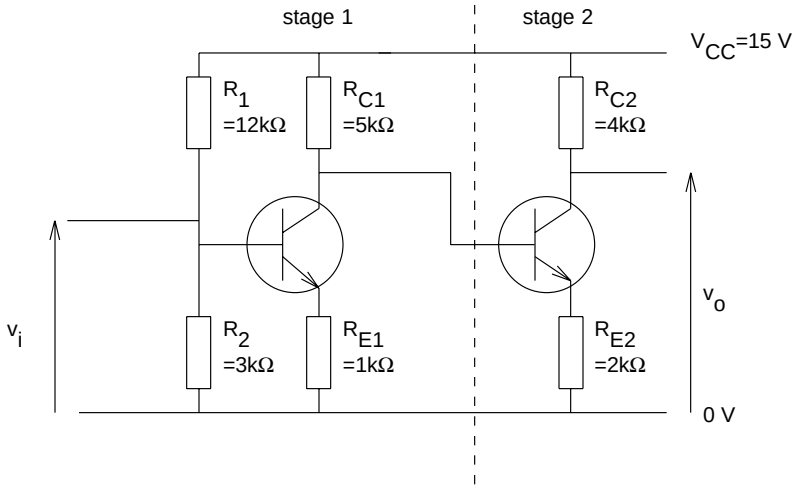
the output resistance is given by

$$r_o \approx R_C = 1\ \text{k}\Omega$$

and the voltage gain is

$$\text{voltage gain} \approx \frac{R_C}{r_e} \approx \frac{1000}{11} \approx 90$$

**7.14** A suitable circuit is shown below.




**7.15** Enter the circuit of the design (for example that given above) into PSpice using suitable transistors (e.g. a Q2N2222) and add a VSIN voltage source. Suitable settings for the VSIN parameters might be VAMPL = 0.2V, FREQ = 1k, VOFF = 0, AC = 0 and DC = 0. With a frequency of 1 kHz a suitable value for the capacitor is 10 uF. Add a viewpoint to the collector of each transistor to display the quiescent voltages and set up the analysis to evaluate bias point details and to perform a transient analysis. Suitable values for the transient analysis would be a step size of 20us and a final time of 2 ms.

Run the analysis and look at the input and output voltages. This should show that the notional voltage gain and the output swing are as required.

**7.16** Suitable component values for the circuit of Figure 7.34 are: $R$ = 20kΩ and $R_C$ = 10kΩ, with $V_{CC}$ = 12 V and $V_{EE}$ = -12 V. Almost any general purpose *npn* transistors could be used. In order to simulate the circuit the transistor must be within the component library and for PSpice Q2N2222 transistors would be suitable.

To simulate the circuit enter the circuit and add a 1 kΩ resistor from the base of T2 to ground, and a 1 kΩ resistor from the base of T1 to a VSIN voltage source

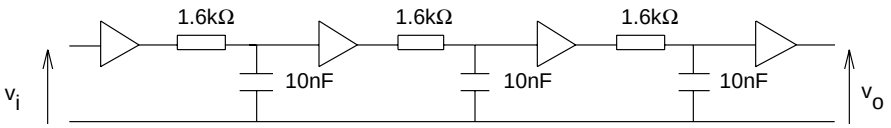
connected to ground. Suitable settings for the voltage source would be FREQ = 1k, VAMPL = 50mV, VOFF = 0, AC = 0, and DC = 0. Set up a transient analysis with a step value of 20us and a final time of 2ms. Run the analysis and display the output voltage $v_3$. Measure the magnitude of this signal and hence compute the gain from a single sided input to a single sided output. This gain will be about 173. Next remove the resistor connected to the base of T2 and connect this terminal of T2 to the base of T1 so that the sinusoidal input is applied to both transistors (a common-mode input). Again measure the output voltage $v_3$ and measure the ratio of this to the common-mode input voltage. This gain should be about 0.153. Thus the common-mode rejection ratio is about 173/0.153 = 1130.

The gain and CMRR measured above are for a single output. One could define the output as the differential signal $v_3 - v_4$. This would have approximately double the gain since $v_3$ and $v_4$ are complementary. Unfortunately, because the simulation uses identical transistors and resistors the circuit is exactly symmetrical and the differential output for a common-mode signal will be zero, giving an infinite CMRR.

# Chapter 8
# ANALOGUE SIGNAL PROCESSING

**8.1** The gain and phase responses for the two circuits are as shown in Figure 8.1 of the text. The cut-off frequencies for circuits (a) and (b) are 39.8 Hz and 15.9 kHz respectively.

**8.2**




Since the three stages are buffered the gain of the whole is simply the product of the gains of the stages.

The voltage gain of a single stage is given by

$$\text{voltage gain} = \frac{1}{1 + j\dfrac{f}{f_{co}}}$$

where $f_{co}$ is the cut-off frequency of a single stage. Therefore the voltage gain of the complete circuit is

$$\text{voltage gain} = \left(\frac{1}{1 + j\dfrac{f}{f_{co}}}\right)^3$$

At the −3 dB point

$$|\text{voltage gain}| = \frac{1}{\sqrt{2}}$$

Therefore

$$\left|\left(\frac{1}{1 + j\dfrac{f}{f_{co}}}\right)^3\right| = \frac{1}{\sqrt{2}}$$

Thus

$$\left|1 + j\frac{f}{f_{co}}\right| = \sqrt[6]{2} = 1.122$$

and

$$1 + \left(\frac{f}{f_{co}}\right)^2 = 1.26$$

giving

$$f = f_{co} \times 0.510$$

In this case

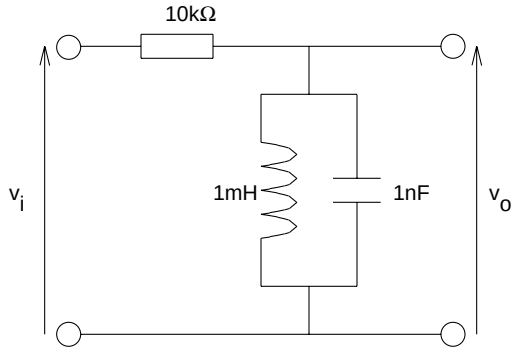
$$f_{co} = \frac{1}{2\pi\ 10^{-8}\ 1.6\times10^{3}} = 9947 \text{ Hz}$$

and therefore the bandwidth of the three stage filter is given by

$$f = f_{co} \times 0.510 = 9947 \times 0.510 = 5.07 \text{ kHz.}$$

**8.3** The simplest way to perform this exercise is to load FILE 8A and to edit the component values to match those in the question. The input voltage source may be set to a magnitude of 1V and the analysis set up for an AC sweep. Suitable parameters for the sweep would be a decade sweep from 10Hz to 100kHz with 101 points per decade. When the analysis is complete Probe can be used to measure the cut-off frequency (where the magnitude falls to 0.707V) which will be found to be exactly as predicted in the last exercise.

**8.4**




The frequency response is as shown in Figure 8.7(a) of the text, with the resonant frequency given by

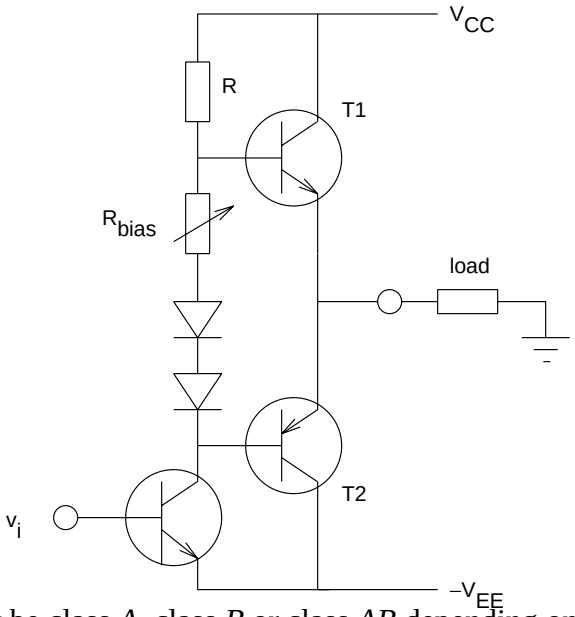
$$f_o = \frac{1}{2\pi\sqrt{(LC)}} = \frac{1}{2\pi\ \sqrt{(10^{-3}\ 10^{-9)}}} \approx 160 \text{ kHz}$$

The *Q* of the circuit is the ratio of the bandwidth and the centre frequency. It is known as the *quality factor* of the circuit.

**8.5** The requirements of filters differ considerably between applications. In many cases an ideal filter of the form shown in Figure 8.7(a) would be desirable but unfortunately such a characteristic is not achievable. Various approximations are available which may be selected according to their characteristics. For example some produce a very sharp cut-off but suffer from great variations in their gain within the pass-band. Others have a relatively constant gain within their pass-band but produce considerable phase distortion. A compromise is required where the important characteristics are selected for a given application.

**8.6** Simulating the circuit within FILE 8D will show that the centre frequency $f_o$ of this filter is about 1.46 kHz and the bandwidth is about 3.42 kHz. The Q is given by $f_o$/BW which is about 0.43.

**8.7**




The amplifier may be class *A*, class *B* or class *AB* depending on the setting of $R_{bias}$ (see Section 8.3.2).

**8.8** Class *AB* is generally preferred to class *B* for audio power amplifiers because it produces much less crossover distortion (see Section 8.3.2). The disadvantage of class *AB* in comparison with class *B* is that it has a high power dissipation. This increases the amount of heat which must be dissipated.

**8.9** Inductive and capacitive sensors always have some resistance associated with them and are thus always sources of thermal noise.

**8.10** From the discussion of Section 8.4.1 we know that, at normal ambient temperature,

$$V_n\,(\text{r.m.s.}) = (4kTBR)^{\frac{1}{2}}$$

$$= 1.27 \times 10^{-10} \times (BR)^{\frac{1}{2}}$$

Substituting values for $B$ and $R$ gives

$$V_n\,(\text{r.m.s.}) = 1.27 \times 10^{-10} \times (5{\times}10^6\ 10{\times}10^3)^{\frac{1}{2}}$$

$$\approx 28\ \mu\text{V}.$$

**8.11** From Equation 8.3 we have

$$I_n\,(\text{r.m.s.}) = (2qBI)^{\frac{1}{2}}$$

Substituting values for $q$, $B$ and $I$ gives

$$I_n\,(\text{r.m.s.}) = (2 \times 1.6{\times}10^{-19} \times 5{\times}10^6 \times 10^{-9})^{\frac{1}{2}}$$

$$= 4{\times}10^{-11}\ \text{A}$$

This represents 4% of the signal current.

**8.12** White noise has a uniform spectral density, that is, it has components at all frequencies with equal noise power. Pink noise has a spectrum in which most of the power is concentrated at lower frequencies. Here the power halves for a doubling of frequency. It is also called 1/f noise.

**8.13** Three natural sources include lightning, solar emissions and cosmic radiation. Man-made sources include automotive ignition systems, mobile phones, electric motors, etc.

**8.14** Narrow band sources include mobile phones and the internal oscillators within superheterodyne radio receivers. Wide band sources include circuit breakers, power distribution systems and automobile ignition systems.

**8.15** Design techniques to reduce the susceptibility of a system to radiated interference are discussed in Section 8.5.5 of the text. Techniques include opto-isolation of input lines and the use of mains filters.

**8.16** Design techniques to reduce the susceptibility of a system to conductive interference are discussed in Section 8.5.5 of the text. Techniques include the use of screened enclosures and cables.

**8.17** This topic is discussed in Section 8.5.4. The primary mechanisms of electromagnetic coupling between the various stages of an electronic system may be divided into those related to radiated energy and those related to conducted energy. Noise often radiates from power supply or from drive circuits and this may affect sensitive sections of the system. Noise may also be conducted into the system from sensors and actuators, or between modules within the system, through signal lines. Power supply and earth lines also provide a a route for noise.

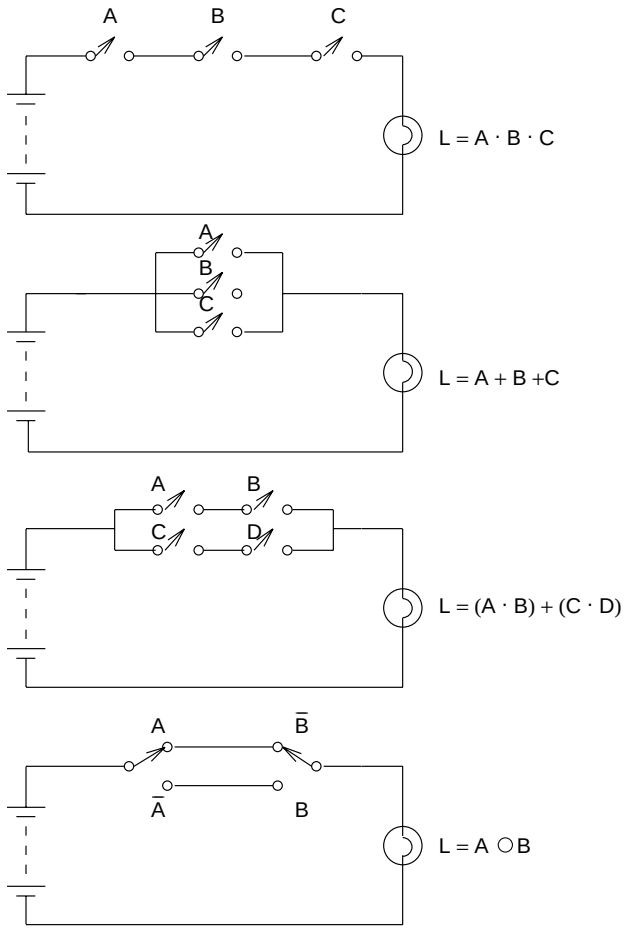
**8.18** The importance of circuit layout in relation to EMC is discussed in Section 8.5.5.

**8.19** The choice of grounding techniques, and considerations of frequency are discussed in Section 8.5.5 in the subsection on "Circuit partitioning and grounding".

**8.20** The relevance of quality to EMC is discussed in Section 8.5.6.

# Chapter 9
# DIGITAL SYSTEMS

**9.1**




**9.2** The two arrangements may be described by the following (non-unique) expressions

$$L = A\ ((B \cdot C) + E) \cdot (D + F) \cdot G$$

$$L = (A \cdot B \cdot D \cdot F) + (A \cdot \bar{B} \cdot E \cdot \bar{F}) + (\bar{A} \cdot C \cdot \bar{D} \cdot F) + (\bar{A} \cdot \bar{C} \cdot \bar{E} \cdot \bar{F})$$

**9.3** The first would require $2^7 = 128$ lines, the second would require $2^6 = 64$ lines.

**9.4** (i) The truth tables for the two arrangements are as below

| A | B | C |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

(a)

| A | B | C |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

(b)

(ii) The first arrangement may be described by the following Boolean expression

$$C = \overline{A} + \overline{B}$$

this may be manipulated using DeMorgan's theorem to the form

$$C = \overline{A \cdot B}$$

which is clearly equivalent to the second arrangement.

**9.5** (i) The arrangements may be described by the following truth tables

| A | B | C |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

(a)

| A | B | C |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

(b)

(ii) The first arrangement may be described by the following Boolean expression

$$C = \overline{A} \cdot \overline{B}$$

this may be transformed using DeMorgan's theorem to

$$C = \overline{A + B}$$

which is clearly equivalent to the second arrangement.

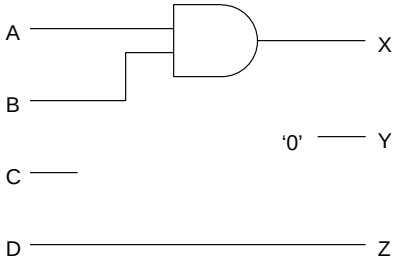
**9.6** From the diagram $X$ is given by $A \cdot B$. This does not simplify.
$Y$ is given by the expression

$$Y = A \cdot B \cdot (\overline{B + C})$$
$$= A \cdot B \cdot (\overline{B} \cdot \overline{C}) = 0$$

Thus $Z$ is given by

$$Z = Y + D = 0 + D = D$$

and therefore the arrangement may be simplified to




**9.7**

X

| C \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 |

$X = \bar{B} + AC$

Y

| CD \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 0 | 1 | 1 |
| 01 | 0 | 1 | 1 | 1 |
| 11 | 0 | 0 | 0 | 0 |
| 10 | 1 | 0 | 0 | 1 |

$Y = \bar{B}\bar{D} + A\bar{C} + B\bar{C}D$

Z

| CD \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 1 | 0 | X |
| 01 | 0 | X | 1 | 0 |
| 11 | 0 | 1 | X | 0 |
| 10 | X | 1 | 0 | 1 |

$Z = \bar{B}\bar{D} + BD + \bar{A}B$

**9.8**

$110101_2 = 53_{10}$

$754_8 = 492_{10}$

$A\,10E_{16} = 41230_{10}$

**9.9**

$67_{10} = 1000011_2$

$3.625_{10} = 11.101_2$

$635_8 = 110\ 011\ 101_2$

$8FE_{16} = 1000\ 1111\ 1110_2$

**9.10** $48602_{10} = BDDA_{16}$

$307_8 = C7_{16}$

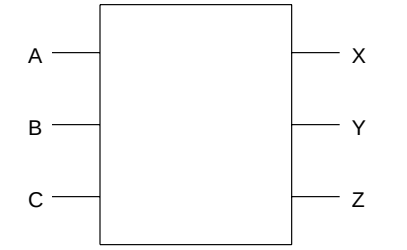
$1100101_2 = 65_{16}$

**9.11**

```
  1 0 1 1 1          1 1 0 1 0 1          1 0 1 1
+ 1 0 0 1          - 1 1 0 1 0          x 1 1 1
-----------          -----------          -------
1 0 0 0 0 0            1 1 0 1 1            1 0 1 1
                                          1 0 1 1 0
                                        1 0 1 1 0 0
                                        -----------
                                      1 0 0 1 1 0 1
```

```
                  1 1 1
              -------------
1 1 0 ) 1 0 1 0 1 0
        1 1 0
        -----
          1 0 0 1
            1 1 0
          -------
              1 1 0
              1 1 0
              -----
              - - -
```

**9.12** The required system may be described by the following block diagram and truth table.




| A | B | C | X | Y | Z |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 |

From the truth table a series of Karnaugh maps may be formed and Boolean expressions found for the outputs.

X

| C \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 |

$X = A$

Y

| C \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 |

$Y = \bar{A}B + B\bar{A}$

$= A \bigcirc B$

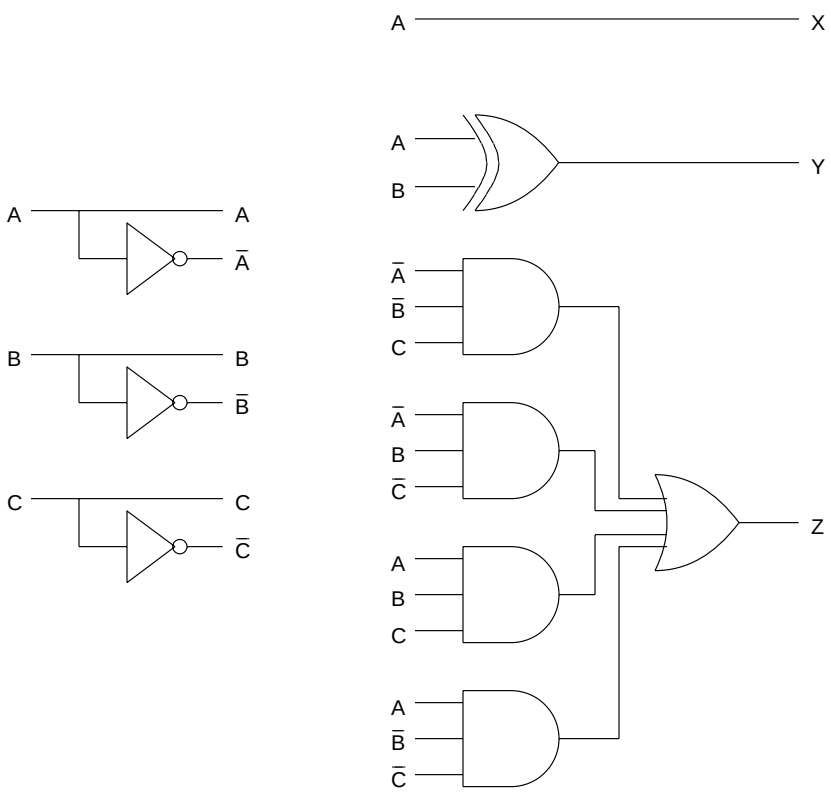
Z

| C \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 |

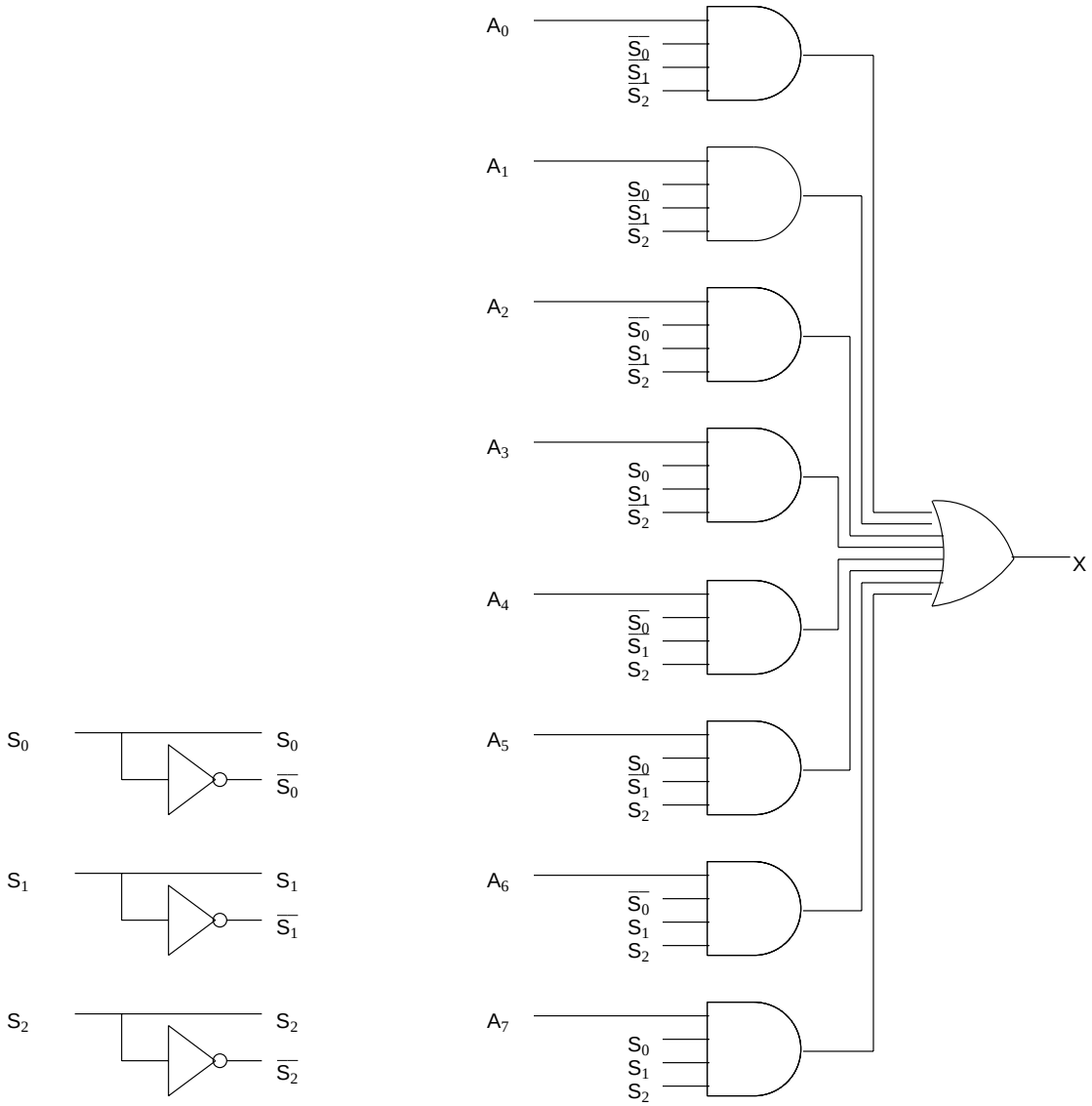
$Z = \bar{A}\bar{B}C + \bar{A}B\bar{C}$

$+ ABC + A\bar{B}\bar{C}$

From these expressions appropriate circuits may be designed.



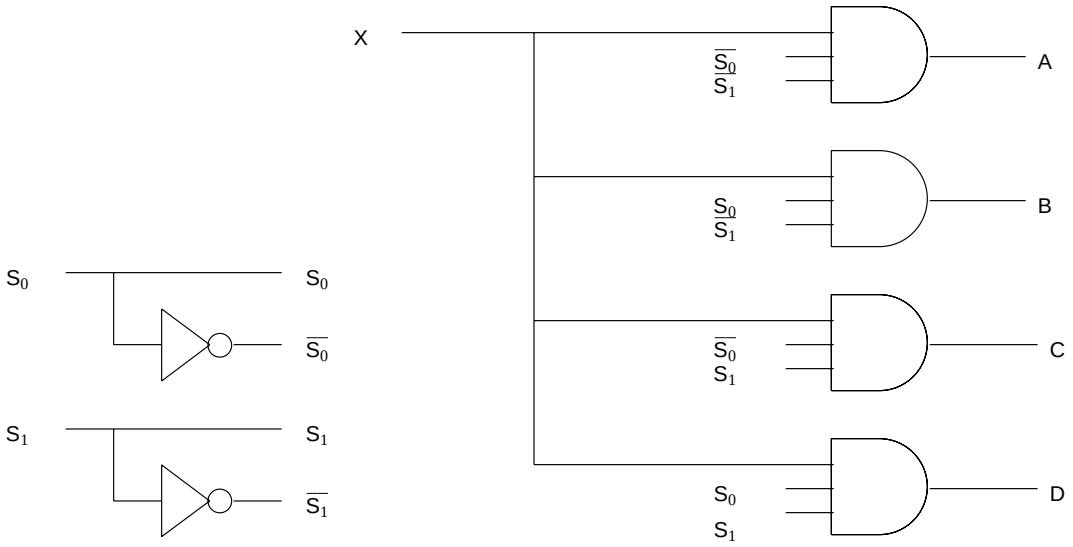
**9.13** A suitable design is as follows.




**9.14** The operation of this circuit can be demonstrated in a number of ways within PSpice. Perhaps one of the most visual means is to adopt a similar approach to that used in computer simulation exercise 9.1 as demonstrated in FILE 9A. This uses logic nodes HI or LOW for each input and displays the output voltage level using a viewpoint. This allows the inputs to be changed and the results to be seen instantly on the schematic by running the simulation.

The evaluation version of PSpice does not include an 8 input OR gate so this function must be produced using a combination of simpler gates. A resistor connected to ground must be connected to the output of the final gate to produce a voltage that can be displayed using a viewpoint. A value of 10k is suitable.

**9.15** A suitable design is as follows.




**9.16** The operation of this circuit can be demonstrated in a number of ways within PSpice. As described above for Exercise 9.14, perhaps one of the most visual means is to adopt a similar approach to that used in computer simulation exercise 9.1 as demonstrated in FILE 9A. This uses logic nodes HI or LOW for each input and displays the output voltage levels using viewpoints. This allows the inputs to be changed and the results to be seen instantly on the schematic by running the simulation.

The evaluation version of PSpice does not include a 4 input OR gate so this function must be produced using a combination of simpler gates. Restistors to ground must be connected to the outputs of the output gates to produce voltages that can be displayed using viewpoints. A value of 10k is suitable.

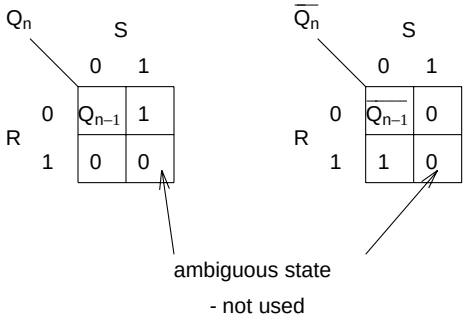
# Chapter 10
# SEQUENTIAL LOGIC

**10.1** The terms bistable, monostable and astable are defined in Section 10.1 of the text.

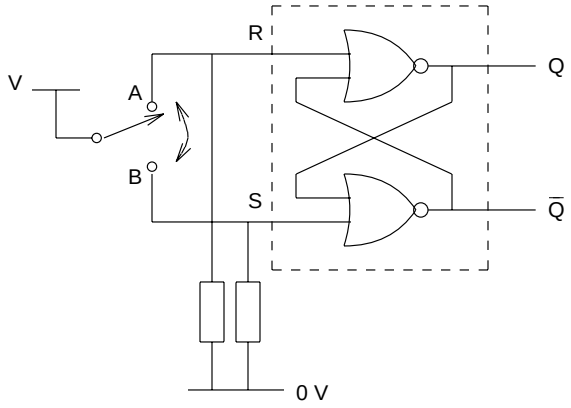
**10.2** The *S* input *Sets* the *Q* output to 1, while the *R* input *Resets* the *Q* output to 0.

**10.3** In an S–R bistable formed using two NOR gates, the inputs are active-high. The transition table and Karnaugh map of such a circuit are shown below.

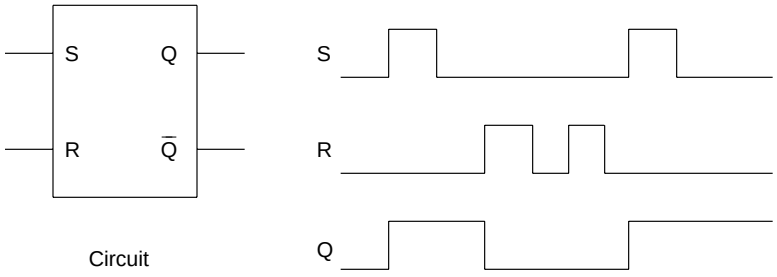
| S | R | $Q_n$ | $\overline{Q_n}$ | |
|---|---|---|---|---|
| 0 | 0 | $Q_{n-1}$ | $\overline{Q_{n-1}}$ | No change |
| 0 | 1 | 0 | 1 | RESET |
| 1 | 0 | 1 | 0 | SET |
| 1 | 1 | 0 | 0 | Ambiguous state |

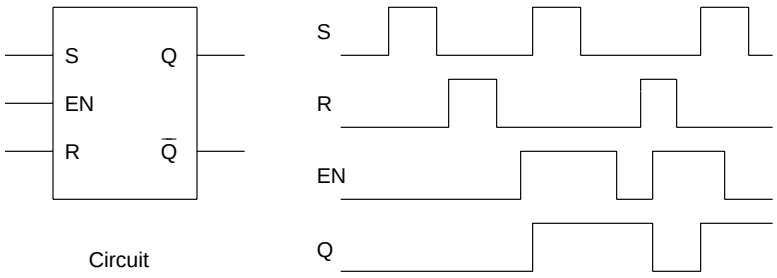


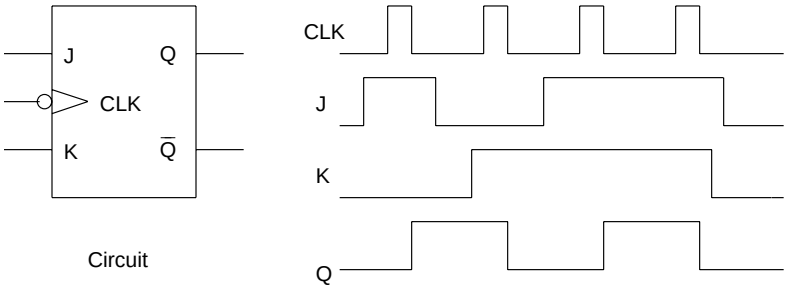

**10.4** Switch bounce can cause problems if it is connected to circuitry which senses the state of the switch during the period of time in which it is bouncing, or if the signal is used as the input of a counter. The circuit given below will remove the effects of switch bounce from a changeover switch.



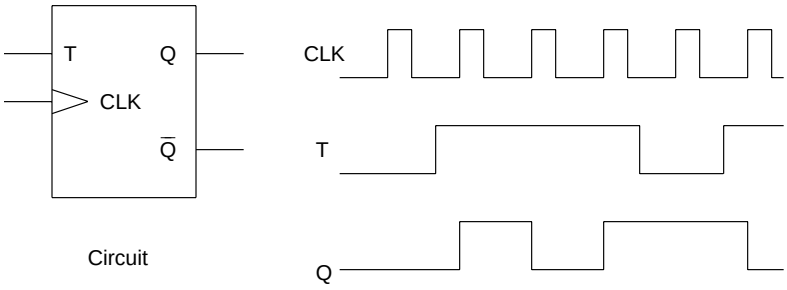

**10.5** The diagram below shows the waveform at the $Q$ output of the circuits, in each case it is assumed that the $Q$ output was previously at 0.






Circuit

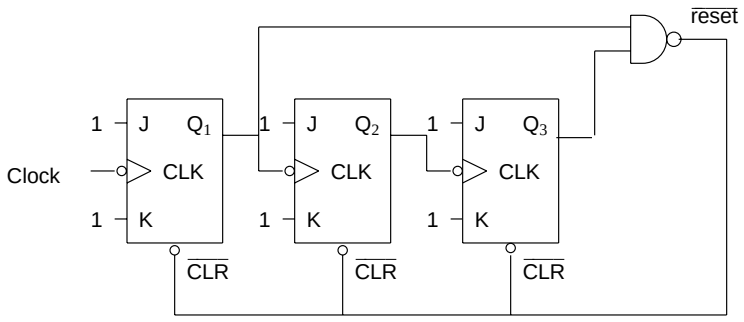



Circuit

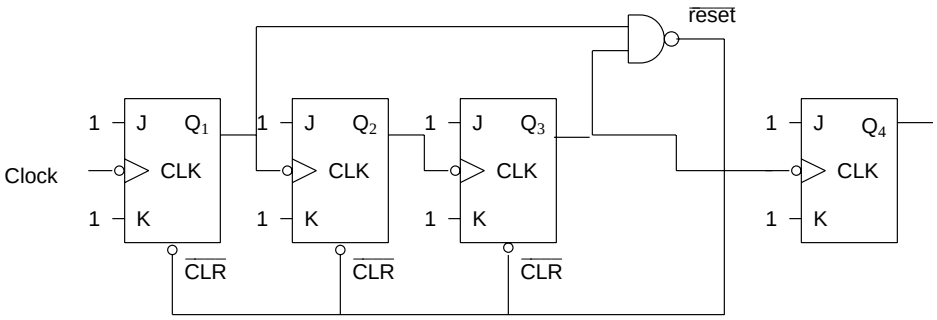
**10.6** In a synchronous counter all the elements change state at the same time, this being determined by a clock signal. This ensures that a short time after the clock signal changes, all the stages will have responded and the counter may be read.

In an asynchronous counter the output of one stage forms the input of the next. Thus changes ripple through the counter with each stage producing a slight delay. This arrangement is simpler than a synchronous counter but has problems at high speeds.

**10.7** The diagram below shows a suitable circuit.

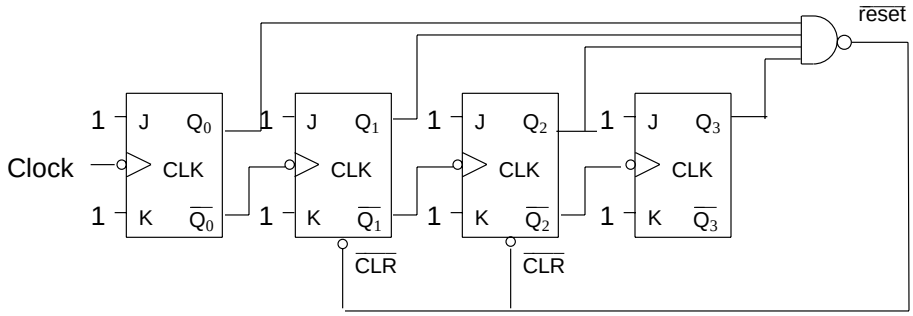


**10.8** A suitable circuit may be formed by adding a divide-by-two stage at the end of the modulo-5 counter described in the last exercise.




**10.9** The above circuit can be simulated very easilly in PSpice. Enter the circuit into the schematics editor using 7473 J-K flip-flops and a 7400 2-input NAND gate. Use a DSTM for the clock input. Suitable parameters for this digital signal source are DELAY = 0.5us, ONTIME = 0.5us and OFFTIME = 0.5us. Hi logic nodes can be used to set all the J and K input to logic 1. The CLR input of the output flip-flop should also be set Hi. Set up the analysis options to perform a transient analysis. Suitable parameters are a Print Step of 200ns and a Final Time of 12 us. Put level markers on the outputs of each flip-flop and on the reset signal. Then run the analysis and observe the outputs. This should show a square wave on the final output with a period of 10us as expected.

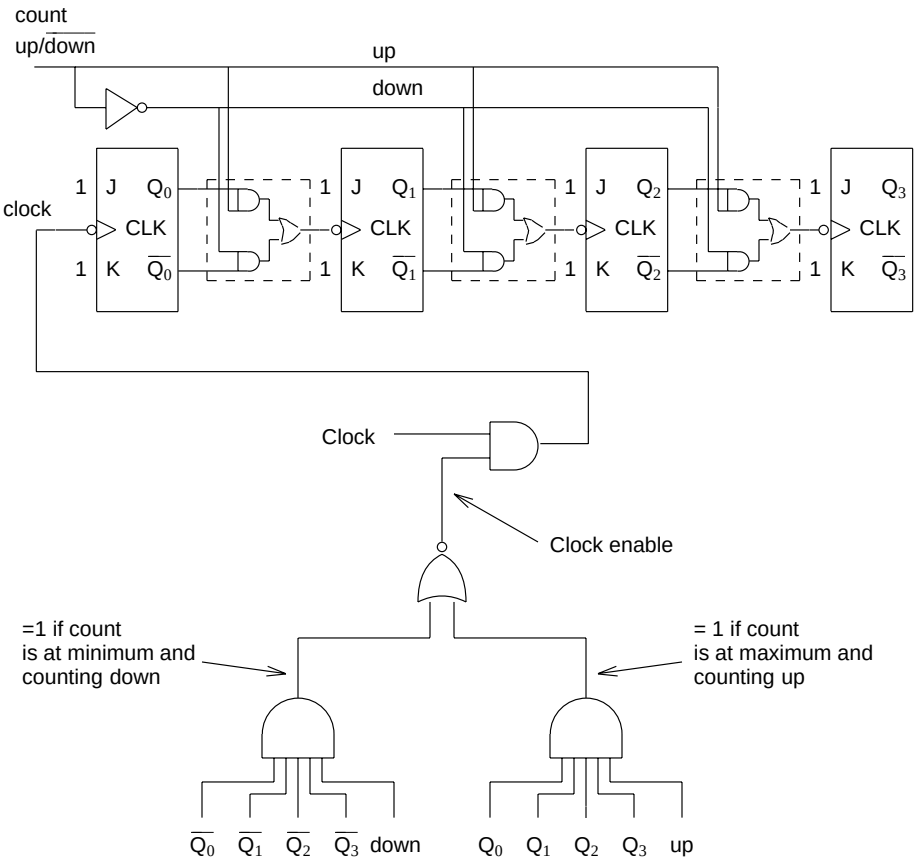
**10.10** The functionality required can be achieved by combining the techniques used to generate the decade up-counter, with those of the ripple down-counter. This takes a four bit down counter and adds circuitry to detect the number following the last required number, and uses the occurence of this number to reset the system into the first number of the sequence required. In this example the last number of the sequence is zero and the following number is therefore 15 (all 1's). Therefore circuitry is added to detect the number 15 and to reset the counter to 9. The resultant circuit is shown below.




**10.11** If the above circuit is simulated (using an approach similar to that outlined for exercise 10.9 above) it will be found that the circuit does *not* operate correctly. The problems encountered are related to *races* within the circuit caused by the small delays

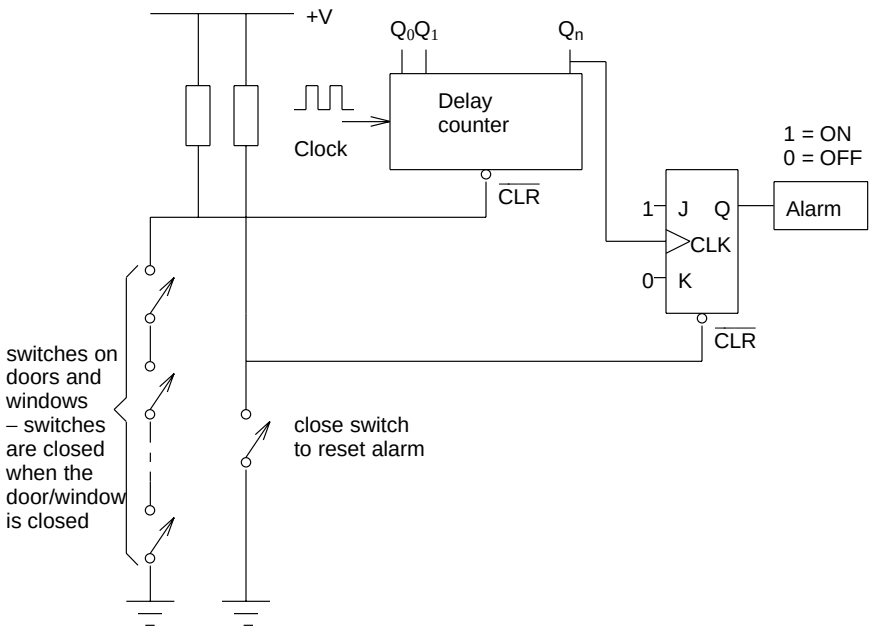
introduced by each device. Our simple theory would suggest that the reset output of the NAND gate should be low only after the counter has counted down to zero and then moved on to a count of all 1's. However, if the output of this gate is displayed it will be seen that the output goes low at other times during the counting process. This is caused by the finite time that it takes for each flip-flop to change state as discussed in Section 10.3.4. Although the fairly simply circuits given in the text give an insight into the design of various forms of counters, the circuits used within integrated circuit counters are invariably slightly more complicated to deal with issues such as race hazards. This example provides a useful illustration of some of the limitations of these simple circuits.

**10.12** The circuit below shows a possible solution.




Such a counter might be used in an application where a gain or level is being set. For example a digital volume control where one might push a button to increase or decrease the volume. One would not want the volume to go to minimum if one continued to push the button when maximum had been reached.

**10.13** The diagram below shows a possible solution.




Here the S–R bistable has been replaced by a clocked J–K device and a counter has been added to provide a 30 second delay.

The delay is in the form of a counter which counts pulses from an oscillator. The counter and oscillator frequency are chosen such that if the counter starts from zero the most significant bit of the counter, $Q_n$, is set after 30 seconds.

The $Q_n$ output from the counter acts as a clock to a J–K bistable which is arranged such that a positive transition on the clock will set the $Q$ output to 1. This output is connected to the alarm.

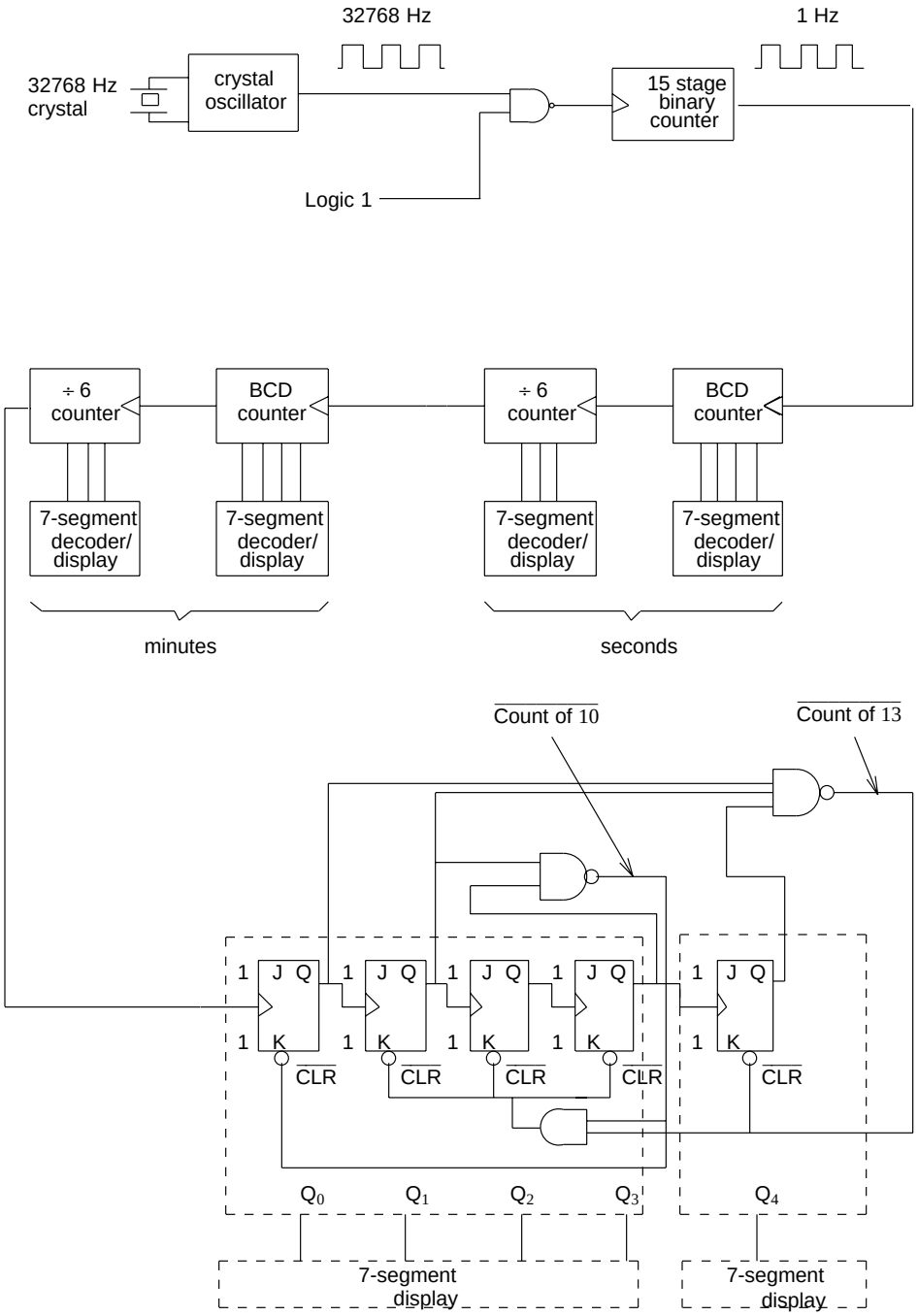
The various door and window switches are connected in series with a pull-up resistor and the combination is connected to the $\overline{CLR}$ input of the counter. Therefore while the doors and windows are closed the counter is held with all its outputs at zero. If now one of the switches is opened the counter will no longer be held in its reset mode and will begin to count up. After 30 seconds the $Q_n$ output will go high and the positive going transition will act as a clock trigger to the bistable setting the $Q$ output high and turning ON the alarm. Either before or after the alarm has been triggered the bistable may be cleared by closing the reset switch. This will turn OFF the alarm if it is sounding, or prevent it from sounding if it is left closed.

This simple arrangement fulfills the requirements given in the Exercise, but is perhaps not an ideal solution since a door may be opened and closed quickly without triggering the alarm. A more sophisticated design would therefore be adopted. It is worth noting that even at this relatively low level of complexity a real system would probably use a single-chip microcomputer rather than discrete counters and bistables. This would allow much more sophisticated facilities to be produced in software.

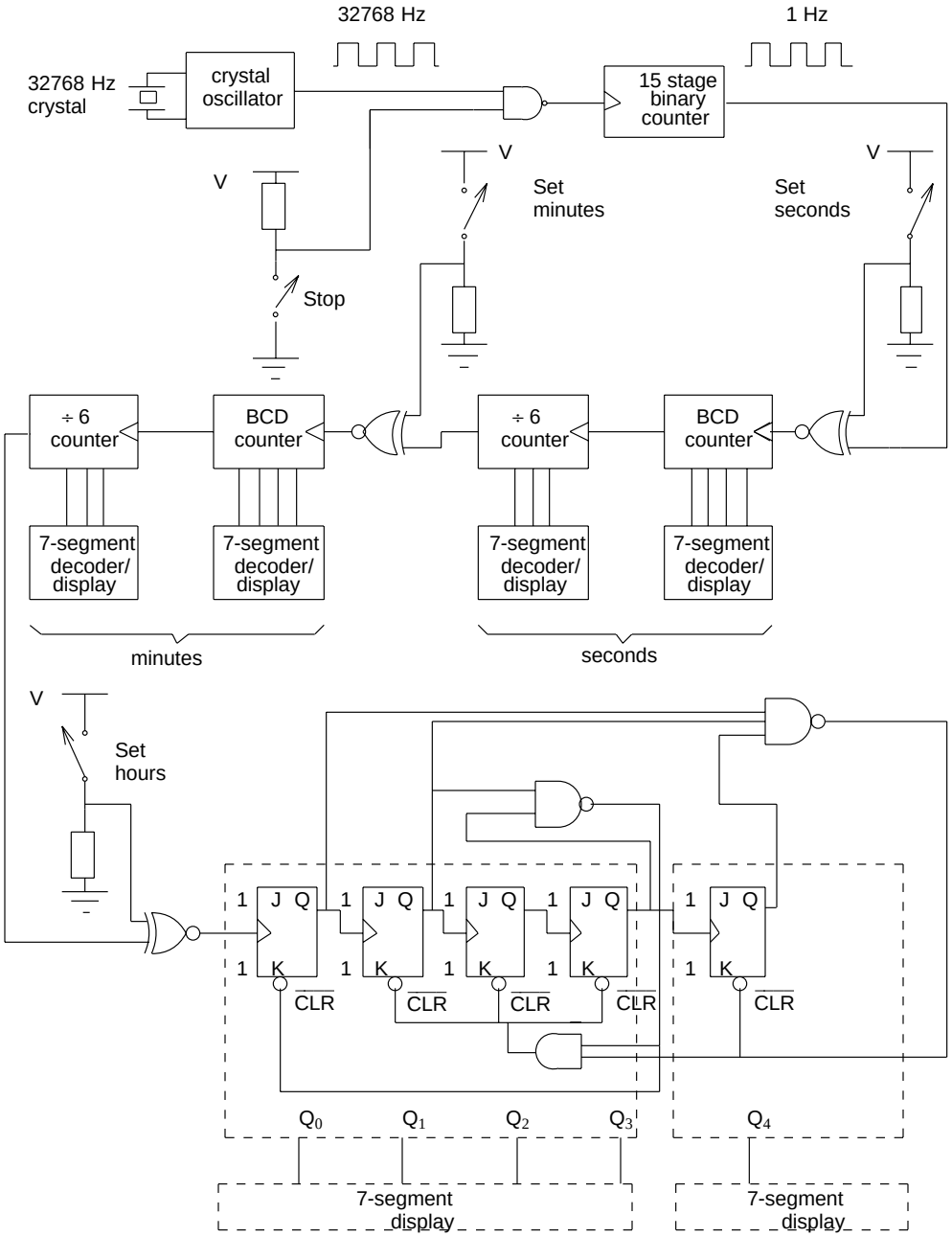
**10.14** A suitable clock may be formed by extending the arrangement shown in Figure 10.65, to include a counter and display for the hours function. This may be driven from the output of the minutes stage in the same way that the minutes are driven from the seconds stage. Since we are now considering a clock rather than a stop-watch, the stop, start and reset functions are inappropriate. We will consider setting of the clock in the next exercise.

The hours section requires a two stage counter to measure units and tens of hours. The unusual feature of this stage is that the counter must count from 1 to 12 rather than from 0 to 11. This is achieved using a modified version of the divide-by-N counter where a count of 13 is detected and used to clear the bits of the count. In this case the clear is applied to all bits except the least significant bit. Since this bit is set to 1 for a count of 13 the result is that the counter is reset to 1 rather than to 0. This arrangement is shown overleaf.

The least significant bit of the 4-bit counter is cleared when a count of ten is detected but not when a count of 13 is reached. The other bits of the 4-bit counter are cleared both at a count of 10 and a count of 13. The divide by 2 stage is cleared when 13 is reached.


32768 Hz
1 Hz
32768 Hz
crystal
crystal
oscillator
15 stage
binary
counter
Logic 1
÷ 6
counter
BCD
counter
÷ 6
counter
BCD
counter
7-segment
decoder/
display
7-segment
decoder/
display
7-segment
decoder/
display
7-segment
decoder/
display
minutes
seconds
Count of 10
Count of 13
J Q
K
CLR
Q0
Q1
Q2
Q3
Q4
7-segment
display
7-segment
display

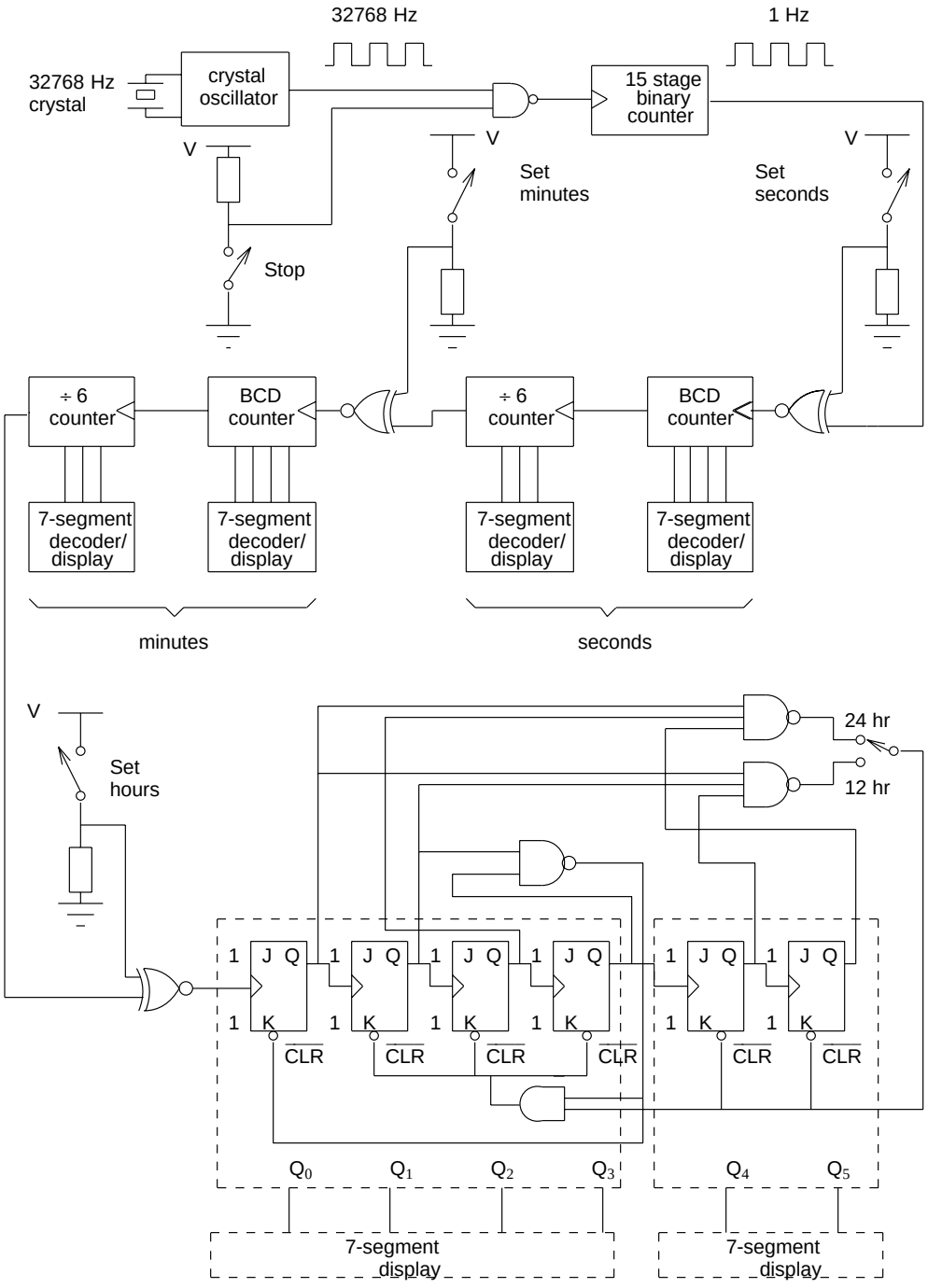
**10.15** One method of incrementing the seconds, minutes and hours settings of the clock of the last exercise is to use push-buttons as shown below.



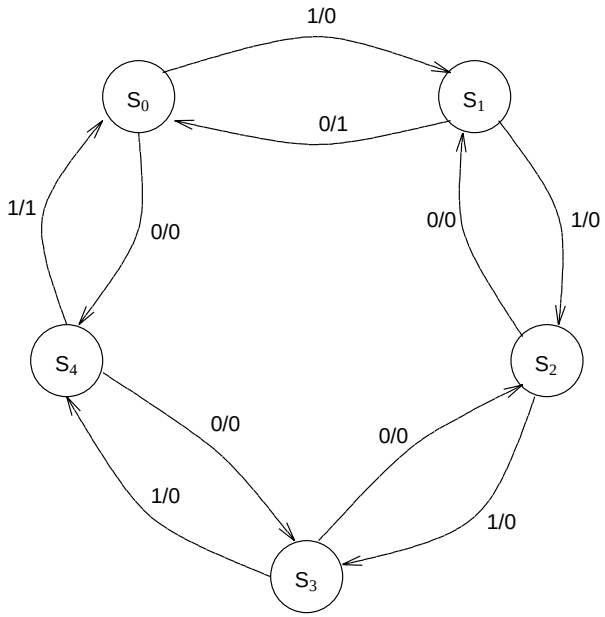

It is useful to be able to stop the normal timing function of the clock while setting the time. This is achieved by gating the oscillator output through a NAND gate with one input to this gate coming from a switch. Incrementing the individual stages of the clock is achieved by adding an exclusive-OR gate at the input of each stage. One of the inputs to each of these gates comes from a normally-open push-button. When the switch is open the exclusive-OR gate has a 0 on one of its inputs and it therefore passes the other input to its output unchanged. If the push-button is now depressed the output signal will be inverted (irrespective of its state). Thus depressing and releasing the push-button will cause the input to the corresponding stage to see an input which changes state and then reverts to its original state. This will always produce a single positive going edge which will increment that stage by one. The process is repeated until the appropriate time is reached.

Although the above design is appropriate for students at this level it is not an ideal solution. Firstly, incrementing one stage of the counter through its maximum value and back to zero will have the effect of incrementing the next stage. Also, the switches will certainly exhibit switch bounce which will result in multiple increments for one depression of the switch. It is worth pointing out these deficiencies but probably not worth attempting to overcome them within the design. In practice, a design of this complexity would not be performed using discrete gates.

**10.16** Some 24 hour clocks display hours in the range 1 to 24 and others in the range 0 to 23. For simplicity in this exercise we will assume the former operation. In order to count up to 24 hours an additional bistable must be added to the tens counter of the hours stage. The only other modification required to our clock is that additional circuitry must be added to detect a count of 25, and the reset signal to both stages must be switchable between this detector and that detecting a count of 13. This arrangement is shown overleaf.


32768 Hz
1 Hz
32768 Hz crystal
crystal oscillator
15 stage binary counter
V
V
V
Set minutes
Set seconds
Stop
÷ 6 counter
BCD counter
÷ 6 counter
BCD counter
7-segment decoder/ display
7-segment decoder/ display
7-segment decoder/ display
7-segment decoder/ display
minutes
seconds
V
Set hours
24 hr
12 hr
1 J Q
1 K
CLR
Q0
Q1
Q2
Q3
Q4
Q5
7-segment display
7-segment display

**10.17** The design methodology for this exercise is as described in Section 10.21.1. A state transition diagram is shown below in which the transitions are $D/Q$.




This may be used to form a state transition table.

| Present state | Input conditions D | Next state | Output Q |
|---|---|---|---|
| $S_0$ | 0 | $S_4$ | 0 |
| | 1 | $S_1$ | 0 |
| $S_1$ | 0 | $S_0$ | 1 |
| | 1 | $S_2$ | 0 |
| $S_2$ | 0 | $S_1$ | 0 |
| | 1 | $S_3$ | 0 |
| $S_3$ | 0 | $S_2$ | 0 |
| | 1 | $S_4$ | 0 |
| $S_4$ | 0 | $S_3$ | 0 |
| | 1 | $S_0$ | 1 |

Inspection of the state table will show that all the states are unique and that no state reduction is possible.

For a system with 5 internal states, three internal variables are needed. These are assigned as shown below

| State | Internal variables ABC |
|---|---|
| $S_0$ | 000 |
| $S_1$ | 001 |
| $S_2$ | 010 |
| $S_3$ | 011 |
| $S_4$ | 100 |

This allows us to represent the state transition table in terms of the internal variables.

| Present state ABC | Input conditions D | Next state ABC | Output Q |
|---|---|---|---|
| 000 | 0 | 100 | 0 |
| | 1 | 001 | 0 |
| 001 | 0 | 000 | 1 |
| | 1 | 010 | 0 |
| 010 | 0 | 001 | 0 |
| | 1 | 011 | 0 |
| 011 | 0 | 010 | 0 |
| | 1 | 100 | 0 |
| 100 | 0 | 011 | 0 |
| | 1 | 000 | 1 |

At this stage we must decide on a method of implementation. Let us assume that, as in the example in the text, we are to use J–K flip-flops. The control inputs of these devices may be described by the following table

| Present state $Q_n$ | Next state $Q_{n+1}$ | Control inputs required J | K |
|---|---|---|---|
| 0 | 0 | 0 | X |
| | 1 | 1 | X |
| 1 | 0 | X | 1 |
| | 1 | X | 0 |

From the state transition table and the control data for the flip-flop we can construct an excitation table as below.

| Present state ABC | Input conditions D | Next state ABC | Flip-flop inputs | | | | | | Output |
|---|---|---|---|---|---|---|---|---|---|
| | | | $J_A$ | $K_A$ | $J_B$ | $K_B$ | $J_C$ | $K_C$ | Q |
| 000 | 0 | 100 | 1 | X | 0 | X | 0 | X | 0 |
| | 1 | 001 | 0 | X | 0 | X | 1 | X | 0 |
| 001 | 0 | 000 | 0 | X | 0 | X | X | 1 | 1 |
| | 1 | 010 | 0 | X | 1 | X | X | 1 | 0 |
| 010 | 0 | 001 | 0 | X | X | 1 | 1 | X | 0 |
| | 1 | 011 | 0 | X | X | 0 | 1 | X | 0 |
| 011 | 0 | 010 | 0 | X | X | 0 | X | 1 | 0 |
| | 1 | 100 | 1 | X | X | 1 | X | 1 | 0 |
| 100 | 0 | 011 | X | 1 | 1 | X | 1 | X | 0 |
| | 1 | 000 | X | 1 | 0 | X | 0 | X | 1 |
| 101 | XX | XXX | X | X | X | X | X | X | X |
| 110 | XX | XXX | X | X | X | X | X | X | X |
| 111 | XX | XXX | X | X | X | X | X | X | X |

This may be implemented by hardware as shown in Figure 10.58 of the text, where the details of the combinational logic are described by the following Karnaugh maps.

$J_A$

| CD \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 0 | X | X |
| 01 | 0 | 0 | X | X |
| 11 | 0 | 1 | X | X |
| 10 | 0 | 0 | X | X |

$J_A = \overline{B}\overline{C}\overline{D} + BCD$

$K_A$

| CD \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | X | X | X | 1 |
| 01 | X | X | X | 1 |
| 11 | X | X | X | X |
| 10 | X | X | X | X |

$K_A = 1$

$J_B$

| CD \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | X | X | 1 |
| 01 | 0 | X | X | 0 |
| 11 | 1 | X | X | X |
| 10 | 0 | X | X | X |

$J_B = A\overline{D} + CD$

$K_B$

| CD \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | X | 1 | X | X |
| 01 | X | 0 | X | X |
| 11 | X | 1 | X | X |
| 10 | X | 0 | X | X |

$K_B = \overline{C}\overline{D} + CD$

$J_C$

| CD \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 1 | X | 1 |
| 01 | 1 | 1 | X | 0 |
| 11 | X | X | X | X |
| 10 | X | X | X | X |

$J_C = B + A\overline{D} + \overline{A}D$

$K_C$

| CD \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | X | X | X | X |
| 01 | X | X | X | X |
| 11 | 1 | 1 | X | X |
| 10 | 1 | 1 | X | X |

$K_C = 1$

The output logic is described by the following Karnaugh map.

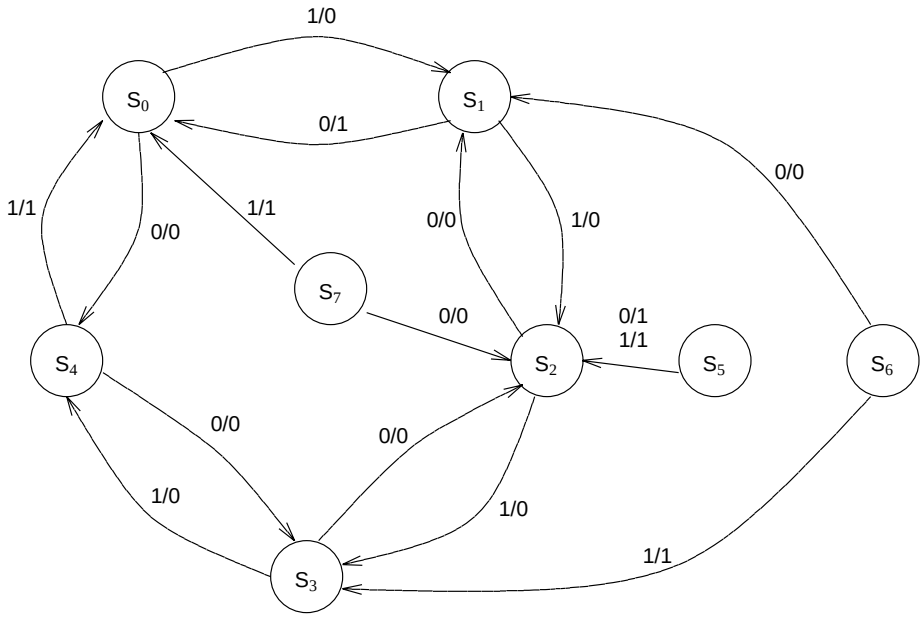
Q

| CD \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | X | 0 |
| 01 | 0 | 0 | X | 1 |
| 11 | 0 | 0 | X | X |
| 10 | 1 | 0 | X | X |

$Q = \overline{B}C\overline{D} + AD$

The combinational logic required may then be implemented directly as described in Section 10.12.1.

Having designed the counter it is now necessary to investigate the nature of the unused states to ensure that the counter starts correctly. A full transition diagram is as follows.




It is clear from the above diagram that the unused states cause no problems. In each case after a single clock cycle the system will be in one of the used states.

**10.18** The arrangement has two stable states, $S_0$ and $S_2$. In each of these states the output is 0. Taking the input to 1 while in state $S_0$ will cause it to leave this state and to enter state $S_3$ where the output is 1. From this state it will always enter state $S_2$ on the next clock pulse, and the output will return to 0. While the input stays high it will remain in state $S_2$. When in state $S_2$ taking the input low will cause it to leave this state and go, via state $S_1$ (where the output is high) to state $S_0$ (where the output is low). Thus when the input is 0 it will move to, and remain in, state $S_0$ and when the input is 1 it will move to, and remain in, state $S_2$. In each case the output goes high for one clock period when it leaves one of the stable states.

**10.19** The design methodology for this exercise is as described in Section 10.21.1.

The state diagram may be used to form a state transition table. In this table the input is given the label $D$ and the output the label $Q$.

| Present state | Input conditions D | Next state | Output Q |
|---|---|---|---|
| $S_0$ | 0 | $S_0$ | 0 |
| | 1 | $S_3$ | 1 |
| $S_1$ | 0 | $S_0$ | 0 |
| | 1 | $S_0$ | 0 |
| $S_2$ | 0 | $S_1$ | 1 |
| | 1 | $S_2$ | 0 |
| $S_3$ | 0 | $S_2$ | 0 |
| | 1 | $S_2$ | 0 |

Inspection of the state table will show that all the states are unique and that no state reduction is possible.

For a system with 4 internal states, two internal variables are needed. These are assigned as shown below

| State | Internal variables AB |
|---|---|
| $S_0$ | 00 |
| $S_1$ | 01 |
| $S_2$ | 10 |
| $S_3$ | 11 |

This allows us to represent the state transition table in terms of the internal variables.

| Present state ABC | Input conditions D | Next state ABC | Output Q |
|---|---|---|---|
| 00 | 0 | 00 | 0 |
| | 1 | 11 | 1 |
| 01 | 0 | 00 | 0 |
| | 1 | 00 | 0 |
| 10 | 0 | 01 | 1 |
| | 1 | 10 | 0 |
| 11 | 0 | 10 | 0 |
| | 1 | 10 | 0 |

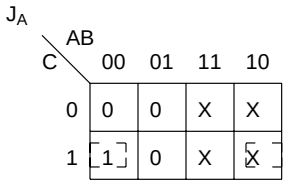
At this stage we must decide on a method of implementation. Let us assume that, as in the example in the text, we are to use J–K flip-flops. The control inputs of these devices may be described by the following table

| Present state $Q_n$ | Next state $Q_{n+1}$ | Control inputs required J | K |
|---|---|---|---|
| 0 | 0 | 0 | X |
| | 1 | 1 | X |
| 1 | 0 | X | 1 |
| | 1 | X | 0 |

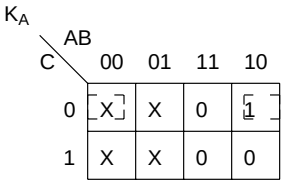
and thus we can construct an excitation table as below.

| Present state AB | Input conditions D | Next state AB | Flip-flop inputs $J_A$ | $K_A$ | $J_B$ | $K_B$ | Output Q |
|---|---|---|---|---|---|---|---|
| 00 | 0 | 00 | 0 | X | 0 | X | 0 |
| | 1 | 11 | 1 | X | 1 | X | 1 |
| 01 | 0 | 00 | 0 | X | X | 1 | 0 |
| | 1 | 00 | 0 | X | X | 1 | 0 |
| 10 | 0 | 01 | X | 1 | 1 | X | 1 |
| | 1 | 10 | X | 0 | 0 | X | 0 |
| 11 | 0 | 10 | X | 0 | X | 1 | 0 |
| | 1 | 10 | X | 0 | X | 1 | 0 |

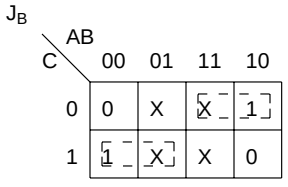
This may be implemented by hardware as shown in Figure 10.58 of the text, where the details of the combinational logic are described by the following Karnaugh maps.



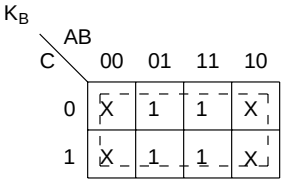

$J_A = \bar{B}D$




$K_A = \bar{B}\bar{D}$




$J_B = A\bar{D} + \bar{A}D$




$K_B = 1$

The output logic is described by the following Karnaugh map.

Q

| C \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 |

$Q = A\bar{B}\bar{D} + \bar{A}\bar{B}D$

The combinational logic required may then be implemented directly as described in Section 10.12.1.

This circuit has no unused states.

**10.20** The design methodology for this exercise is as described in Section 10.21.1.

The state diagram may be used to form a state transition table. In this table the input is labelled $D$ and the output $Q$.

| Present state | Input conditions D | Next state | Output Q |
|---|---|---|---|
| $S_0$ | 0 | $S_1$ | 0 |
| | 1 | $S_4$ | 1 |
| $S_1$ | 0 | $S_1$ | 0 |
| | 1 | $S_2$ | 1 |
| $S_2$ | 0 | $S_3$ | 1 |
| | 1 | $S_3$ | 1 |
| $S_3$ | 0 | $S_0$ | 0 |
| | 1 | $S_3$ | 0 |
| $S_4$ | 0 | $S_3$ | 1 |
| | 1 | $S_3$ | 1 |

Inspection of the state table will show that all the states are unique and that no state reduction is possible.

For a system with 5 internal states, three internal variables are needed. These are assigned as shown below

| State | Internal variables ABC |
|---|---|
| $S_0$ | 000 |
| $S_1$ | 001 |
| $S_2$ | 010 |
| $S_3$ | 011 |
| $S_4$ | 100 |

This allows us to represent the state transition table in terms of the internal variables.

| Present state ABC | Input conditions D | Next state ABC | Output Q |
|---|---|---|---|
| 000 | 0 | 001 | 0 |
| | 1 | 100 | 1 |
| 001 | 0 | 001 | 0 |
| | 1 | 010 | 1 |
| 010 | 0 | 011 | 1 |
| | 1 | 011 | 1 |
| 011 | 0 | 000 | 0 |
| | 1 | 011 | 0 |
| 100 | 0 | 011 | 1 |
| | 1 | 011 | 1 |

At this stage we must decide on a method of implementation. Let us assume that, as in the example in the text, we are to use J–K flip-flops. The control inputs of these devices may be described by the following table

| Present state $Q_n$ | Next state $Q_{n+1}$ | Control inputs required J | K |
|---|---|---|---|
| 0 | 0 | 0 | X |
| | 1 | 1 | X |
| 1 | 0 | X | 1 |
| | 1 | X | 0 |

and thus we can construct an excitation table as below.

| Present state ABC | Input conditions D | Next state ABC | Flip-flop inputs | | | | | | Output |
|---|---|---|---|---|---|---|---|---|---|
| | | | $J_A$ | $K_A$ | $J_B$ | $K_B$ | $J_C$ | $K_C$ | Q |
| 000 | 0 | 001 | 0 | X | 0 | X | 1 | X | 0 |
| | 1 | 100 | 1 | X | 0 | X | 0 | X | 1 |
| 001 | 0 | 001 | 0 | X | 0 | X | X | 0 | 0 |
| | 1 | 010 | 0 | X | 1 | X | X | 1 | 1 |
| 010 | 0 | 011 | 0 | X | X | 0 | 1 | X | 1 |
| | 1 | 011 | 0 | X | X | 0 | 1 | X | 1 |
| 011 | 0 | 000 | 0 | X | X | 1 | X | 1 | 0 |
| | 1 | 011 | 0 | X | X | 0 | X | 0 | 0 |
| 100 | 0 | 011 | X | 1 | 1 | X | 1 | X | 1 |
| | 1 | 011 | X | 1 | 1 | X | 1 | X | 1 |
| 101 | XX | XXX | X | X | X | X | X | X | X |
| 110 | XX | XXX | X | X | X | X | X | X | X |
| 111 | XX | XXX | X | X | X | X | X | X | X |

This may be implemented by hardware as shown in Figure 10.58 of the text, where the details of the combinational logic are described by the following Karnaugh maps.

$J_A$

| CD \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | X | X |
| 01 | 1 | 0 | X | X |
| 11 | 0 | 0 | X | X |
| 10 | 0 | 0 | X | X |

$J_A = \overline{B}\overline{C}D$

$K_A$

| CD \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | X | X | X | 1 |
| 01 | X | X | X | 1 |
| 11 | X | X | X | X |
| 10 | X | X | X | X |

$K_A = 1$

$J_B$

| CD \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | X | X | 1 |
| 01 | 0 | X | X | 1 |
| 11 | 1 | X | X | X |
| 10 | 0 | X | X | X |

$J_B = B + CD$

$K_B$

| CD \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | X | 0 | X | X |
| 01 | X | 0 | X | X |
| 11 | X | 0 | X | X |
| 10 | X | 1 | X | X |

$K_B = C\overline{D}$

$J_C$

| CD \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 1 | X | 1 |
| 01 | 0 | 1 | X | 1 |
| 11 | X | X | X | X |
| 10 | X | X | X | X |

$J_C = \overline{D} + B + A$

$K_C$

| CD \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | X | X | X | X |
| 01 | X | X | X | X |
| 11 | 1 | 0 | X | X |
| 10 | 0 | 1 | X | X |

$K_C = \overline{B}D + B\overline{D}$

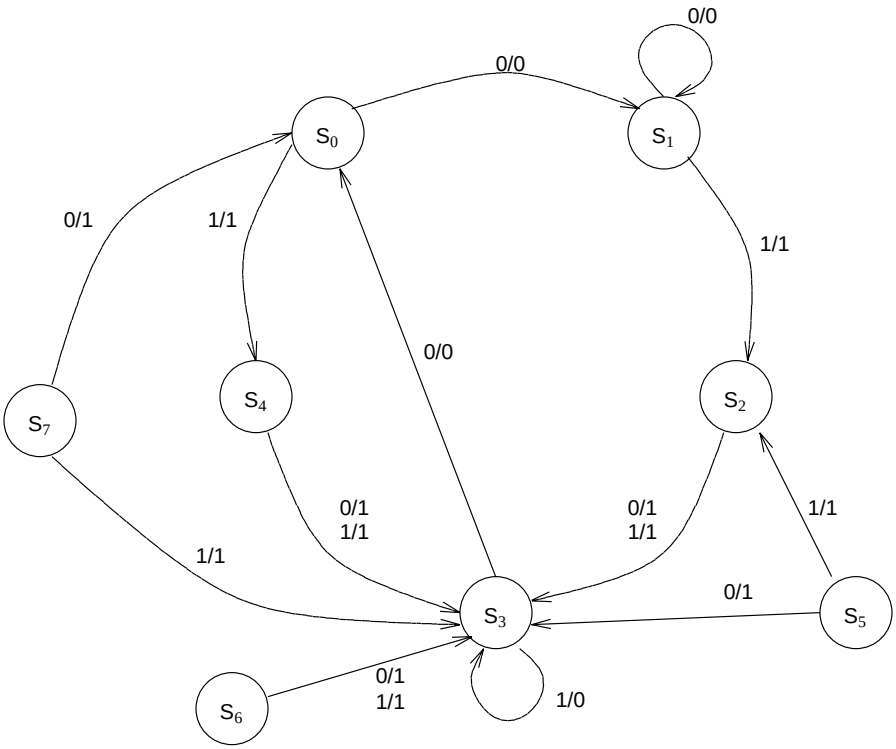
The output logic is described by the following Karnaugh map. The combinational logic required may then be implemented directly as described in Section 10.12.1.

Q

| CD \ AB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 1 | X | 1 |
| 01 | 1 | 1 | X | 1 |
| 11 | 1 | 0 | X | X |
| 10 | 0 | 0 | X | X |

$Q = A + B\overline{C} + \overline{B}D$

Having designed the counter it is now necessary to investigate the nature of the unused states to ensure that the counter starts correctly. A full transition diagram is as follows.




It is clear from the above diagram that the unused states cause no problems. In each case after a single clock cycle the system will be in one of the used states.

# Chapter 11
# DIGITAL DEVICES

**11.1** Typical logic voltages at the output of a TTL gate are 3.4 V for a logical 1, and 0.2 V for a logical 0. The input and output voltage ranges are given in Figure 11.20 of the text.

Typical logic voltages at the output of a CMOS gate are very close to the supply rails. More details on the input and output voltage ranges are given in Figure 11.32.

**11.2** The meanings of these terms are given in the text. Discussion of the various topics may be found using the index.

**11.3** There is no perfect answer to this question. One could suggest that suitable answers might be: (a) ECL, FAST TTL or Advanced Schottky TTL; (b) CMOS and (c) CMOS.

**11.4** The meanings of these terms are given in the text. Discussion of the various topics may be found using the index.

**11.5** Schottky TTL devices use Schottky transistors which do not saturate. This removes the effects of storage time which limits the speed of conventional TTL circuits.

**11.6** ECL is faster than TTL because the transistors in ECL gates are working within their active region and are prevented from entering saturation. In TTL circuits (other than Schottky versions) the transistors are driven into saturation. They are therefore subject to storage time when turning OFF.

**11.7** The transfer characteristic of a typical TTL gate is given in Figure 11.22 of the text.

**11.8** The circuit can be simulated easily in PSpice. Suitable transistors might be type Q2N2222 and suitable diodes type 1N914. Connect a VSRC voltage source to the input and setup the simulation to perform a DC sweep of this voltage from 0 to 5 V in 0.1V steps. Initially connect a 1k resistor from the output to ground. After the analysis run probe and look at the output voltage. This should show a transfer function similar to that given in the text in Figure 11.22. Removing the resistor at the output increases the logic 1 output voltage to about 5V.

**11.9** 7400 family devices are specified over a temperature range of from 0 to 70°C, while 5400 parts can be used from −55 to 125°C.

**11.10** NMOS gates suffer from a high output resistance in one of their output states which limits the speed at which they can charge capacitive loads. CMOS devices have a relatively low output impedance in both states and are therefore faster in operation. CMOS gates also have a lower power consumption than NMOS gates as one of the push-pull output devices is always turned OFF in the steady state. NMOS devices are easier to fabricate than CMOS parts since only one polarity of transistors is required.

**11.11** The minimum noise immunity for TTL is 0.4 V, and for CMOS is $0.3 \times V_{DD}$. If CMOS is operated from a 5 V supply, as for TTL, this gives a noise immunity of 1.5 V, which is considerably greater than that of TTL.

**11.12** (a) Unused TTL NOR gate inputs should be connected to ground.

(b) Unused TTL AND gate inputs should be connected to the positive supply through a resistor.

(c) Unused CMOS OR gate inputs should be connected to ground.

(d) Unused CMOS NAND gate inputs should be connected to the positive supply rail.

**11.13** The various MOS technologies are most widely used for VLSI applications because their circuits require very little chip area and dissipate little power. Low power dissipation allows large amounts of circuitry to be integrated into a single chip without exceeding the operating temperature of the material.

Of the MOS technologies CMOS is now established as the dominant family with most new designs adopting this approach. This is more complex to produce than NMOS but has advantages of increased speed and lower power consumption.

**11.14** (a) The outputs of totem-pole TTL gates may not be joined together.

(b) The outputs of open collector TTL gates may be freely connected to a single pull-up resistor to produce a ‘wired-AND’ function.

(c) The outputs of three-state gates may be joined provided that the output of only one gate is enabled at any one time.

**11.15** The power consumption of CMOS gates may be reduced by decreasing the clock rate. The static power consumption of CMOS circuitry is negligible in most applications.

**11.16** Because the logic levels and current requirements are not directly compatible.

**11.17** The operation and function of a Schmitt trigger are described in Section 11.6.3 of the text.

**11.18** The primary uses of both open collector and three-state gates are in the production of bus systems and in other forms of signal multiplexing.

**11.19** The function of opto-isolators in reducing noise pick-up is discussed in Section 11.6.3 of the text.

**11.20** Most CMOS gates are fitted with gate protection circuitry in the form of clamp diodes as discussed in Section 11.4.2. However, the current handling capacity of the diodes contained within i.c.s is limited and for extra protection in very noisy environments it is prudent to duplicate this circuitry externally using fast diodes with a high current capacity.

**11.21** The 74HC family of devices are high speed CMOS parts which operate at conventional CMOS logic levels. The 74HCT devices have a similar performance but their inputs and outputs use logic levels compatible with TTL gates allowing them to be used as direct, low-power, replacements for TTL parts.

**11.22** This can be achieved using open collector TTL gates by joining the outputs of many gates to a single pull-up resistor to form a wired-AND connection. This is described in Section 11.3.2 of the text.

**11.23** A relay could be driven using a high voltage open collector gate. The relay would be used in place of the pull-up resistor with the relay connecting the output to a 24 V supply. The data sheets on the relay and the TTL gate would need to be checked to ensure that the gate could provide the current required to operate the relay. Most high voltage open collector gates will operate with supply voltages of up to 30 V.

In order to protect the output of the gate from the back EMF produced by the relay, a catch diode should be fitted across the relay as described in Example 5.6.

**11.24** The term ’glue logic’ refers to the circuitry needed to *bolt together* the major components of circuits such as microcomputers. The term ’random logic’ describes a block of circuitry that contains an apparently *random* collection of various logic functions.

**11.25** The characteristics of PLAs, PALs and PROMs are described in Sections 11.5.1, 11.5.2 and 11.5.4 respectively. The main point being sought here is that these three forms of logic device are very similar architecturally. In particular each has an AND array and an OR array. The main difference between them is that: in a PLA both arrays are programmable; in a PAL the AND array is programmable and the OR array is fixed; and in a PROM the OR array is programmable and the AND array is fixed.

**11.26** The characteristics of CPLDs and FPGAs are described in Sections 11.5.5 and 11.5.6 respectively.

**11.27** In CMOS gates the current consumption is negligible when the device is static, but a surge of current is passed as the circuit switches from one state to another. In systems where a large number of CMOS gates are switched synchronously from a single clock this produces large current surges which are many times greater than the average value. Any resistance or inductance in the power supply lines converts these current surges into voltage spikes.

# Chapter 12
# MICROCOMPUTERS

**12.1** A suitable block diagram is given as Figure 12.1 of the text.

**12.2** The main components of the CPU of a typical 8-bit microprocessor are described in Section 12.3.1.

**12.3** In a bus system the outputs of a number of gates are joined together to allow information to flow onto a common data highway. However, if the outputs of two conventional gates are joined together they will oppose each other and the state of the resultant signal will be indeterminate. The solution is to use three-state gates and to enable only one output at any one time. This allows any one of the outputs to drive the bus without conflict.

**12.4** The essential principle here is that before jumping to a subroutine the processor stores away in memory the current contents of its program counter. The value stored represents the location of the instruction following the 'jump to subroutine' instruction, and is termed the 'return address'. At the end of the subroutine the processor retrieves the return address and replaces it in the program counter. At the end of this process the processor performs an instruction fetch and is now back in its original sequence of instructions.

If the processor stored the current contents of the program counter in a fixed location problems would occur if one subroutine called another, since the original contents would be overwritten by the second return address. This problem is overcome by storing the return address on the stack. Subroutines can then be nested in the same way that interrupts are nested (see Section 12.5.5).

**12.5** Bus multiplexing is discussed in Section 12.3.2 of the text.

**12.6** a) A 64 kbyte ROM requires 16 address lines.

b) A 2 kbyte RAM requires 11 address lines.

c) A 64 kbit (8 k $\times$ 8 bits) ROM requires 13 address lines.

**12.7** These terms are discussed in Section 12.5 of the text. Discussions of the individual terms may be located using the index.

**12.8** These input/output methods are discussed in Section 12.5.1 of the text.

**12.9** The use of the stack in interrupt handling is covered in Section 12.5.5.

**12.10** System vectors would normally be stored in ROM since this is non-volatile. If stored in RAM the values would disappear when the system was turned off and would therefore not be available when the system was restarted.

**12.11** This refers to the order in which the bytes of addresses are stored in memory. Some store the most significant part of the address first (that is at the lower address location) and then store the least significant part of the address at the next highest location. Other systems store the least significant part of the address first. The two techniques are often referred to as ‘high-byte, low-byte’ and ‘low-byte, high-byte’.

**12.12** EEPROM is normally considered to be a ROM, rather than a non-volatile RAM, because although it can be read at full operating speeds it can be written (or programmed) only relatively slowly.

**12.13** The processor cannot distinguish between programs and data within memory. It simply executes the programs it is given and assumes that programs and data are where they should be.

**12.14** (a) Reading push buttons in a computer controlled washing machine is probably more suited to the use of polling.

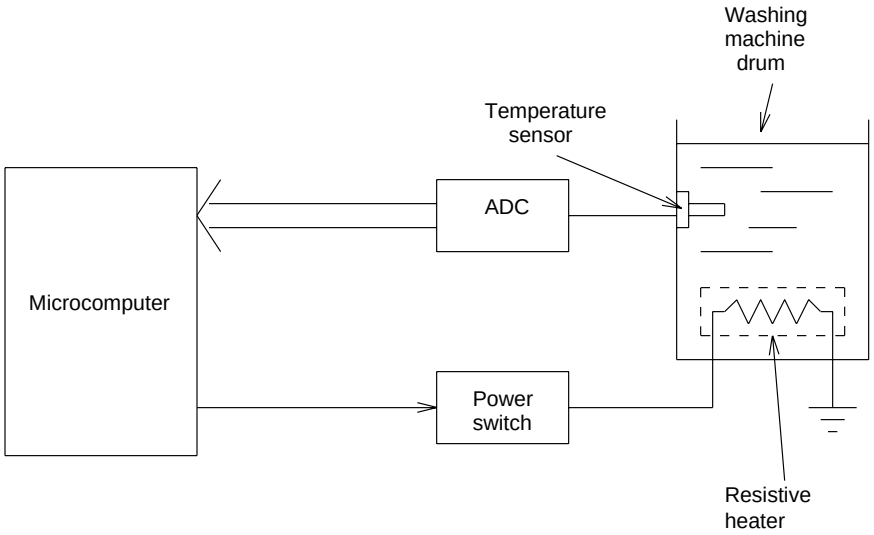
(b) Interfacing a keyboard to a personal computer is more suited to interrupt driven techniques, since polling would waste a considerable amount of processor time.

(c) Connecting a high-speed disk drive to a computer is a suitable application for DMA because of the need for high speed block transfers.

**12.15** A FIFO is a ‘first-in-first-out’ structure. Examples of such an arrangement include print queues and keyboard buffers. A FILO is a ‘first-in-last-out’ structure. An example of such an arrangement is the stack in a microprocessor.

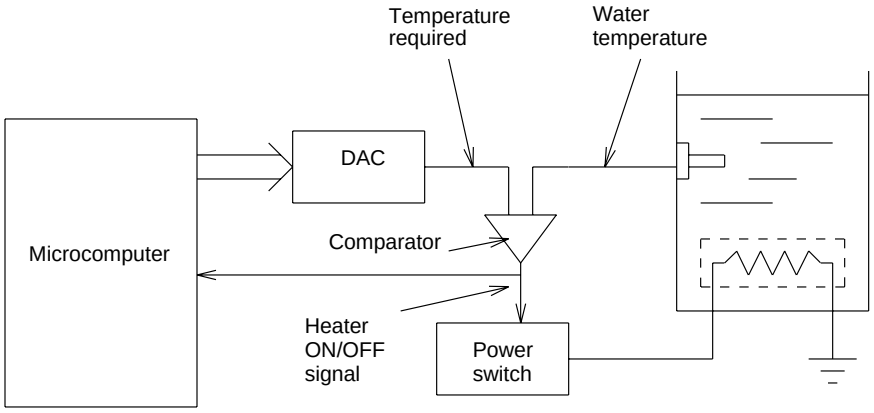
**12.16** A ‘turn-key’ system is one which starts executing automatically when it is turned on. This is achieved by storing the application software in a non-volatile memory device (such as a ROM or EPROM) and storing an appropriate reset vector (also in non-volatile memory) to point to the start of the program.

**12.17** An obvious approach to the control of water temperature is to adopt a closed loop control based on some form of temperature sensor, an analogue to digital converter (ADC) and a power switch to turn the heater on and off (ADCs are discussed in Chapter 13). A typical arrangement is shown below.



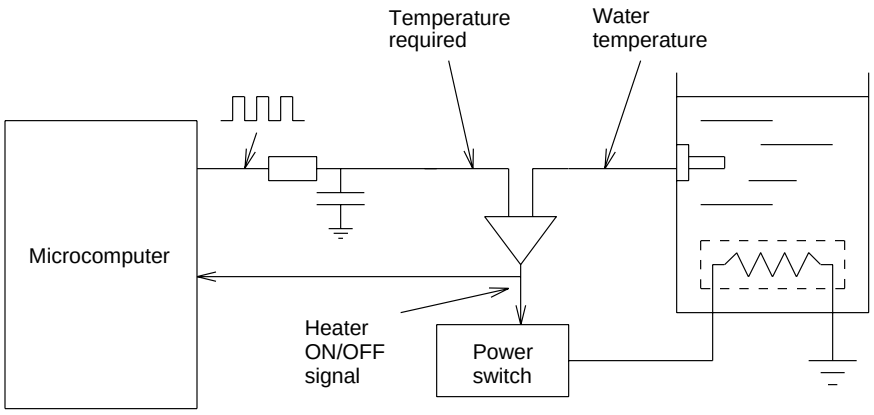

Using this arrangement the microcomputer is able to monitor the current temperature of the water and to turn the heater on or off as appropriate. A typical sensor would be a thermister since they are inexpensive and very robust. The power switch would probably take the form of a triac as in the Design Study of Chapter 12.

The above solution is perhaps an obvious approach to this problem but is not an attractive method for a high volume product such as a washing machine. The ADC is a relatively expensive component and it is worth looking at ways of removing this from the design. Consider the following approach.




In the previous approach we sensed the actual water temperature and compared this within the computer with the required temperature. In this second method we output the required temperature and compare this externally with the actual temperature. The signal is output from the processor in a parallel form and is converted to analogue using a digital to analogue converter (DAC). This signal is compared with the signal from the temperature sensor using an analogue comparator and the output of this operation is used to control the heater switch. It is thus the comparator which controls the heater rather than the microcomputer itself. The heater on/off signal is fed back to the computer to tell the processor when the water has reached the appropriate temperature.

This second approach has the advantage of dispensing with the ADC, but instead needs a DAC. Fortunately the latter is less expensive than the former, but this is still not an ideal method. Consider instead the arrangement shown below.




Here both the ADC and the DAC have been removed. The arrangement is similar to the previous method except that much of the function of the DAC has been absorbed into the microcomputer. The processor now outputs a train of pulses on a single output line. This pulse train is generated such that its mark to space ratio represents the required temperature. If a train of all '1's is output the average value of the waveform is equal to the high logic level. This represents the highest temperature. If a train of '0's is output the average value of the waveform is equal to the low logic level. This represents the lowest temperature. Intermediate temperatures are represented by an appropriate sequence of '1's and '0's. Externally a simple low pass filter formed by a resistor and a capacitor is used to turn the pulse train into an appropriate d.c. value representing the required temperature.

This final method places an increased computational load on the processor (although some modern processors have hardware facilities which simplify this process) in order to greatly reduce the external hardware required. In this final version the hardware is reduced to a few very simple components costing only a few pence. This approach is very attractive for a high volume product where hardware costs are all important. It should be remembered that this approach does require the provision of additional software to implement this function. Because of the high cost of this software it is likely that this approach would not be adopted for a similar low volume application.

It is worth noting that the thermal time constant of the water in a washing machine is long compared with the time for which the water is used. It is therefore not necessary to continually monitor the water temperature and turn on and off the heater. It is normally sufficient to bring the water up to the correct temperature and then to continue with the wash program relying on the fact that the water temperature will not change appreciably before it is pumped out. The only case where this is not true is where washing is soaked for long periods at a fixed temperature.

The user push-buttons of a washing machine are used before the machine starts its wash cycle. During this time the machine is doing little else and it is therefore quite acceptable to use the processor's time to poll the input buttons. When the 'start' button is pressed the machine begins to wash clothes and can now ignore the push-buttons. The master on/off switch can be used to turn off the machine if necessary, this being safer than having a dedicated button read by the processor (see the Design Study at the end of Chapter 14 for further discussion of this point). The use of polling is preferred to the use of interrupts since the latter requires more complicated hardware (usually) and is more difficult to test.

# Chapter 13
# DATA ACQUISITION AND CONVERSION

**13.1** The main components of a typical data acquisition system are: signal conditioning units; anti-aliasing filters; an analogue or digital multiplexer; one or more analogue to digital converter and some form of processor.

**13.2** The 'Nyquist rate' is the minimum rate at which a signal may be sampled in order to gain sufficient information to allow reconstruction of the signal. This is numerically equal to twice the highest frequency component in the signal.

A 2 kHz signal must be sampled at not less than 4 kHz, although normally it would be sampled at a somewhat higher frequency to allow for non-ideal filtering of the signal. Sampling below this frequency would result in 'aliasing' as described in Section 13.2.

**13.3** The terms resolution and accuracy are defined at the beginning of Section 13.3 of the text.

**13.4** The binary-weighted resistor method has the advantage of simplicity in that less resistors are used. However, in this method the resistors have a wide range of values and therefore suffer from temperature drift as the resistors are affected differently by temperature changes.

In the R–2R resistor chain method the resistors are all of similar values and so will tend to drift equally with temperature producing a more stable result.

**13.5** Modifying the circuit of computer simulation exercise 13.1 (FILE13A) to represent the *R-2R* converter should produce similar results.

**13.6** A comparison of the performance of successive approximation and counter ADCs is given in Section 13.3.2 of the text.

**13.7** The advantage and disadvantages of parallel analogue to digital converters are discussed in Section 13.3.2. Essentially they are fast but expensive.

**13.8** The use of sample and hold gates, and the meaning of 'droop' are described in Section 13.3.3 of the text.

**13.9** ‘Single-chip data acquisition systems’ are discussed in Section 13.4 of the text.

**13.10** Since a speech signal includes frequency components above 3.4 kHz, the signal must first be filtered to remove high frequency components. A filter with a cut-off frequency of 3.4 kHz could be used but since all real filters are non-ideal it would be necessary to sample at somewhat more than twice this frequency to prevent aliasing. A frequency of 20% above the Nyquist rate gives a value of about 8.2 kHz. If each sample requires 8 bits of data this represents $8 \times 8.2 \times 10^3 \approx 65{,}600$ bits per second.

**13.11** The block diagram given in the Design Study of Chapter 13 provides a suitable solution to this Exercise. In this case the anti-aliasing and reconstruction filters should both have cut-off frequencies of 3.4 kHz and the sampling rate of each channel should be 8.2 kHz. This implies that the data converters and the microcomputer must be able to perform about 65,000 samples per second (about 15 μs per conversion). 8-bit converters are required.

# Chapter 14
# SYSTEM DESIGN

**14.1** The major tasks associated with the design of an electronic system are listed and described in Section 14.2 of the text.

**14.2** The customer's requirements are what the system should do. The specification is an attempt to describe a system to perform this task.

**14.3** The role of the specification is to define the *problem* not the *solution*. If the specification includes implementation details it will restrict the designer in his approach to the problem. It is quite likely that the appropriate method of implementing the system will not be clear when the specification is written but will come to light as part of the design phase.

**14.4** The factors affecting the hardware/software trade-off are discussed in the section on top-level design in Section 14.2.

**14.5** A 'top-down' approach involves starting with the overall system and progressively looking at more and more detailed aspects of it. A 'bottom-up' approach starts with the detail of individual sections of the system, and gradually works up to the complete system. Design is normally performed in a 'top-down' manner and testing usually follows a 'bottom-up' approach.

**14.6** Individual modules are tested separately before being assembled into a complete system since testing is easier, and can be carried out more thoroughly, when applied to small sections of the system. It is also sensible to ensure that each module will not cause harm to other modules, or the overall system, before connecting them together.

**14.7** A comparison of analogue and digital systems is given in Section 14.3.

**14.8** A comparison of programmable and non-programmable techniques is given in Section 14.3 of the text.

**14.9** Schematic capture packages, and their interaction with other tools, are discussed in Section 14.4.1.

**14.10** Circuit simulation, PCB layout, PLD design and programming, and design verification tools are discussed in Section 14.4 of the text.

**14.11** System specification languages are discussed in Section 14.4.7 of the text.